

DISPLAY Elektronik GmbH

DATA SHEET

MIP-DISPLAY

DE MIP128128A-W-PW

(1,03" Memory in Pixel, Mono, incl. Backlight)

Product Specification

Version: 0

06.03.2026

Revision History

| VERSION | DATE | REVISED PAGE NO. | Note |
|----------------|-------------|-------------------------|---------------|
| 0 | 06.03.2026 | | First Release |

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1. Applicable Memory Liquid Crystal Display

This TFT-LCD Module is a reflective Active-Matrix with slightly transmissive memory liquid crystal display module with CG-Silicone Thin Film Transistor Module outline is indicated in Figure 14-1

2. Overview

- Reflective Active-Matrix with slightly transmissive Panel of White and Black.
- 1.03" Screen has 128 x 128 Dots resolution.
- 1 Pixel has each 1bit, the Pixel can display 2 Colors.
- Display Control by Serial Data Signal Communication.
- Arbitrary Line Data renewable.
- 1bit internal Memory for Data Storage within the Panel.
- Thin, light-weight and compact Module with monolithic technology.
- Super Low Power Consumption TFT Panel.
- Front Polarizer Surface is HardCoat.
- With FPC (Applicable Connector: Ref to recommended connector on Table 8-1-1)

3. Mechanical Specification

Table 3-1 Module

| ITEM | SPECIFICATION | UNIT |
|--------------------|----------------------|------|
| Screen Size | 1.03" | Inch |
| Active Area | 18.56 x 18.56 | mm |
| Dot Configuration | 128 x 128 | Dot |
| Dot Pitch | 0.145 x 0.145 | mm |
| Pixel Array | Square | - |
| Display Mode | Normally White | - |
| Outline Dimensions | 24.29 x 28.66 x 1.78 | mm |
| Weight | 2.3 | g |
| Surface Treatment | HC (Hard-Coated) | - |

- Note:
1. Outline Dimension: WxHxD (incl. Backlight)
 2. Weight: max. with Backlight
 3. Detail Dimension and tolerance are shown in Figure 14-1

4. Input Terminal Names and Functions

Table 4-1 Pin description

| Terminal | Symbol | I/O | Configurations | Function | Remark |
|----------|----------|-------|----------------|--|----------|
| 1 | SCLK | INPUT | NoPull | Serial clock signal | |
| 2 | SI | INPUT | NoPull | Serial data input signal | |
| 3 | SCS | INPUT | NoPull | Chip select signal (Active of Hi) | |
| 4 | EXTCOMIN | INPUT | NoPull | External COM inversion signal input (Square wave) | Note 4-2 |
| 5 | DISP | INPUT | NoPull | ON/OFF Display ON/OFF signal | Note 4-1 |
| 6 | VDDA | POWER | — | Power supply (Analog) | Note 4-4 |
| 7 | VDD | POWER | — | Power supply (Digital) | Note 4-4 |
| 8 | EXTMODE | INPUT | NoPull | Control mode of COM inversion is select terminal | Note 4-2 |
| 9 | VSS | GND | — | GND (Digital) | Note 4-3 |
| 10 | VSSA | GND | — | GND (Analog) | Note 4-3 |

General Note: Neither Pulled up nor Pulled down.

The input terminals must not be in an indeterminate state (HiZ).

Note 4-1: The display ON/OFF signal is only for display.

Data on the memory will be saved at the time of ON/OFF.

When it's "Hi" data in the memory will display, when it's "Lo", white color will display and data in the memory will be saved.

Note 4-2: When EXTMODE is "Hi", EXTCOMIN signal is enable.

When EXTMODE is "Lo", serial input flag is enable.

"Hi" Mode: Connect the EXTMODE to VDD

"Lo" Mode: Connect the EXTMODE and EXTCOMIN to VSS

Note 4-3 Be sure to connect VSS and VSSA on the board.

(Connection near the connector is recommended)

Note 4-4 VDD ≥ VDDA

4.1 Input Signal States

Table 4-1-1 Input Signal States

| Symbol | I/O | Voltage (V) | 起動時 Boot | データ更新 (Update & Hold mode) | スタンバイ状態 Standby | 備考 note |
|----------|-------|-------------|-------------------------------------|---|---|--------------------------|
| SCLK | Input | 0 / 3.0 | Lo | Hi / Lo (Enter clk) | Lo | EXTMODE=Hi |
| | | | | | Hi / Lo (Enter clk) | EXTMODE=Lo Note 4-1-1 |
| SI | Input | 0 / 3.0 | Lo | Hi / Lo (Enter data) | Lo | EXTMODE=Hi |
| | | | | | Hi / Lo (Enter data) | EXTMODE=Lo Note 4-1-1 |
| SCS | Input | 0 / 3.0 | Lo | Hi (Enter data) | Lo | EXTMODE=Hi |
| | | | | | Hi / Lo (Enter data) | EXTMODE=Lo Note 4-1-1 |
| EXTCOMIN | Input | 0 / 3.0 | Lo | Hi / Lo (Input pulse (CLK) Signal) | Hi / Lo (Input pulse (CLK) Signal) | EXTMODE=Hi Note 4-1-2 |
| | | | | Lo | Lo | EXTMODE=Lo |
| DISP | Input | 0 / 3.0 | Lo | Hi / (Lo) | Hi / (Lo) | Note 4-1-3 |
| EXTMODE | Input | 0 / 3.0 | Hi / Lo (Change is not permitted) | | | Note 4-1-4 |

Common condition

- 1) Each Voltage values show typical voltage.
- 2) Booting
 - When just input Power supply Between PowerON and Input Signal.
- 3) Data Update & Hold mode
 - Updates data in pixel memory. (1Line and Multiple Lines update)
- 4) Standby
 - Maintains memory internal data and maintain current display
- 5) Keep "Lo" Serial Signal (SCS / SI / SCLK) without communicating.
 - Not to make a SCS terminal "Hi" when it does not communicate.
- 6) VDD ≥ VDDA, VSS = VSSA = GND = 0V

[Note 4-1-1] :

To do VCOM control in a serial communication, a periodic signal transmission is necessary and is here.

[Note 4-1-2] :

Input (Clock pulse) is always needed during displaying.

[Note 4-1-3] :

When displaying it, it's driven "Hi" fixing.

[Note 4-1-4] :

Fixed to Hi or Lo. Recommend to connect VDD or GND (VSS)
Not change after starting power supply and during ON.

4.2 Recommended Circuit

4-2) Recommended Circuit

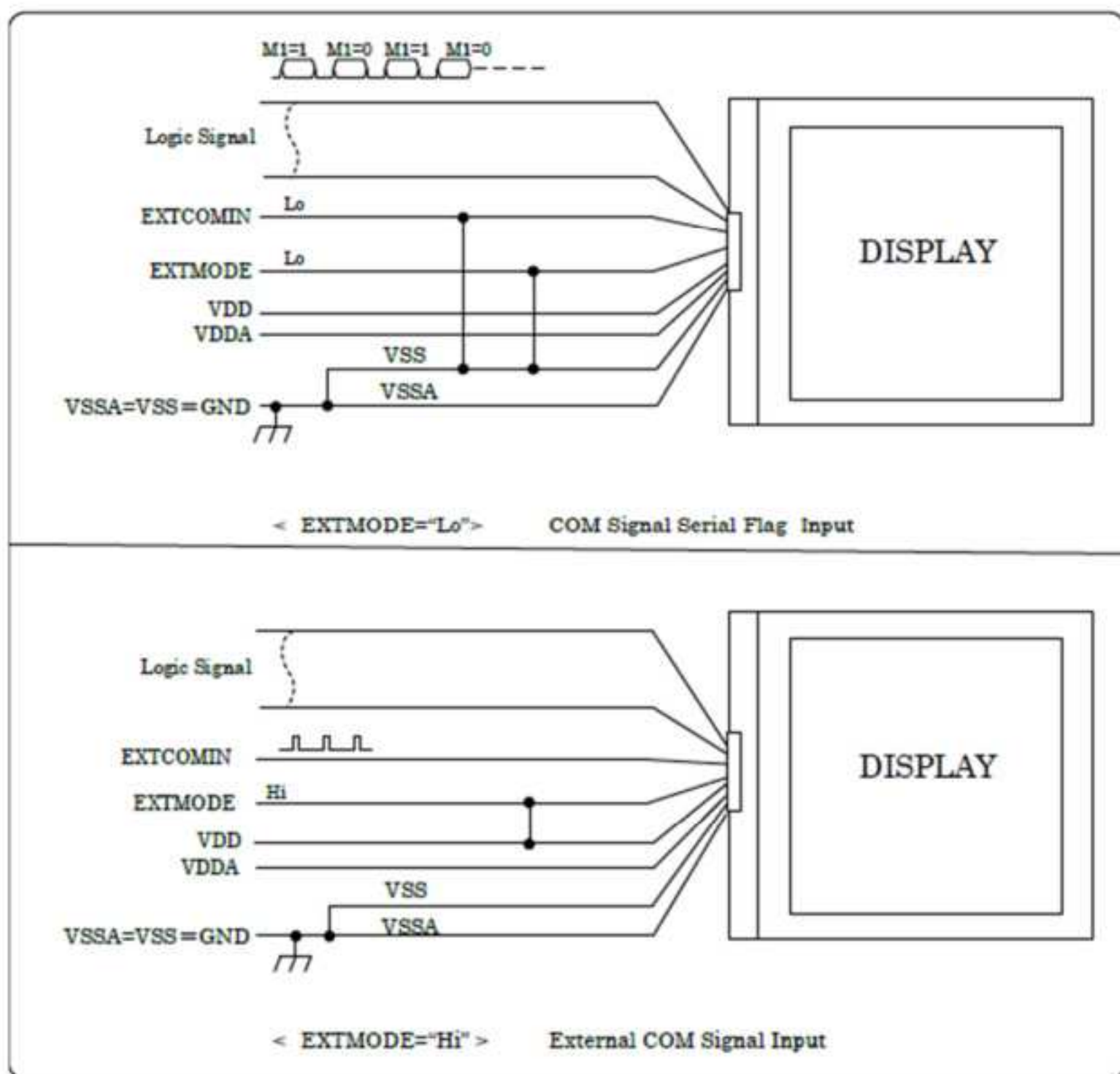


Figure 4-2-1 Recommended circuit

5 Absolute Maximum Rating

Table 5-1 Absolute Maximum Rating

| (GND = 0V) | | | | | | | |
|---|------------|------------|---|------|------|----------------------|--|
| Item | Symbol | Terminal | MIN. | MAX. | Unit | Remark | |
| Power supply voltage | V_VDDA | VDDA | -0.3 | +3.6 | V | Note 5-1 | |
| | V_VDD | VDD | -0.3 | +3.6 | V | Note 5-1 | |
| | V_VSS | VSS , VSSA | 0 | 0 | V | | |
| Input signal voltage | High Level | V_IH | SCLK , SI , SCS DISP , EXTCOMIN EXTMODE | - | VDD | V | |
| | Low Level | V_IL | | -0.3 | - | V | |
| Storage Temperature | Tstg | - | -30 | + 80 | ℃ | Note 5-2 Note 5-3 | |
| Operation Temperature (at panel surface) | Topr | - | -20 | + 70 | ℃ | Note 5-3 Note 5-4 | |

※ The absolute maximum rating is the limit value.

[General Note] Above Voltage value is a value based on VSS / VSSA (GND = 0V)
VSS=VSSA=GND

[Note 5-1] $VDD \geq VDDA$

[Note 5-2]
Do not exceed this temperature in any parts of module.

[Note 5-3

Humidity 95%RH Max. ($T_a \leq 40^\circ\text{C}$) Attention should be paid to static electricity Maximum wet bulb temperature is 39°C or lower. No condensation is allowed.
Condensation will cause electrical leak and may cause the module to not meet this specification.

[Note 5-4

Operating temperature is the temperature that guarantees only for the operation.
For contrast, response time, and other display quality determination, use $T_a = +25^\circ\text{C}$.

6 Electrical Characteristics

6.1 TFT LCD Panel Drive

Table 6-1-1 推奨駆動条件 Recommended operating Condition

(GND = 0V), Ta = +25°C

| Item | Symbol | Terminal | Min. | Typ. | Max. | Unit | Remark | |
|----------------------|------------|-----------|--|---------|------|---------|------------|--|
| Power supply Voltage | VVDDA | VDDA | +2.7 | +3.0 | +3.3 | V | Note 6-1-1 | |
| | VVDD | VDD | +2.7 | +3.0 | +3.3 | V | Note 6-1-1 | |
| | VVSS | VSS, VSSA | 0 | 0 | 0 | V | | |
| Input signal voltage | High Level | VIH | SCLK, SI, SCS DISP, EXTCOMIN | VDD-0.1 | VDD | VDD | V | |
| | | | EXTMODE | VDD | VDD | VDD | V | |
| | Low Level | VIL | SCLK, SI, SCS DISP, EXTCOMIN EXTMODE | VSS | VSS | VSS+0.1 | V | |

[General Note] Above Voltage value is a value based on VSS / VSSA (GND = 0V)
VSS=VSSA=GND

[Note 6-1-1] VDD ≥ VDDA

6-2) LED driving conditions

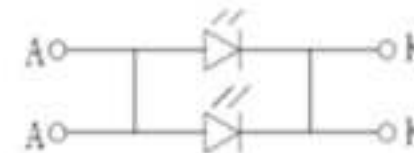
| Item | Symbol | Min | Typ | Max | Unit | Remark |
|-------------------|------------------|--------|-------|-----|------|------------------------|
| LED current | I _{LED} | - | 20 | - | mA | - |
| LED voltage | V _{LED} | 2.4 | 2.8 | 3.2 | V | Note 1 |
| Power consumption | P _{BL} | - | 0.056 | - | W | I _{LED} =20mA |
| LED life time | - | 50,000 | - | - | Hr | Note 2,3,4 |

Note 1 : There are 2 Groups LED

Note 2 : Ta = 25 °C

Note 3 : Brightness to be decreased to 50% of the initial value

Note 4 : The single LED lamp case.



6.2 Power Supply Sequence

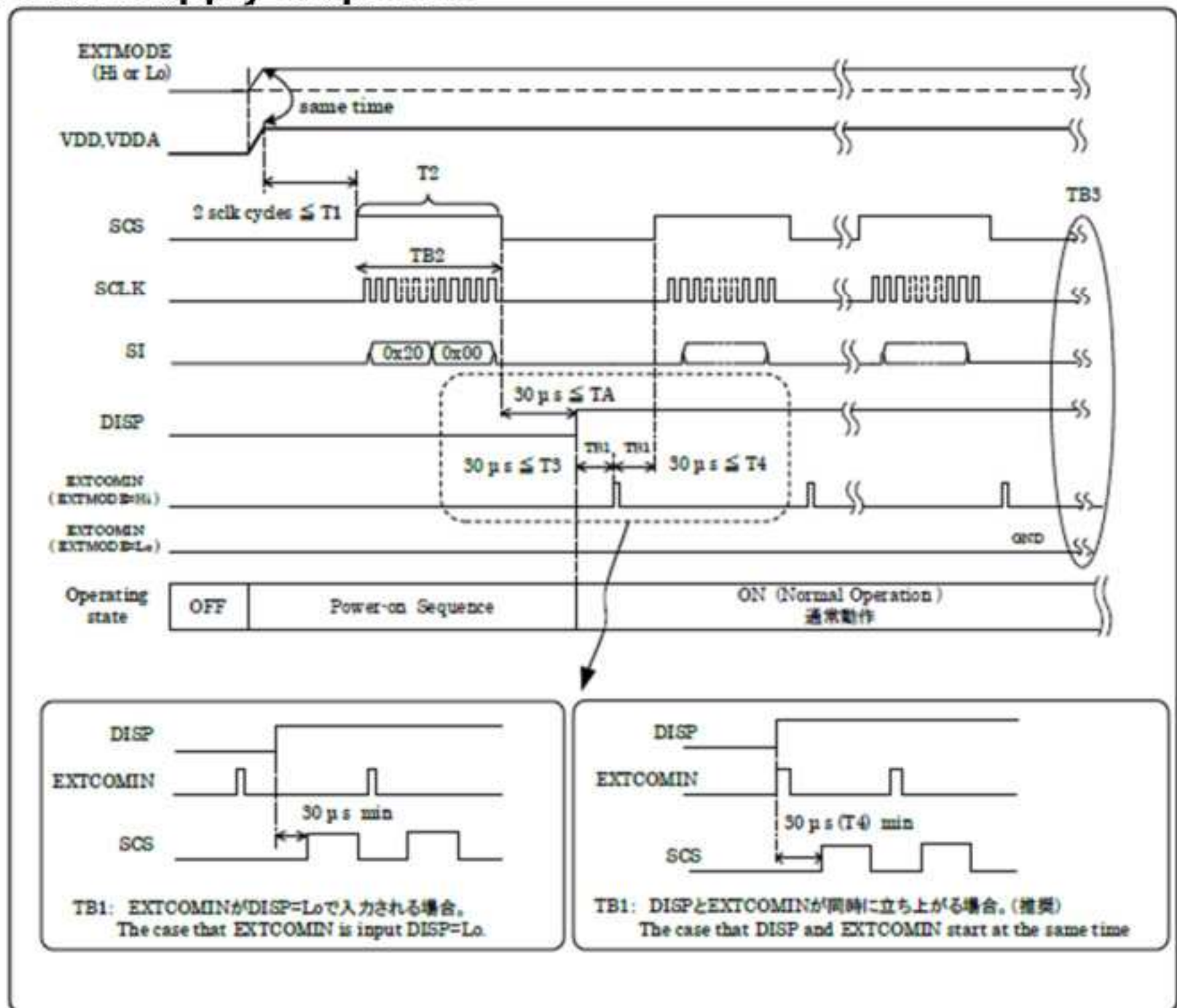


Figure 6-2-1 Power supply sequence

Refer to timing chart and AC timing characteristics for detail

[Note]

Precautions at the time of power on and power off.

When power on , VDD and VDDA are same time or VDD should be faster than the VDDA.

When power off, VDD and VDDA are same time or VDDA should be faster than the VDD.

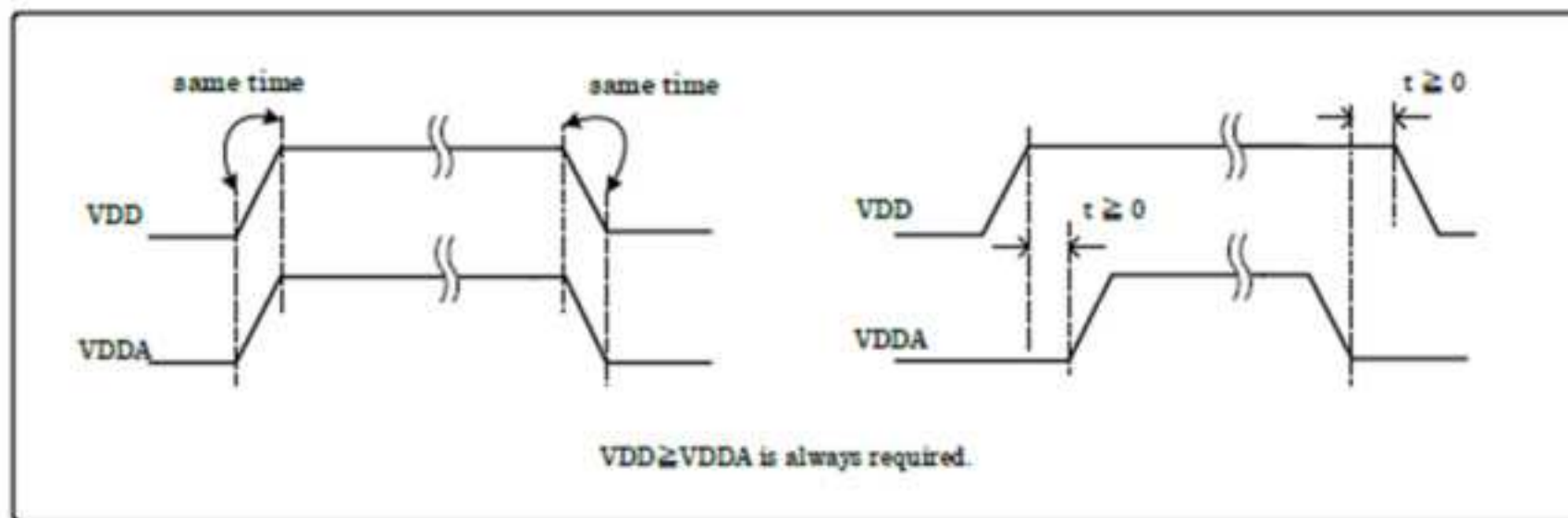


Figure 6-2-2 Power supply sequence

- T1 :
Please start the Signal transmission after a power supply was stable.
- TA :
Please set DISP to Hight Level after the completion of initialization.
- TB1 :
- TA and T3 may be opposite
(however, TCOM polarity inversion will not occur even with EXTCOMIN between DISP= "Lo".)
Also, when DISP and EXTCOMIN are simultaneously started up, allow 30us or more before SCS starts up. (It may be less than 60us).
- TB2
- Setting value for pixel memory initialization.
SCS=Driving accordingly to clear pixel internal memory method.
(use all clear flag or write all screen white)
S1=M2 (all clear flag) = "Hi" or write white.
SCLK : Normal Driving
- TB3 : SCSLK , SCS , S1 "Lo"
 •DISP ON "Hi"
 •EXTCOMIN
 EXTMODE= Lo "Lo"
 EXTMODE= Hi

•EXTMODE Hi / Lo

- Make SCLK,SI and SCS terminals "Lo" while it does not communicate.
- Keep "Hi" DISP terminal ,when power supply on (VDD).
- EXTCOMIN terminal
 This is valid the case of EXTMODE= "Lo" as EXTCOMIN= "Lo".
 This is valid the case of EXTMODE= "Hi" a periodic signal input is necessary.
- Not change (Hi to Lo or Lo to Hi) after starting power supply and during ON

[ON Sequence]

- 1) VDD,VDDA (IC)
 VDD and VDDA rise time (depends on IC).
- (2)
 T2 : 1 M2
 Pixel memory initialization
 T2 : 1 time or more Initialize with M2 (all clear flag) or write all screen white.
- (3) TCOM T3 : 30us
 DISP COM
 Release time for initialization of TCOM latch
 T3 : 30us or more
 Time required to release COM related latch circuit initialization which is initializing using DISP Signals.
- (4) TCOM T4 : 30us
 EXTCOMIN ICOM
 TCOM polarity initialization time. T4 : 30us or more
 Time required initializing TCOM polarity accordingly to EXTCOMIN input.

[Normal Operation]

Duration of normal driving.

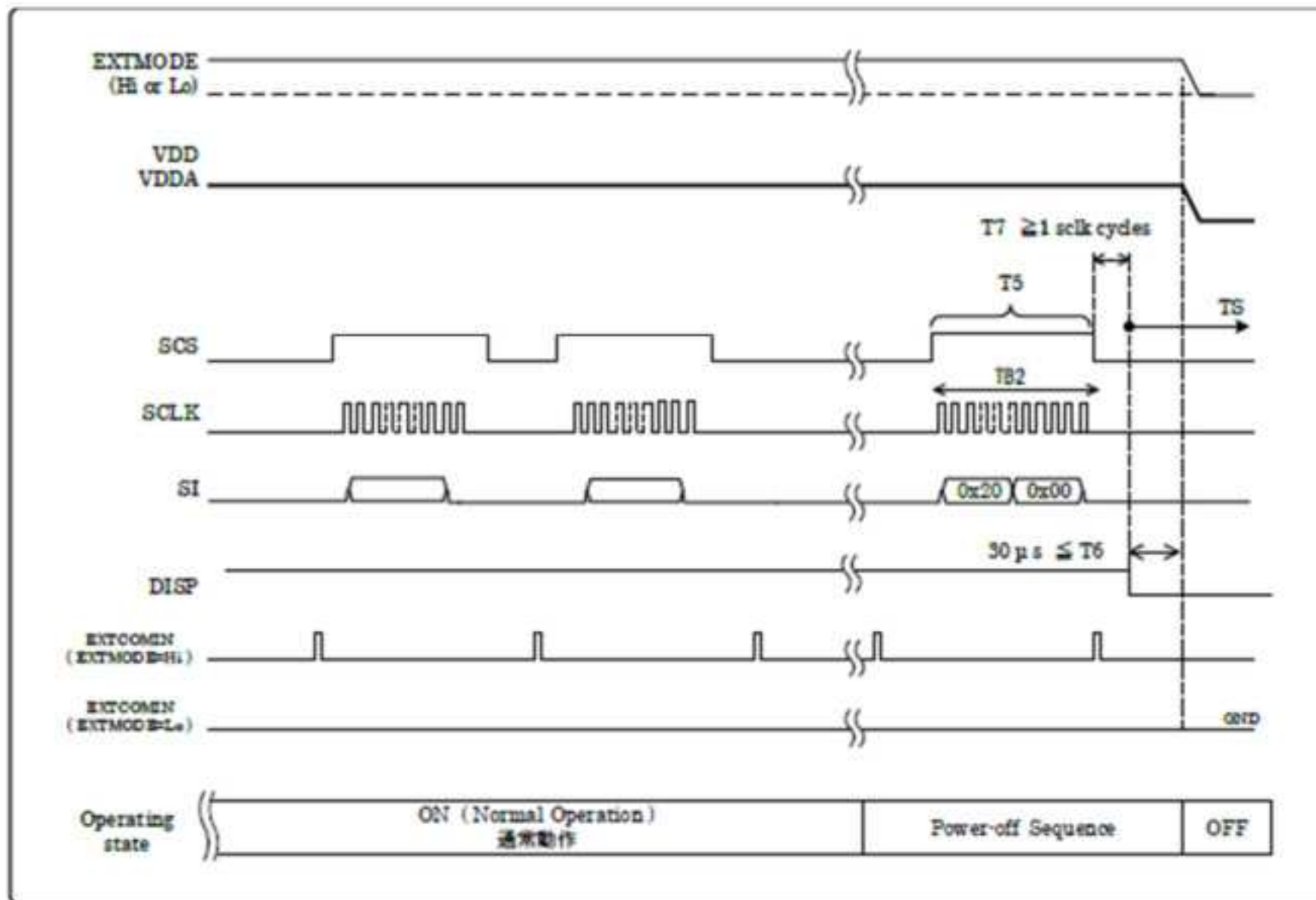


Figure 6-2-2 Power supply sequence

TS : Off control

Please turn off a power supply after making all the control signals into "Low Level", and passing the time of T6.

[Off Sequence]

- (5) Pixel memory initialization. T5 : Same (2)
- (6) VA,VB,VCOM initialization time. T6 : 30us or more
- (7) VDD and VDDA falling time (Depends on IC).

6.3 Input Signal Timing Parameters

Table 6-3-1 Input Signal timing Parameters

VDDA= +3.0V, VDD= +3.0V, GND=0V, Ta=25°C

| Signal | Item | Symbol | Min | Typ | Max | Unit | Remark |
|----------|-----------------|-------------|--------|-----|-----|------|--|
| SCS | Rise time | trSCS | - | - | 50 | ns | |
| | Fall Time | tfSCS | - | - | 50 | ns | |
| | SCS frequency | fSCS | - | - | 59 | Hz | Full screen update Note 6-3-1 Note 6-3-2 |
| | High duration | twhSCS | 153.45 | - | - | us | Data update mode Note 6-3-1 |
| | | | 22.54 | - | - | us | Hold mode Note 6-3-1 |
| | Low duration | twlSCS | 6 | - | - | us | |
| | Set up time | tsSCS | 6 | - | - | us | |
| | Hold time | thSCS | 2 | - | - | us | |
| SI | Rise time | trSI | - | - | 50 | ns | |
| | Fall time | tfSI | - | - | 50 | ns | |
| | Set up time | tsSI | 250 | - | - | ns | |
| | Hold time | thSI | 350 | - | - | ns | |
| SCLK | Clock frequency | fSCLK | - | 1.0 | 1.1 | MHz | |
| | Rise time | trSCLK | - | - | 50 | ns | |
| | Fall time | tfSCLK | - | - | 50 | ns | |
| | High duration | twhSCLK | 404.55 | 450 | - | ns | |
| | Low duration | twlSCLK | 404.55 | 450 | - | ns | |
| EXTCOMIN | Frequency | fEXTCOMIN | 57 | 60 | 66 | Hz | |
| | Rise time | trEXTCOMIN | - | - | 50 | ns | |
| | Fall time | tfEXTCOMIN | - | - | 50 | ns | |
| | High duration | twhEXTCOMIN | 2 | - | - | us | |
| DISP | Rise time | trDISP | - | - | 50 | ns | |
| | Fall time | tfDISP | - | - | 50 | ns | |

[Note 6-3-1]

Please keep SCS in the state of "Lo" when you maintain current display after writing of the display data.

[Note 6-3-2]

This spec applies only to full screen updates.
In updating only specific lines, this spec does not apply Therefore, please design based on other timing specifications.

※SCS, SI, SCLK, DISP, EXTCOMIN : 3.0V input voltage

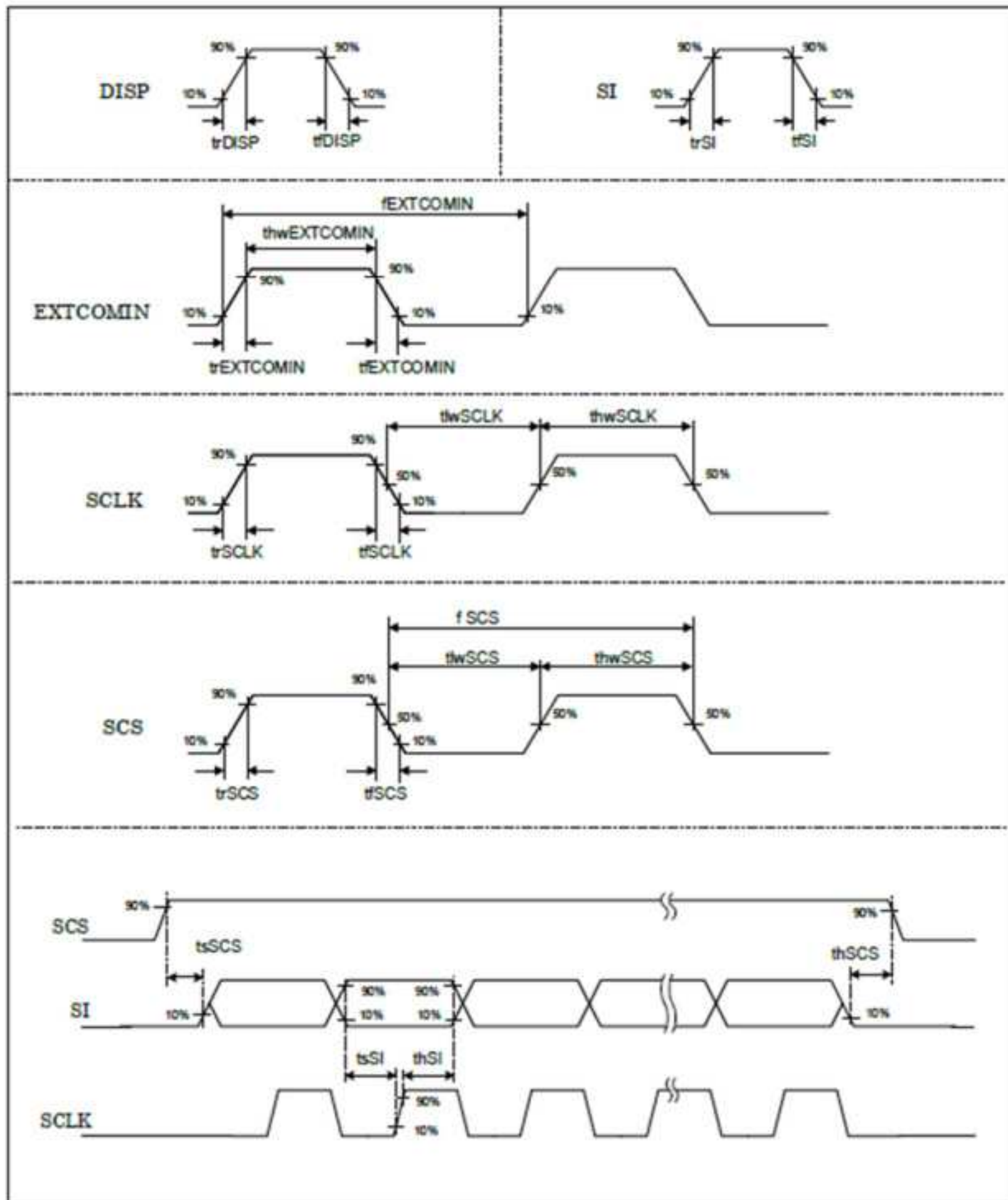


Figure 6-3-1

AC timing characteristics diagram

6.4 Power Consumption

Table 6-4-1 Current Consumption
 Input signal voltage (high) = +3.0 V, VDD= +3.0 V, VDDA= +3.0 V, Ta=25°C

| Condition | Power consumption | | Min | Typ | Max | Unit | Remark |
|-------------|-------------------|---|-----|-----|-----|------|------------|
| Condition 1 | Operating Mode | HOLD (no display data update) | - | 15 | 60 | μ W | Note 6-4-1 |
| | Display pattern | Black display | | | | | |
| Condition 2 | Operating Mode | Data update modewith display update (1fram/sec) | - | 45 | 120 | μ W | Note 6-4-2 |
| | Display pattern | Vertical stripe display | | | | | |

Common condition

VDD=3.0V, VDDA=3.0V, ICLK= 1.0MHz, EXTMODE=VDD, EXTCOMIN=60Hz

Update data on all screens.

Formula for computation

$$(I_{vdd} + I_{vdda}) [\mu A] \times 3.0 [V]$$

(Common Note)

This is value in steady condition, not the falve of peak power at the time of COM operation.

Some marging for power supply is recommended.

We recommend capacitor for VDD and VDDA.

(If VDD and VDDA are on separate systems, we recommend capacitor for each.)

[Note 6-4-1]

Condition 1 : Current measurement period of power supply.

tI_condition 1

Measurement time shall be EXTCOMIN cycles, at least 2 cycles.

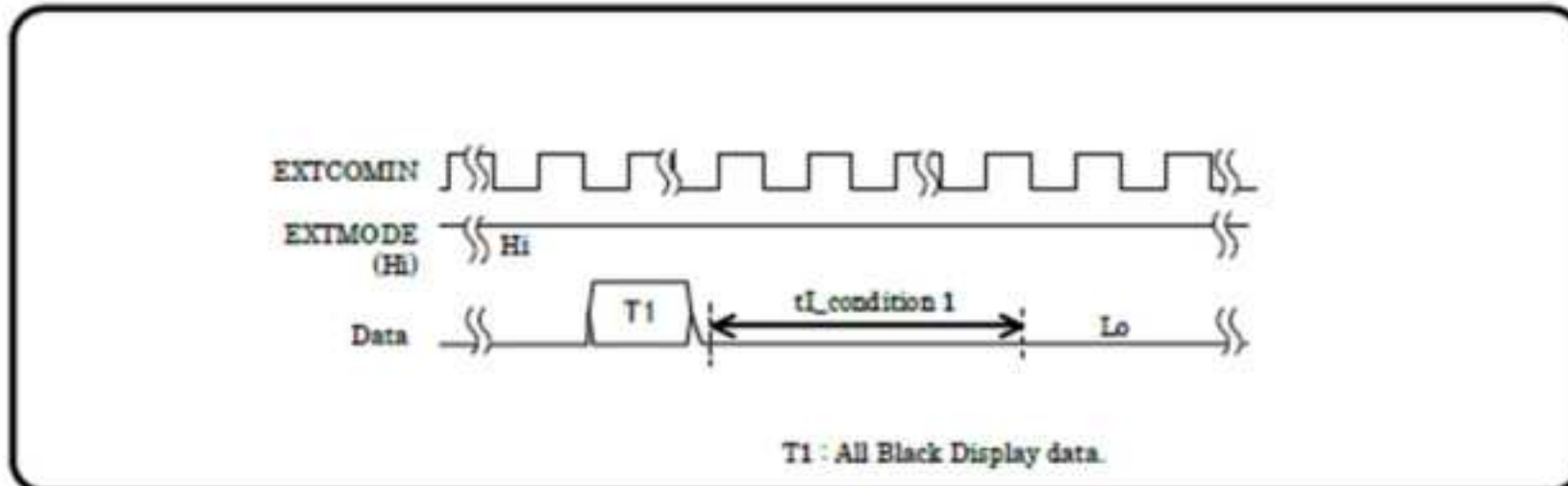


Figure 6-4-1 Current measurement 1

[Note 6-4-2]

Condition 2 : Current measurement period of power supply.

tI_condition 2 :

Measurement time is 1 sec.

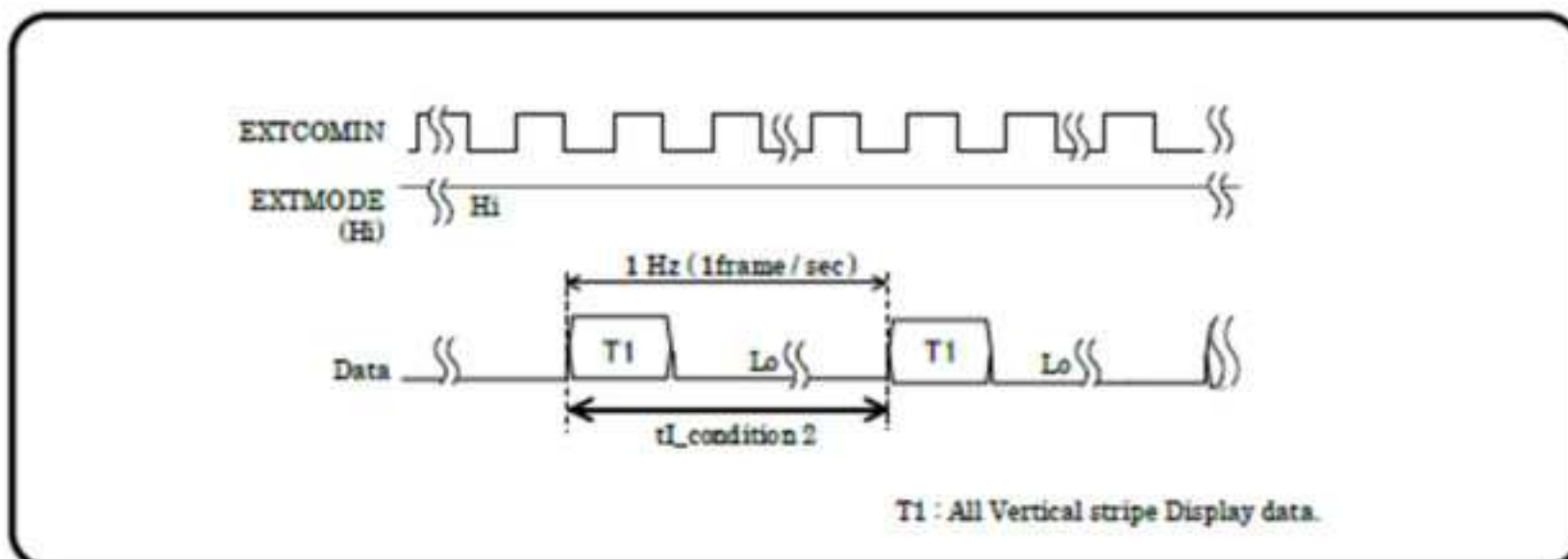


Figure 6-4-2 Current measurement 2

6.5 Input Signal Characteristics

6-5-1)

COM control can be done by serial data or by EXTCOMIN signal.

[General Note 6-5-1]

Please use a frame frequency in the range where there are no problems with the display quality.

[General Note 6-5-2]

LC inversion (COM inversion) :

LC material is needed alternative polarity driving as changing timing which should be constant period.

The conditions as an example (For EXTCOMIN = 60Hz) :

EXTMODE=Hi , SCS=Lo , EXTCOMIN = 60Hz

fEXTCOMIN frequency 60Hz is COM frequency (fCOM) 30Hz.

as shown Figure 6-5-1 (fCOM = 30Hz)

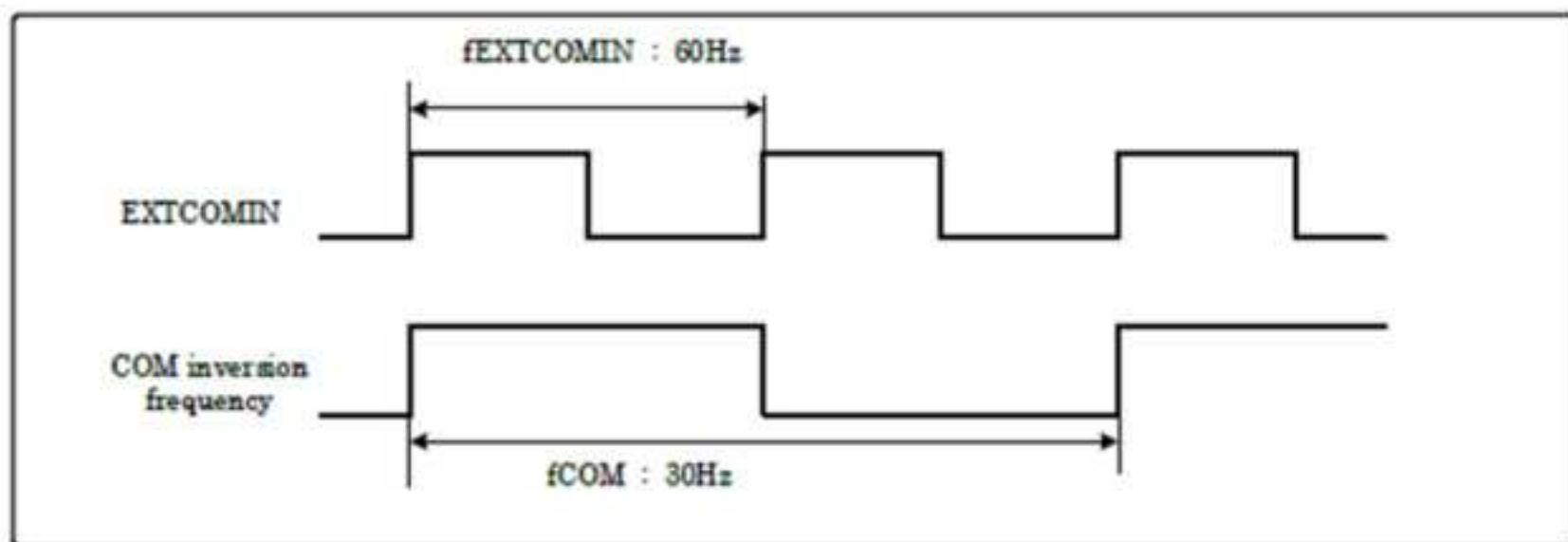


Figure 6-5-1 COM inversion frequency

6-5-2) (When EXTMODE=Lo)

COM driving by the serial comman

For this COM control, the M1 bit must be updated so that the COM cycle (fCOM) is constant regardless of the number of data update lines and update cycle.

For more information, see section 6-6-5).

Table6-5-1 Recommend Operating Conditions and DC Characteristics
 VDDA= +3.0V, VDD= +3.0V GND=0V, Ta=25°C

| Item | Symbol | Min | Typ | Max | Unit | Remark |
|---------------|--------|------|-----|-----|------|---|
| COM Inversion | fV | 57 | — | 66 | Hz | Figure 6-5-1 . Figure 6-6-3 Figure 6-6-5 |
| COM frequency | fCOM | 28.5 | — | 33 | Hz | Figure 6-5-1 . Figure 6-6-3 Figure 6-6-5 |

6-5-3) (When EXTMODE=Hi)

COM driving by the serial command

For more information, see section 6-6-5).

Table6-5-2 Recommend Operating Conditions and DC Characteristics
 VDDA= +3.0V, VDD= +3.0V GND=0V, Ta=25°C

| Item | Symbol | Min | Typ | Max | Unit | Remark |
|---------------|--------|------|-----|-----|------|-----------------------------|
| COM frequency | fCOM | 28.5 | — | 33 | Hz | Figure 6-6-6 , Figure 6-6-7 |

6.6 Input Signal Timing Chart

6-6-1

Data update mode (1 line)

Updates data of only one specified line. (M0= "Hi", M2= "Lo")

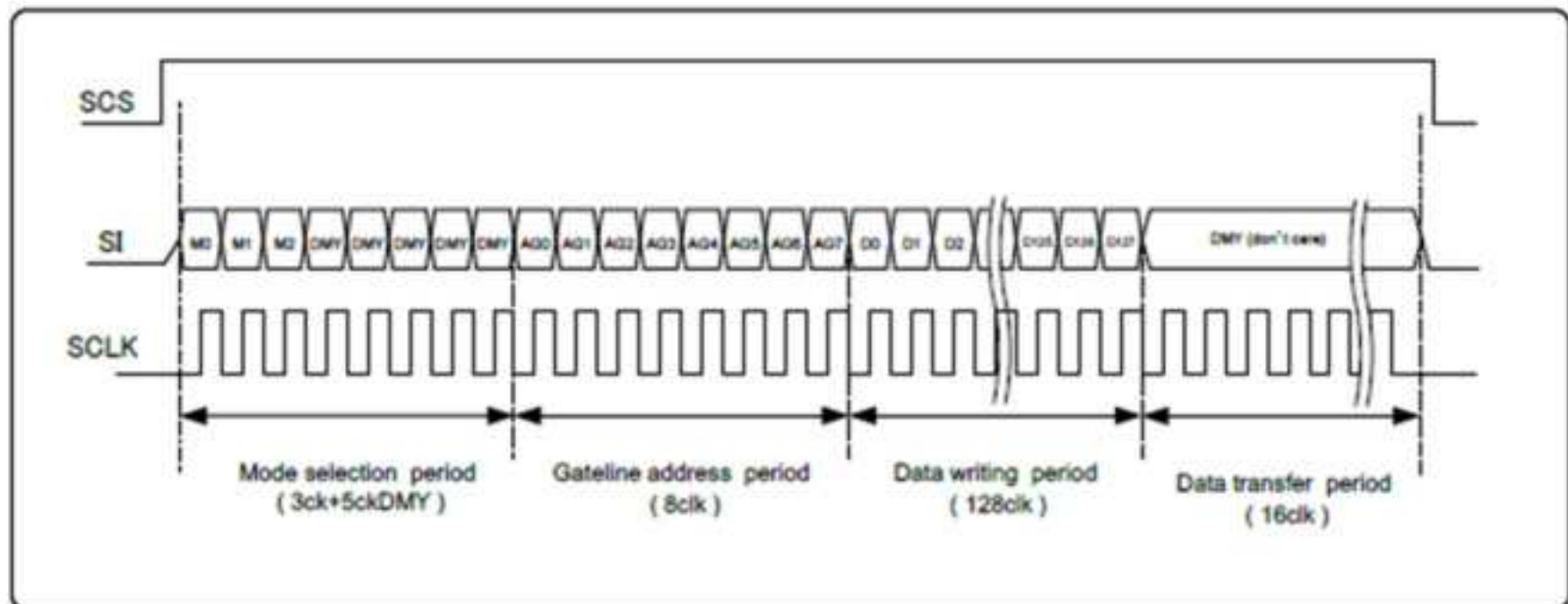


Figure 6-6-1 Data update mode by 1line

M0 : Mode flag.

Set for "Hi" : Data update mode (Memory internal data update)
 Set for "Lo" : Hold mode (maintain memory internal data)

M1 : Frame inversion flag.

When "Hi", outputs VCOM = "Hi", and when "Lo", outputs VCOM = "Lo".
 When EXTMODE = "Hi", it can be "Hi" or "Lo".

M2 : All clear flag.

Refer to 6-6-4) All Clear Mode to execute clear.

DUMMY DATA :

Dummy data : It can be "Hi" or "Lo" ("Lo" is recommended)

D0-D127 :

Writing Image data (Horizontal Line data)

Hi : (White)
 Lo : (Black)

| |
|--|
| ※ Data write period Data is being stored in 1 st latch block of binary driver on panel. |
| ※ Data transfer period Data written in 1 st latch is being transferred (written) to pixel internal memory circuit. |

For gate line address setting, refer to 6-7) Input Signal and Display.

Input data continuously

M1 : Frame inversion flag is enabled when EXTMODE= "Lo".

When SCS becomes "Lo", M0 and M2 are cleared.

6-6-2

Data Update Mode (Multiple Lines)

Updates arbitrary multiple lines data. (M0= "Hi", M2= "Lo")

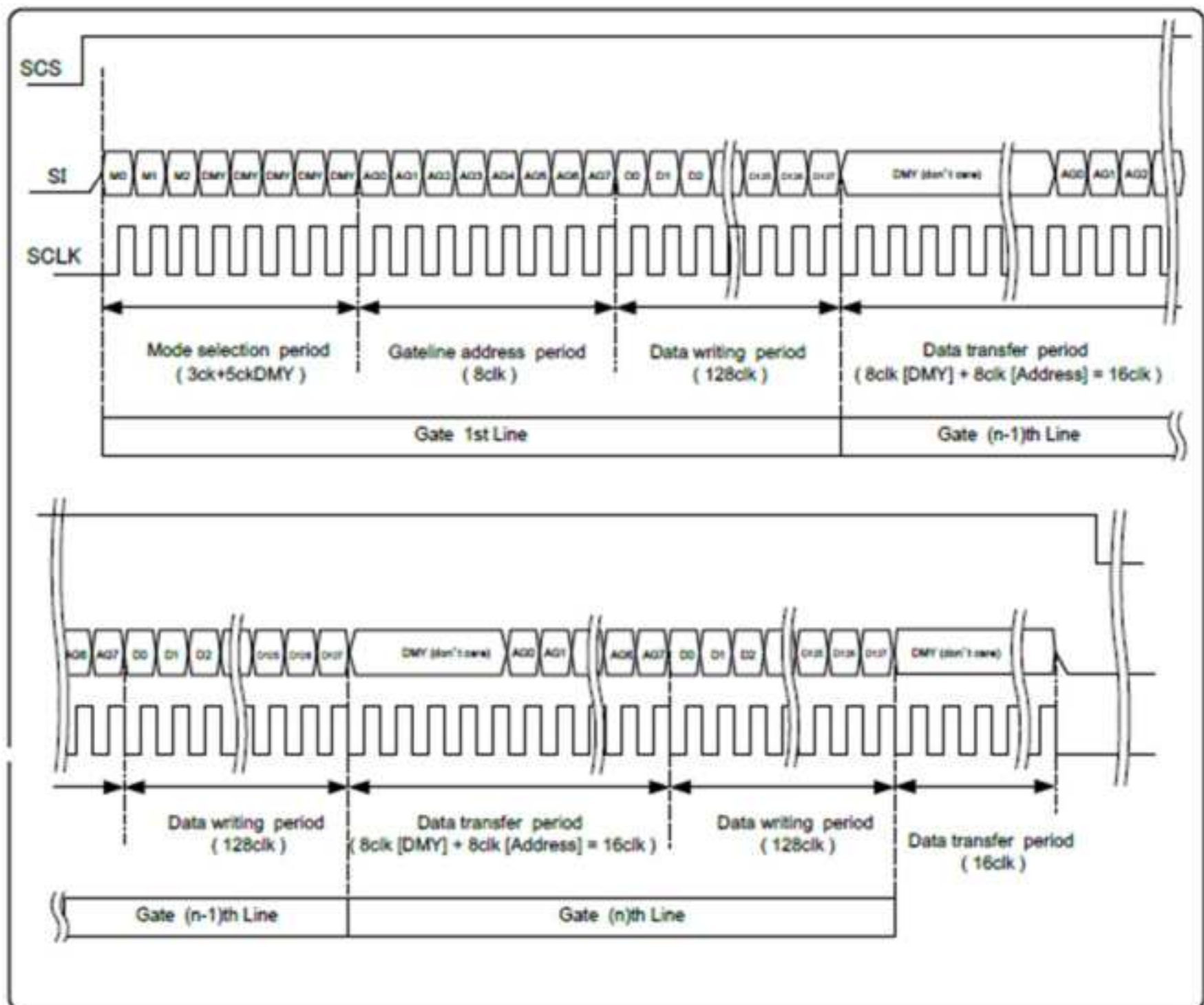


Figure 6-6-2 Data update mode by Multiple Lines

M0 : Mode flag.

Set for "Hi" : Data update mode (Memory internal data update)
 Set for "Lo" : Hold mode (maintain memory internal data).

M1 : Frame inversion flag.

When "Hi", outputs VCOM = "Hi", and when "Lo", outputs VCOM = "Lo".
 When EXTMODE = "Hi", it can be "Hi" or "Lo".

M2 : All clear flag.

Refer to 6-6-4) All Clear Mode to execute clear.

DUMMY DATA :

Dummy data : It can be "Hi" or "Lo" ("Lo" is recommended)

D0-D127 :

Writing Image data (Horizontal Line data)

Hi : (White)

Lo : (Black)

※ Data write period

Data is being stored in 1st latch block of binary driver on panel.

※ Data transfer period

For example, during GL2nd line data transfer period, GL 2nd line address is latched and GL1st line data is transferred from 1st latch to pixel internal memory circuit at the same time.

For gate line address setting, refer to 6-7) Input Signal and Display.

Input data continuously.

M1 : Frame inversion flag is enabled when EXTMODE= "Lo".

When SCS becomes "Lo", M0 and M2 are cleared.

6-6-3

Hold Mode

Maintains memory internal data (maintains current display). (M0= "Lo", M2= "Lo")

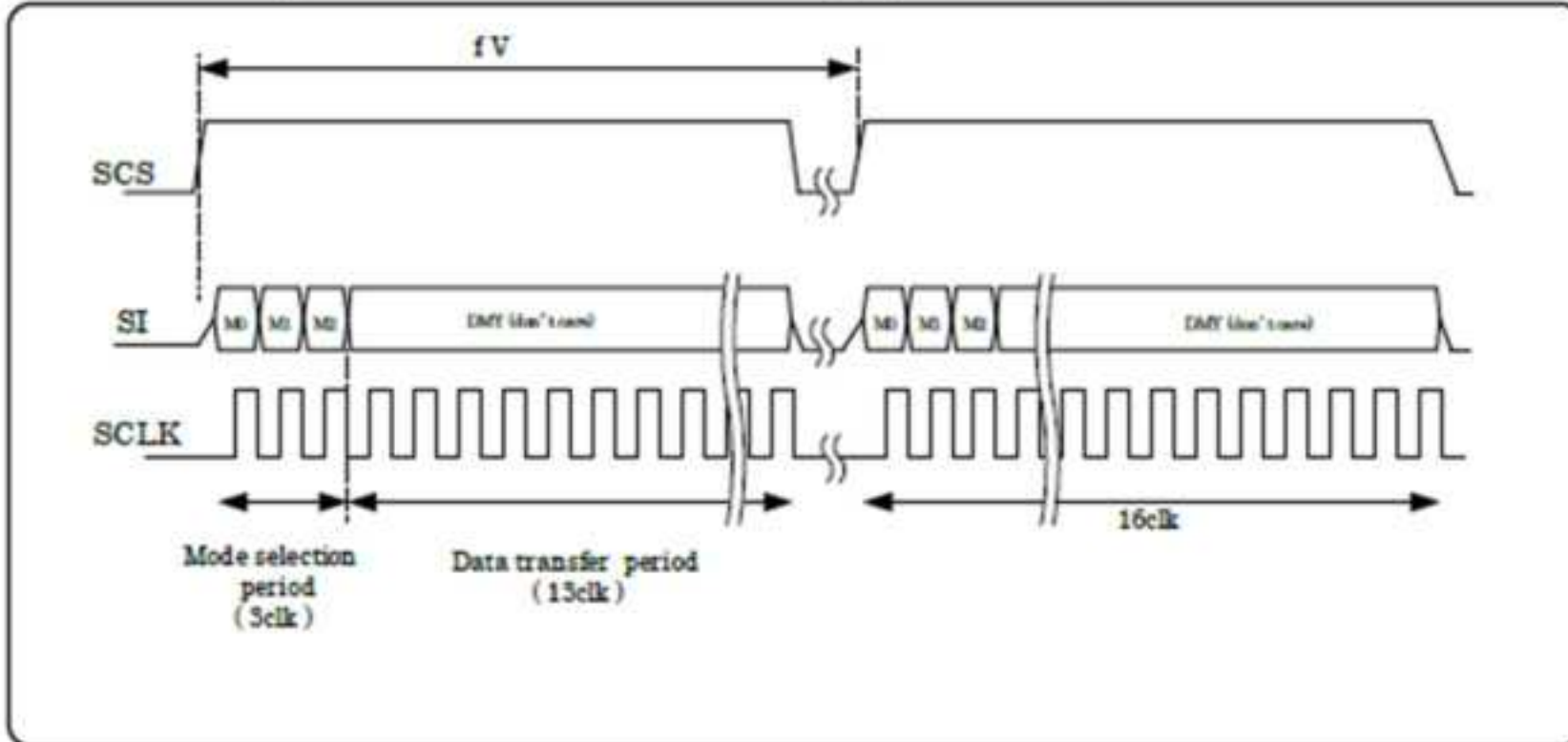


Figure 6-6-3 HOLD mode

M0 : Mode flag.

Set for "Hi" : Data update mode (Memory internal data update)

Set for "Lo" : Hold mode (maintain memory internal data).

M1 : Frame inversion flag.

When "Hi", outputs VCOM = "Hi", and when "Lo", outputs VCOM = "Lo".

When EXTMODE = "Hi", it can be "Hi" or "Lo".

M2 : All clear flag.

Refer to 6-6-4) All Clear Mode to execute clear.

DUMMY DATA :

Dummy data : It can be "Hi" or "Lo" ("Lo" is recommended)

M1 : Frame inversion flag is enabled when EXTMODE= "Lo".

When SCS becomes "Lo", M0 and M2 are cleared.

6-6-4

All Clear Mode

Clears memory internal data and writes white. (M0= "Lo", M2= "Hi")

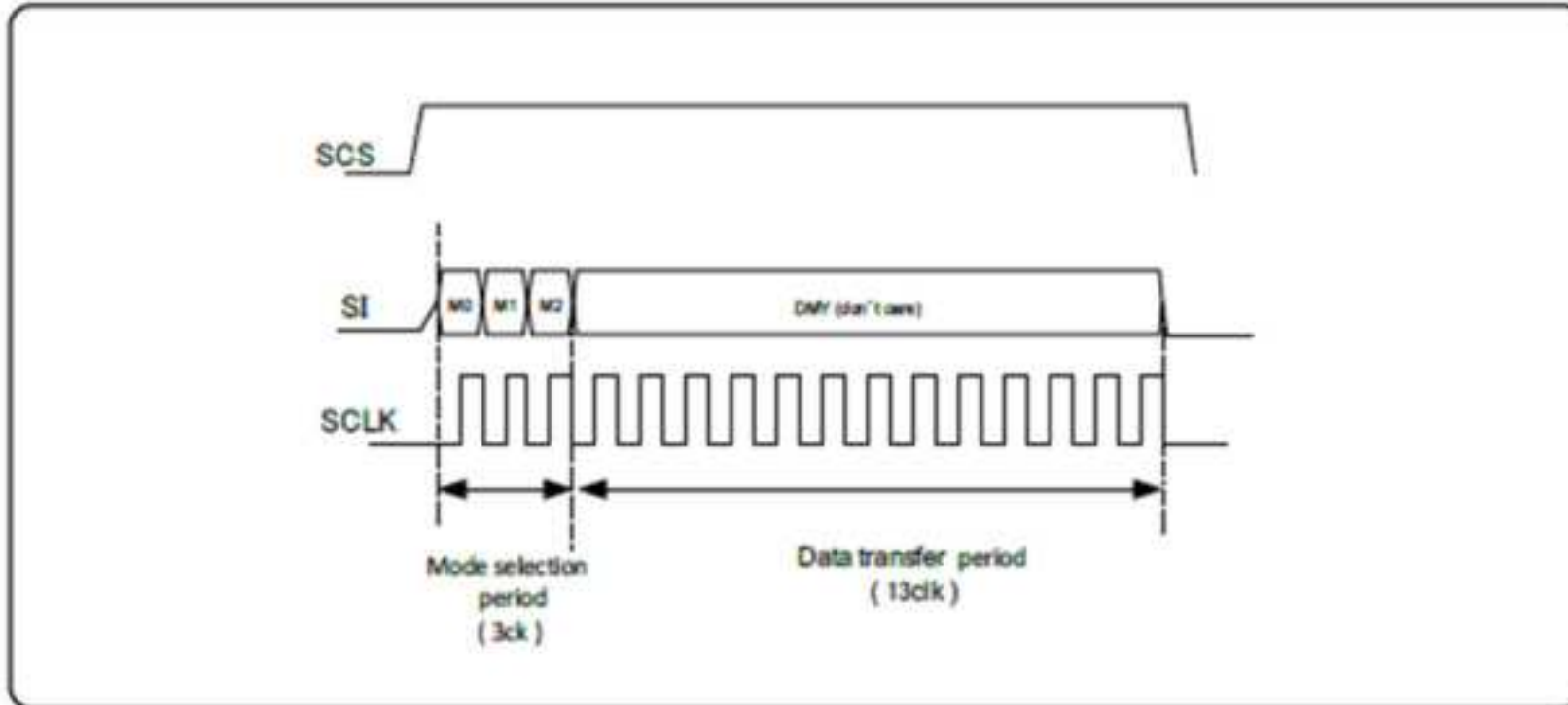


Figure 6-6-4 All Clear mode

M0 : Mode flag.

Set it "Lo".

M1 : Frame inversion flag.

When "Hi", outputs VCOM = "Hi", and when "Lo", outputs VCOM = "Lo".
When EXTMODE = "Hi", it can be "Hi" or "Lo".

M2 : All clear flag.

Set it "Hi"

DUMMY DATA :

Dummy data : It can be "Hi" or "Lo" ("Lo" is recommended)

M1 : Frame inversion flag is enabled when EXTMODE= "Lo".

When SCS becomes "Lo", M0 and M2 are cleared.

6-6-5 COM Inversion

There are two types of inputs, COM signal serial input (EXTMODE= "Lo") and external COM signal input (EXTMODE= "Hi").

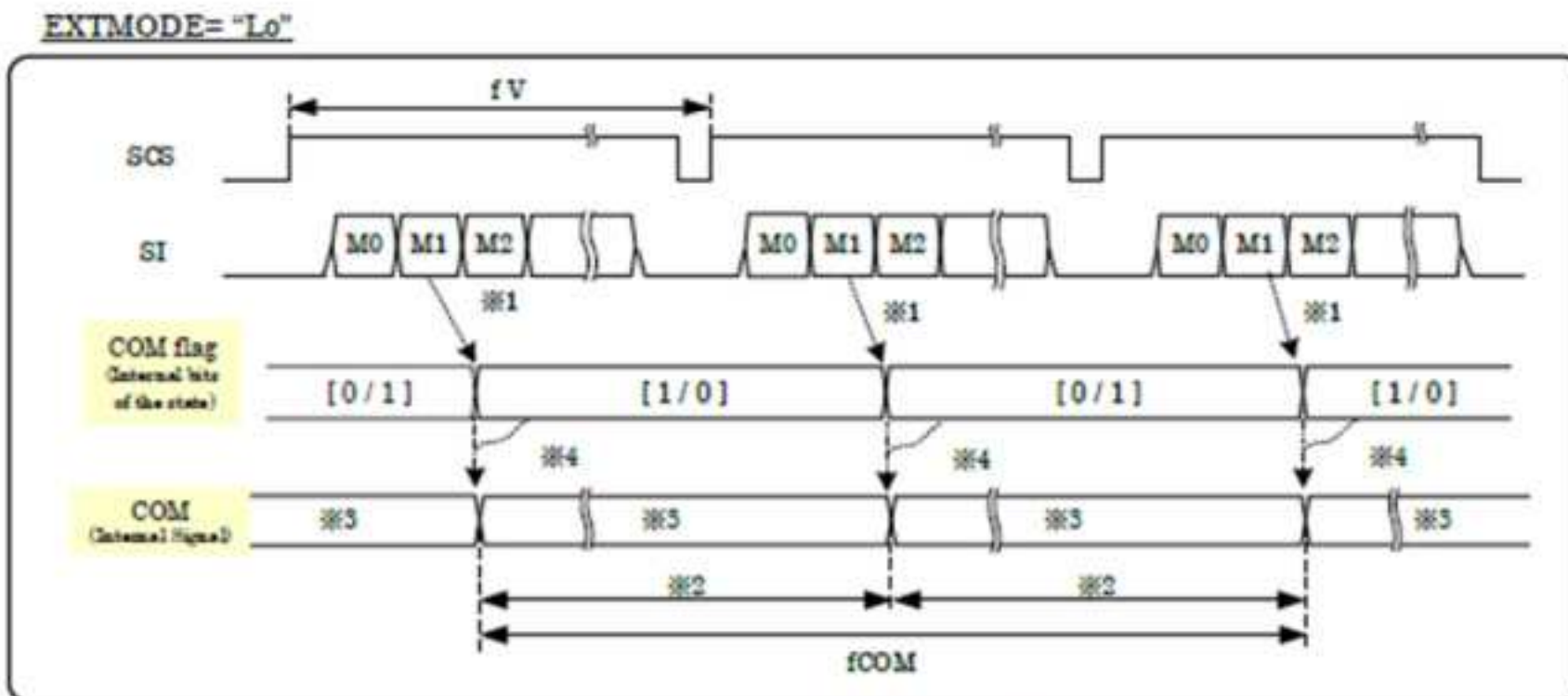


Figure 6-6-5 COM Inversion (EXTMODE= Lo)

M1: COM polarity inversion flag:

If M1 is "Hi" then VCOM= "Hi" is output.
 If M1 is "Lo" then VCOM= "Lo" is output.

COM inversion has been changed by M1 flag statement.

The periods of plus polarity and minus polarity should be same length as much as possible.

If M1 is 1 (Hi), COM is 1 (Hi)

It is reflected according to the COM flag bit at this timing.

Table 6-6-1 COM state 1

| | | COM state (COM flag bit) |
|----------|---|--------------------------|
| M1 (bit) | 1 | 1 |
| | 0 | 0 |

It changes according to the M1 bit regardless of the state before the change.

EXTMODE="Hi" (COM inversion timing has two conditions)

① EXTCOMIN input during high period of the SCS signal

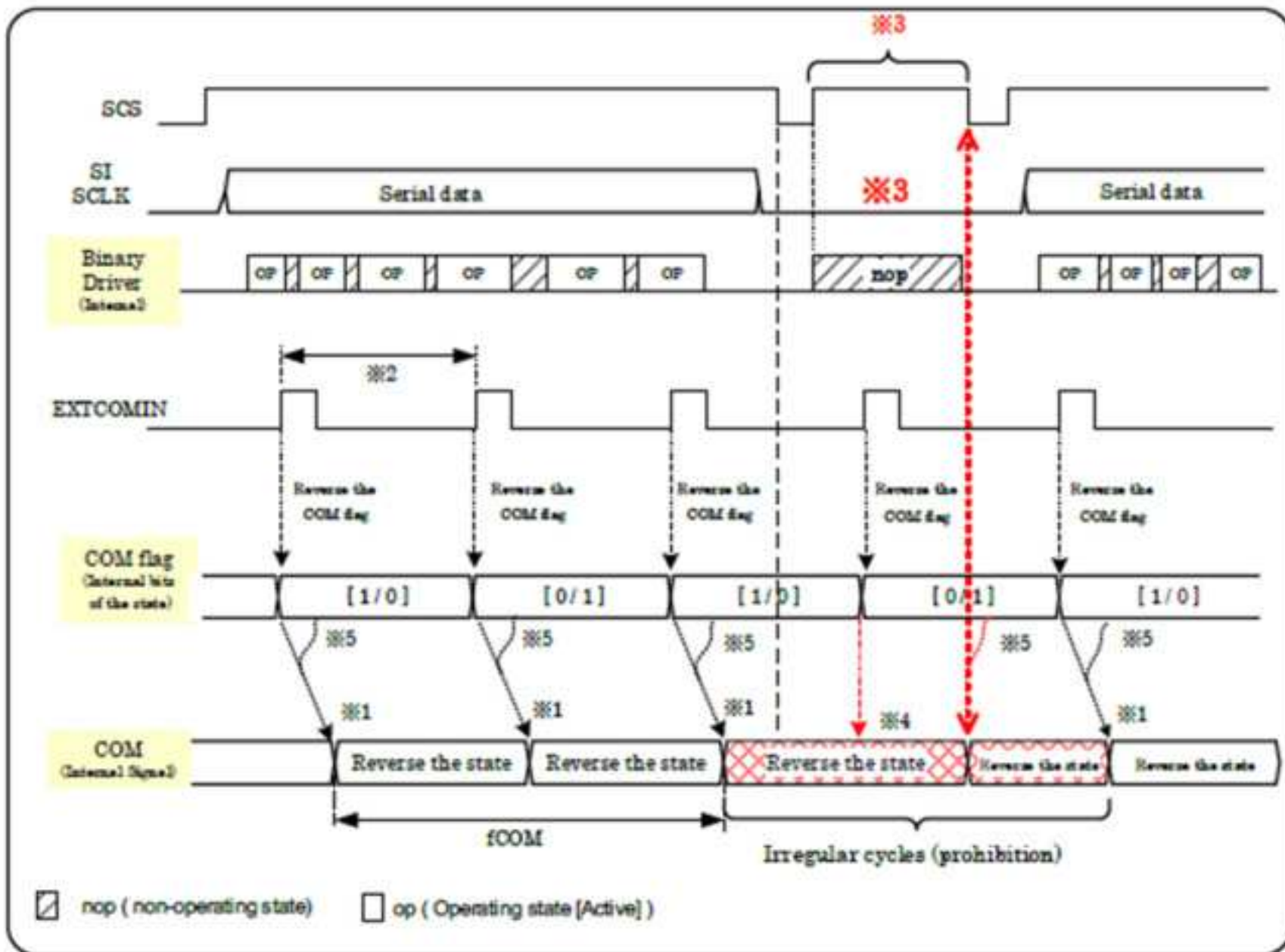


Figure 6-6-6 COM Inversion (EXTMODE=Hi) 1

[Note 6-6-1]

Inversion at EXTCOMIN rising edge.

Make "COM" reversal depending.


The period of EXTCOMIN should be constant and the period of COM inversion should be constant depending on EXTCOMIN. (with Send a serial data or making the period of "SCS= Low")

The signal timing which isn't good.
 Do not set SCS to Hi (1) if data is not to be transmitted

COM inversion does not occur. (State is preserved)

COM Flag-bit and COM inversion on the rising edge of EXTCOMIN.

Table 6-6-2 COM state 2 (EXTMODE=Hi and SCS=Hi)

| | | EXTCOMIN | COM state (COM flag state) [note 6-6-1] | |
|--------|----|---|--|------------------------|
| | | | State before inversion | Status after inversion |
| SCS=Hi | Hi |  | 1 | 0 |
| | | | 0 | 1 |

② EXTCOMIN input during low period of the SCS signal

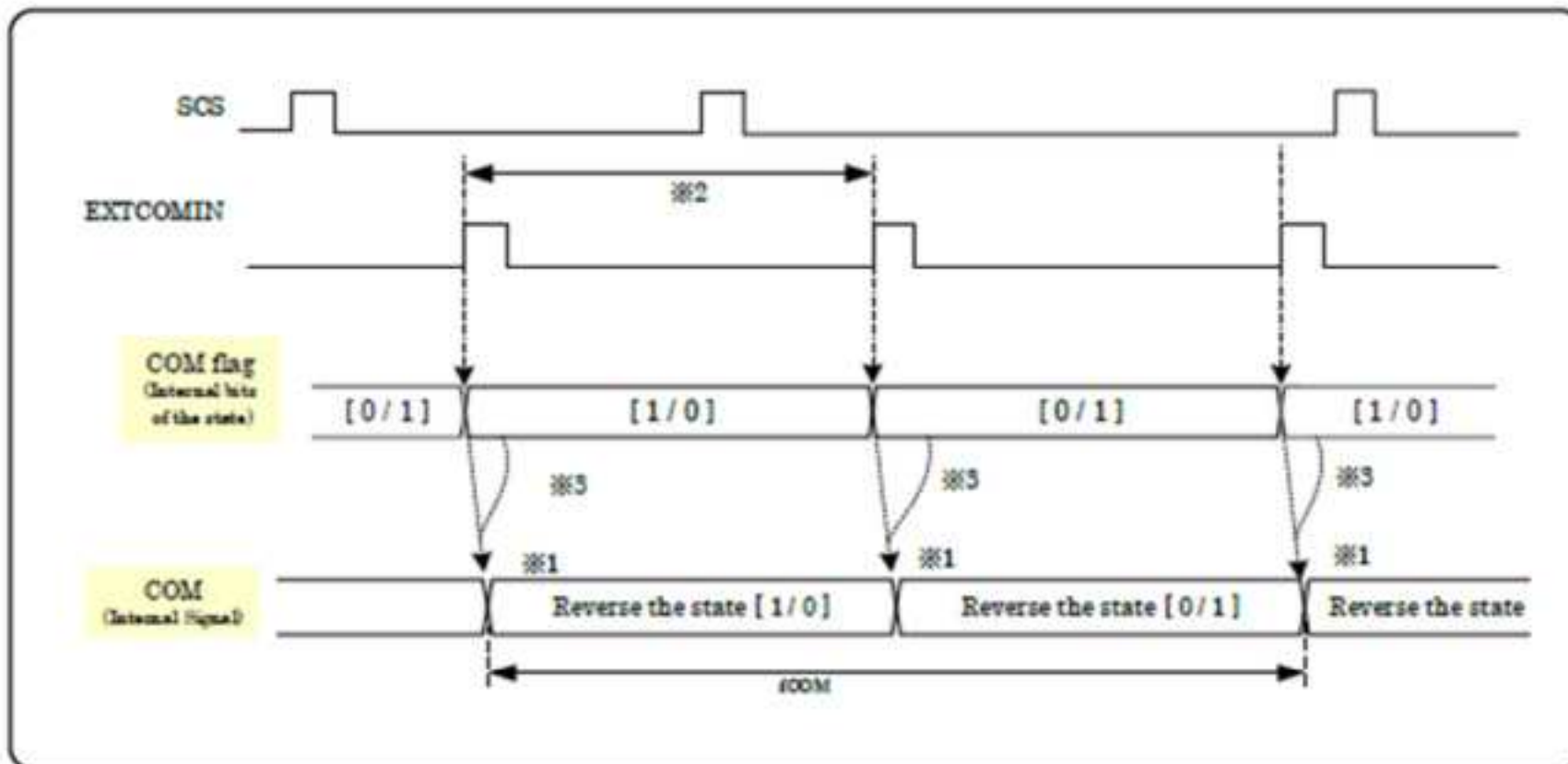


Figure 6-6-7 COM Inversion (EXTMODE=Hi) 2

[Note 6-6-2]

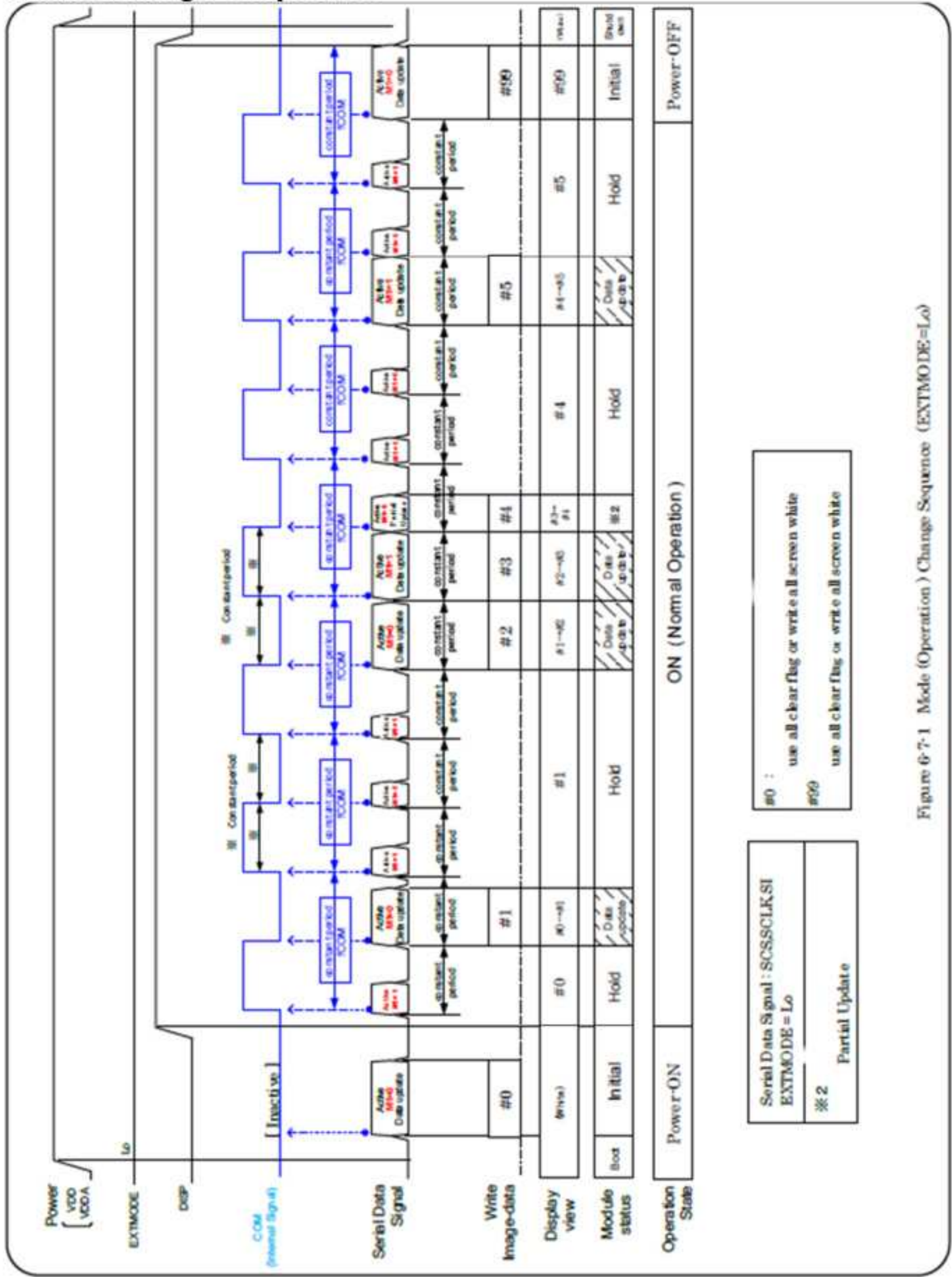
Inversion at EXTCOMIN rising edge.

- ※ 1 : COM inversion polarity has been set by rising edge of EXTCOMIN.
- ※ 2 : The period of EXTCOMIN should be constant.
- ※ 3 : COM Flag-bit and COM inversion on the rising edge of EXTCOMIN.

Table 6-6-3 COM state 3 (EXTMODE=Hi and SCS=Lo)

| | | COM state (COM flag state) [note 6-6-2] | | |
|--------|----|--|------------------------|---|
| | | State before inversion | Status after inversion | |
| SCS=Lo | Hi | | 1 | 0 |
| | | | 0 | 1 |

6.7 Mode Change Sequence



#0 : use all clear flag or write all screen white
 #09 : use all clear flag or write all screen white

Serial Data Signal : SCSSCLKSI
 EXTMODE = Lo
 ※2 Partial Update

Figure 6-7-1 Mode (Operation) Change Sequence (EXTMODE=Lo)

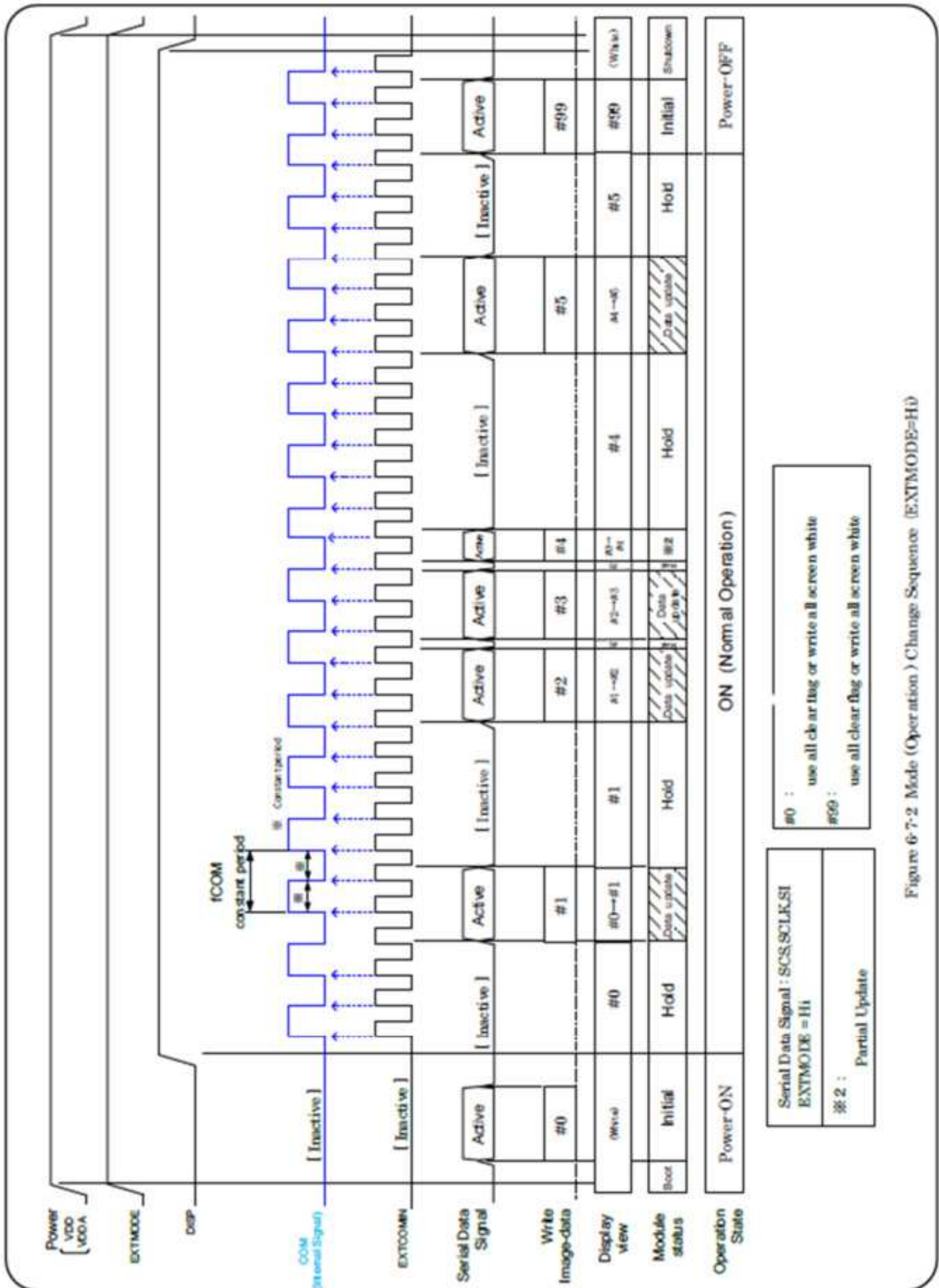


Figure 6-7-2 Mode (Operation) Change Sequence (EXTMODE=Hi)

Serial Data Signal : SCS,SCLK,SI
 EXTMODE = Hi
 ※ 2 : Partial Update

※ 0 : use all clear flag or write all screen white
 ※ 99 : use all clear flag or write all screen white

6.8 Input Signal and Display, Gate Address (Line), Settings

Table 6-8-1

| GL | A00 | A01 | A02 | A03 | A04 | A05 | A06 | A07 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 4 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 5 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 6 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 7 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 8 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 10 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 11 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 12 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 13 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 14 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 16 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 17 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 18 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 19 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 20 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 21 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 22 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 23 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 24 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 25 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 26 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 27 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 28 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 29 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 30 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 31 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 32 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 33 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 34 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 35 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 36 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 37 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 38 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 39 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 40 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 41 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 42 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 43 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 44 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 45 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 46 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 47 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 48 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 49 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 50 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |

Gate line address setting

| GL | A00 | A01 | A02 | A03 | A04 | A05 | A06 | A07 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 51 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 52 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 53 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 54 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 55 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 56 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 57 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 58 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 59 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 60 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 61 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 62 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 63 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 64 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 65 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 66 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 67 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 68 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 69 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 70 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 71 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 72 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 73 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 74 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 75 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 76 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 77 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 78 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 79 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 80 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 81 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 82 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 83 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 84 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 85 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 86 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 87 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 88 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 89 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 90 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 91 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 92 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 93 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 94 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 95 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 96 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 97 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 98 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 99 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 100 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |

GL: Gate address line

| GL | A00 | A01 | A02 | A03 | A04 | A05 | A06 | A07 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 101 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 102 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 103 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 104 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 105 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 106 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 107 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 108 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 109 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 110 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 111 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 112 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 113 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 114 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 115 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 116 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 117 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 118 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 119 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 120 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 121 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 122 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 123 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 124 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 125 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 126 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 127 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 128 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

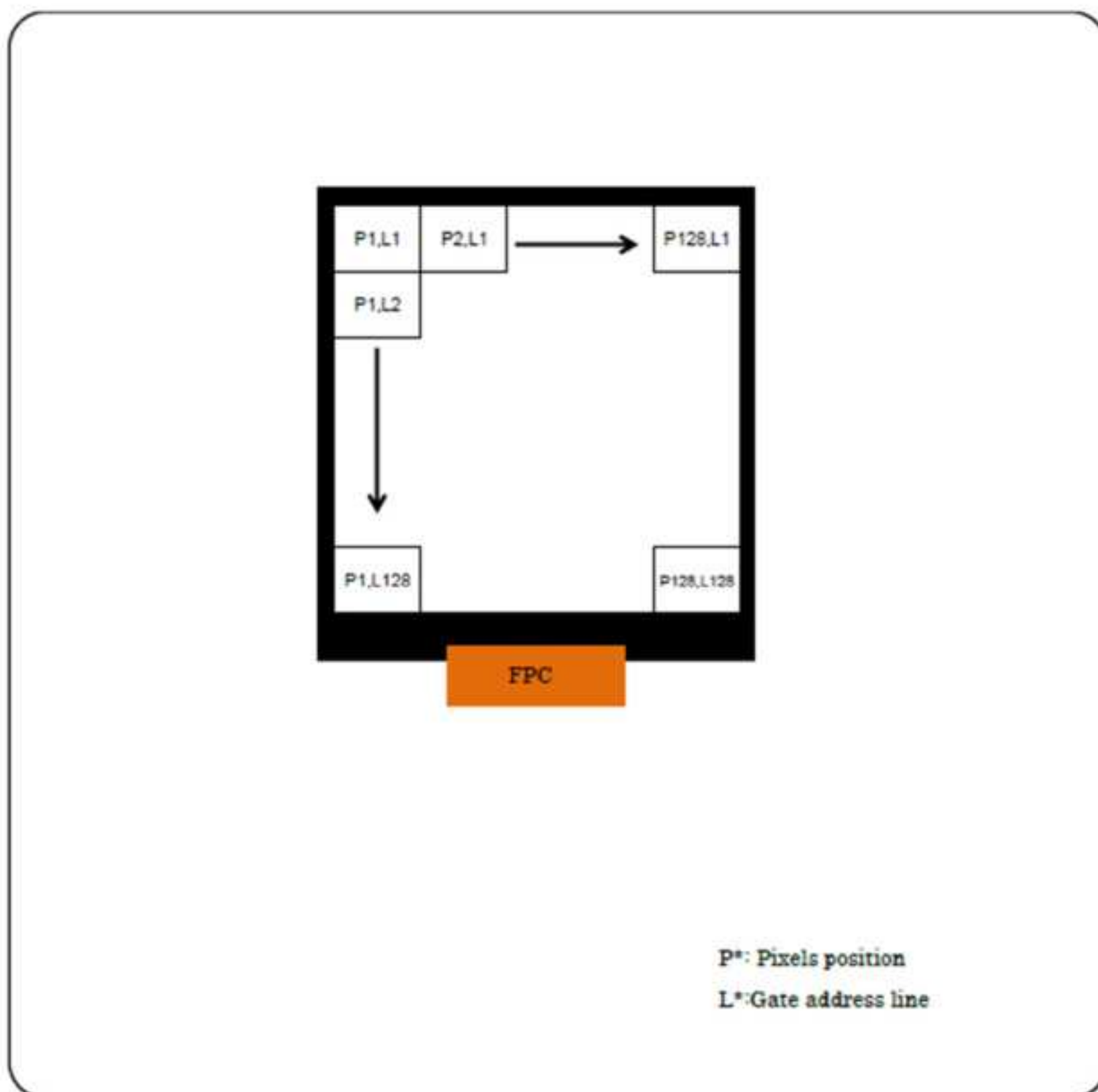


Figure 6-8-1 Data position

7 Optical Specification

7.1 Optical Specification (Reflective Mode)

Table 7-1

Optical specification (Reflective Mode)

VDD=VDDA= +3.0V , Ta=25°C

| Item | Symbol | Min. | Typ. | Max. | unit | Remark | |
|-----------------------------|------------|-------------|------|------|------|-----------------------|----------------------|
| Viewing angle Range CR≥2 | Horizontal | $\theta 21$ | 40 | 60 | - | *(degree) Note 7-1 | |
| | | $\theta 22$ | 40 | 60 | - | | |
| | Vertical | $\theta 11$ | 40 | 60 | - | | |
| | | $\theta 12$ | 40 | 60 | - | | |
| Contrast ratio | CR | 14 | 20 | - | | Note 7-2 Note 7-3 | |
| Reflectivity ratio | R | 12 | 16 | - | % | Note 7-3 | |
| Response Time | Rise | τr | - | 10 | 20 | ms | Note 7-3 Note 7-4 |
| | Fall | τd | - | 20 | 40 | ms | |
| Panel Chromaticity | White | x | - | 0.31 | - | | Note 7-3 |
| | | y | - | 0.33 | - | | |

[Note 7-1]

Defintion of Viewing Angle

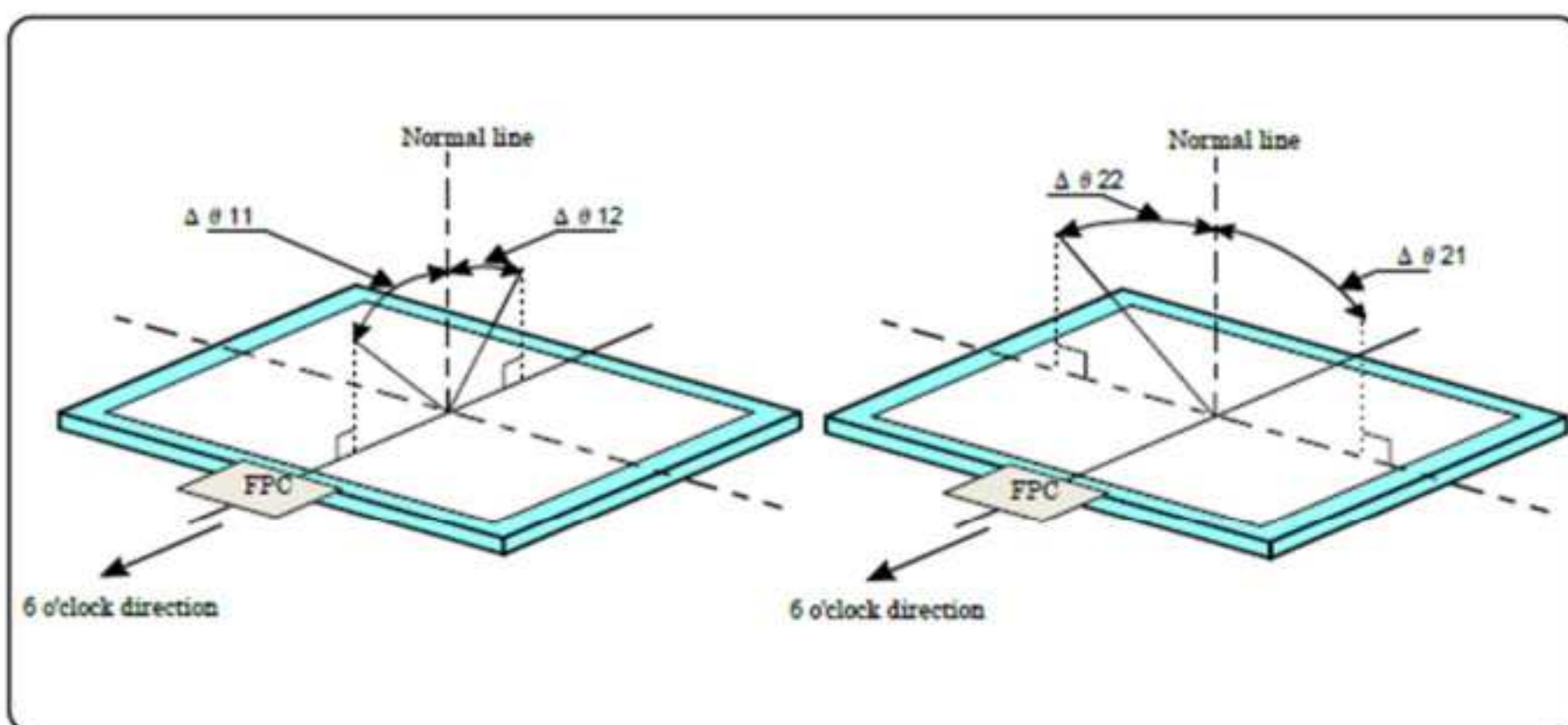


Figure 7-1 Defintion of Viewing Angle

7.2 Optical Specification Transmissive Mode

Table 7-2 Optical specification (+Back light Mode)

VDD=VDDA= +3.0V , Ta=25°C

| Item | Symbol | Min. | Typ. | Max. | unit | Remark |
|--------------------|--------|------|------|------|-------|----------|
| Panel Chromaticity | x | - | 0.30 | - | | Note 7-5 |
| | y | - | 0.31 | - | | |
| | L | 20 | 30 | - | cd/m2 | |

[Note 7-2]

Defintion of Contrast Ratio

•The contrast ratio is defined as the following.

| |
|---|
| $\text{Contrast ratio(CR)} = \frac{\text{Reflection intensity in white display}}{\text{Reflection intensity in black display}}$ |
|---|

[Note 7-3]

Optical characteristics measurement equipment.

• Figure 7-2 is for contrast ratio, reflectivity ratio, and panel chromaticity measurement, and Figure 7-3 is for response time measurement. Both are to be conducted in a dark or room equipment to a dark room

Measurement equipment
(CM700d)

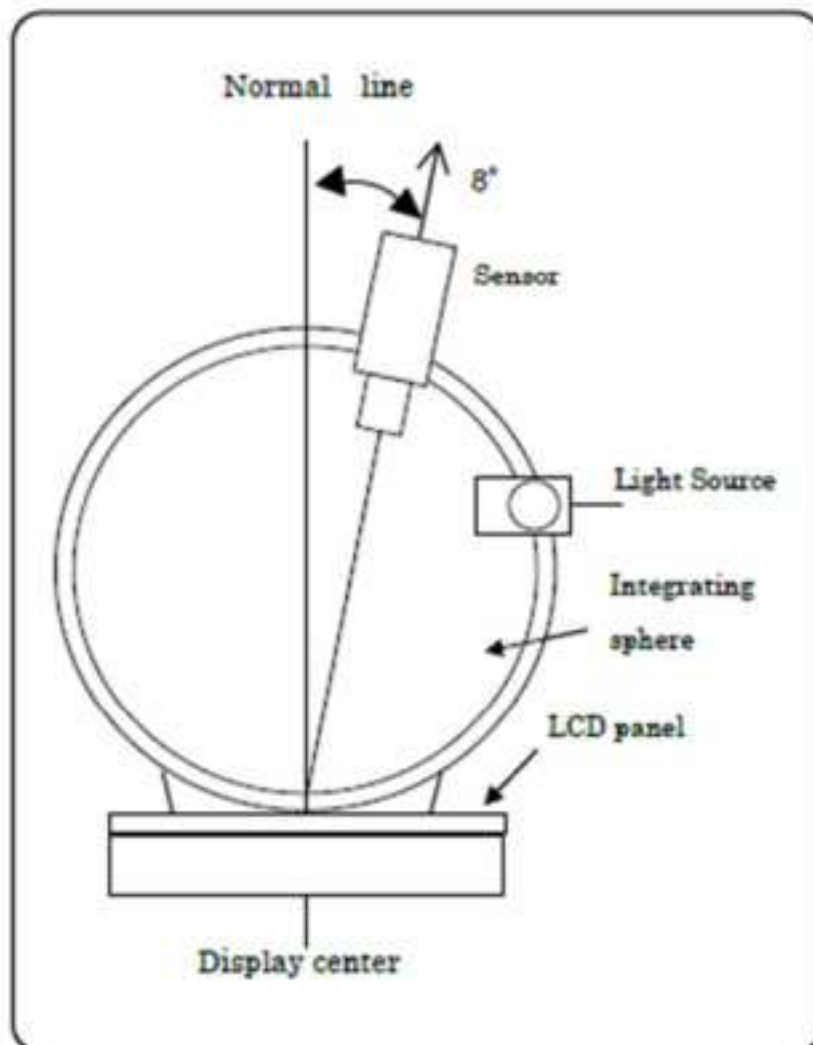


Figure 7-2 Contrast ratio, Reflection ratio,

Measurement equipment
(LCD-5200)

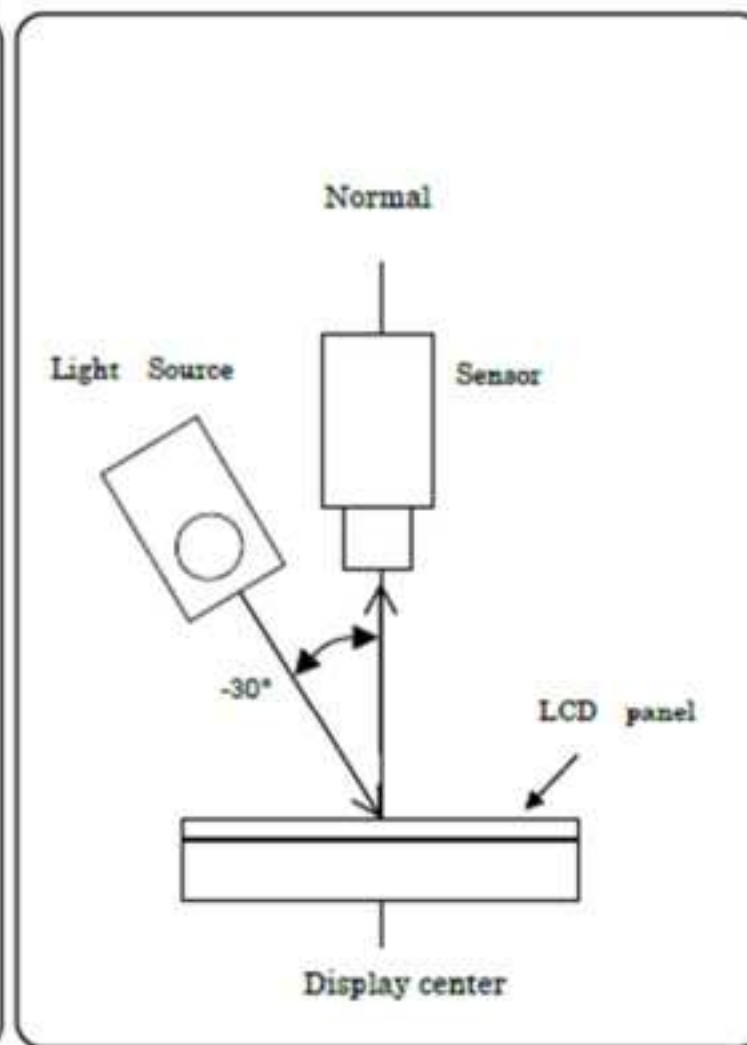


Figure 7-3 Response time

[Note 7-4]

Response time (Change in reflection ratio)

• It's defined by the time change of optical receiver output when signal is input to display white or black

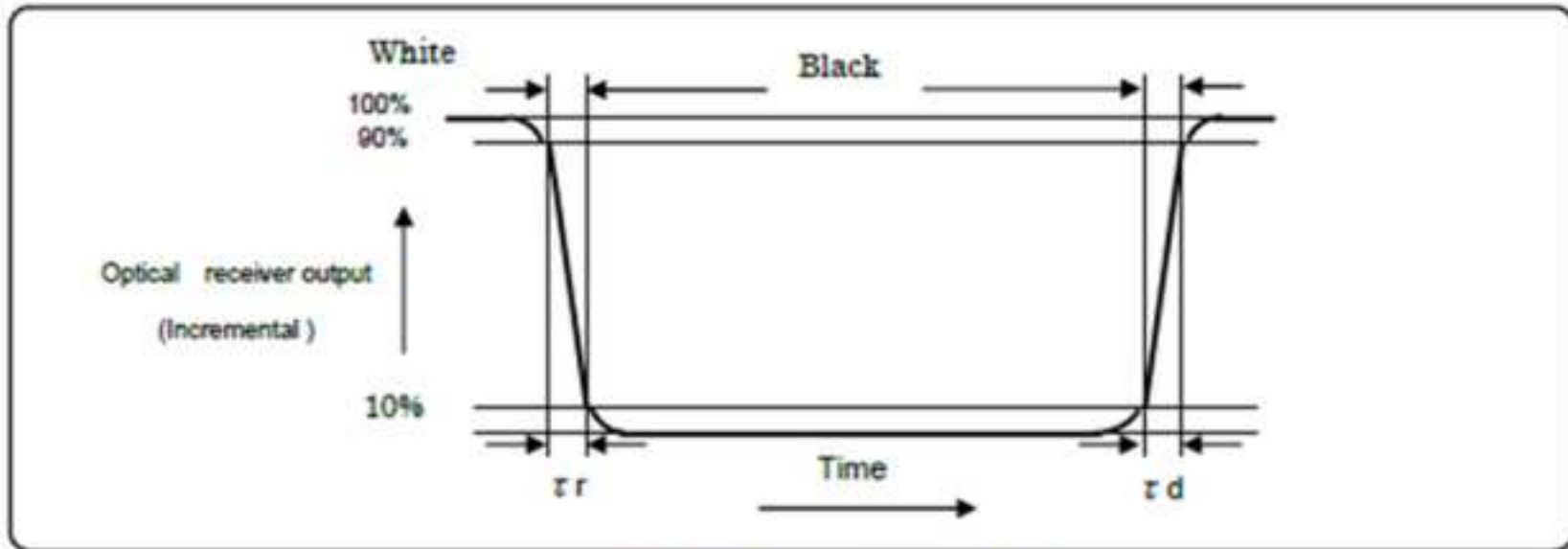


Figure 7-4 Response time

[Note 7-5]

Measurement equipment (Transmissive mode)

The measuring method of the optical characteristics (Transmissive mode) is shown by the following figure. A measurement device is TOPCON luminance meter SR-3 UL1R.

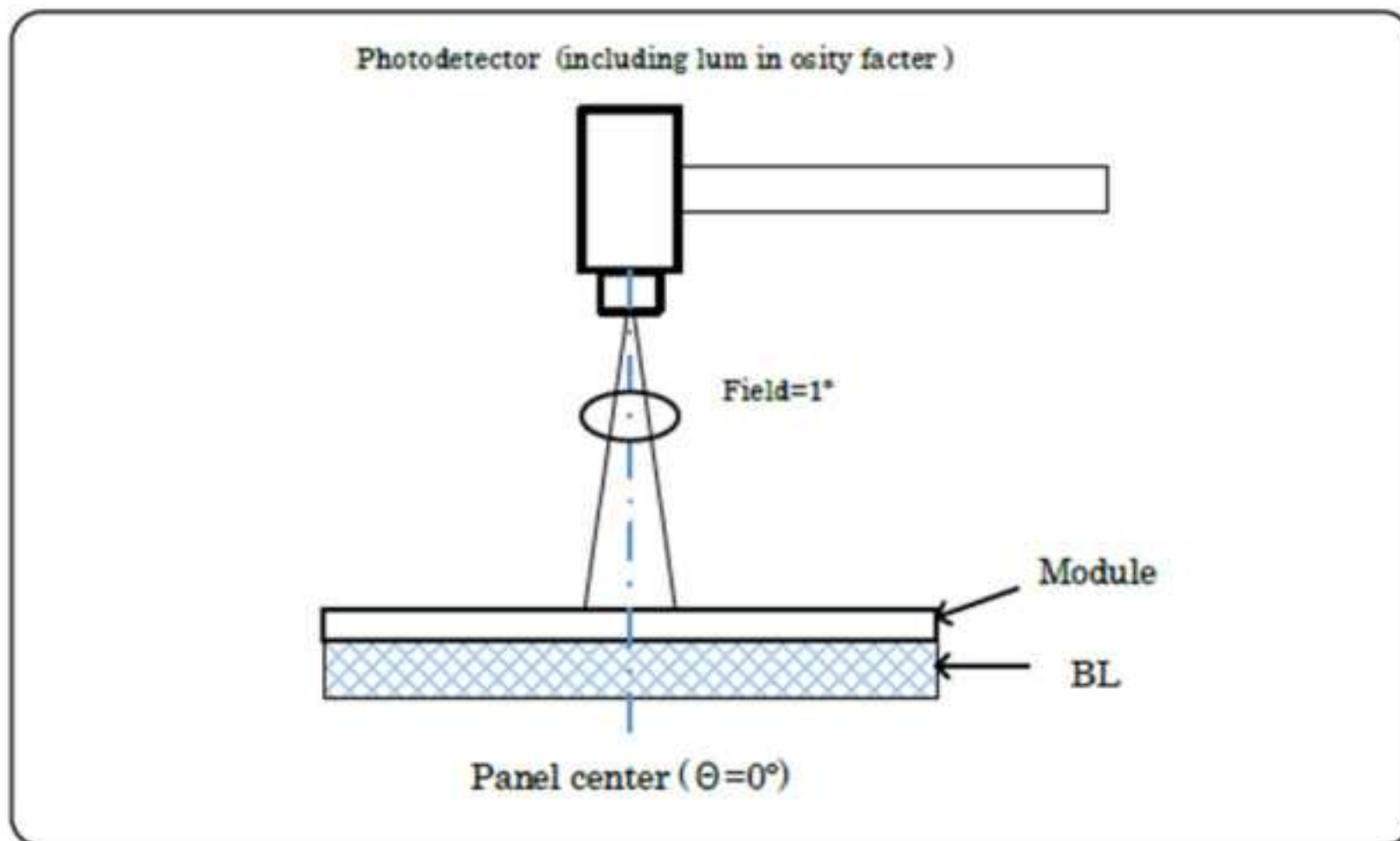
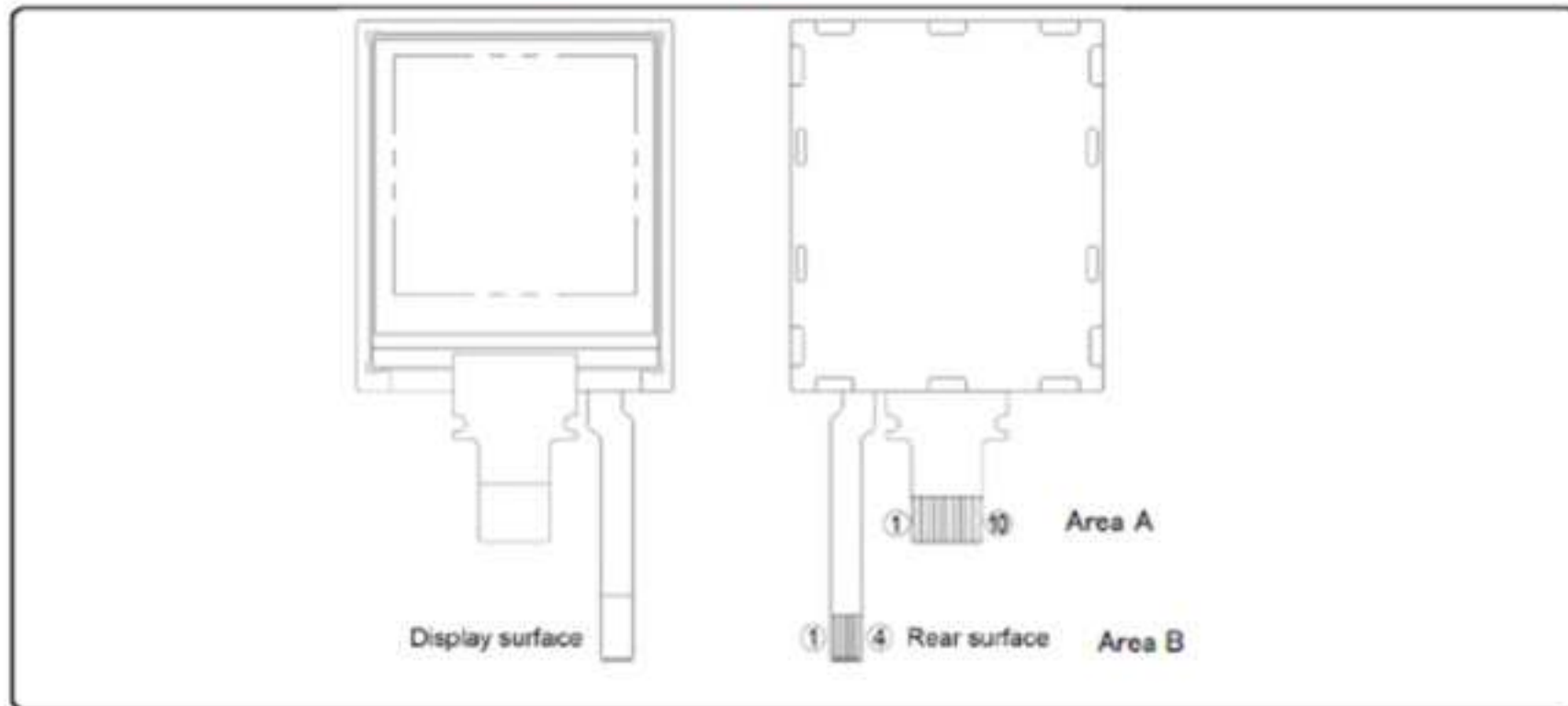


Figure 7-5 Measuring setup for Luminance

8 Pin Assignment

8.1 Pin Assignment

The outline dimensions are shown in Figure 14-1



| No. | Symbol |
|-----|----------|
| 1 | SCLK |
| 2 | SI |
| 3 | SCS |
| 4 | EXTCOMIN |
| 5 | DISP |
| 6 | VDDA |
| 7 | VDD |
| 8 | EXTMODE |
| 9 | VSS |
| 10 | VSSA |

Table 8-1-1 TFT LCD panel terminal

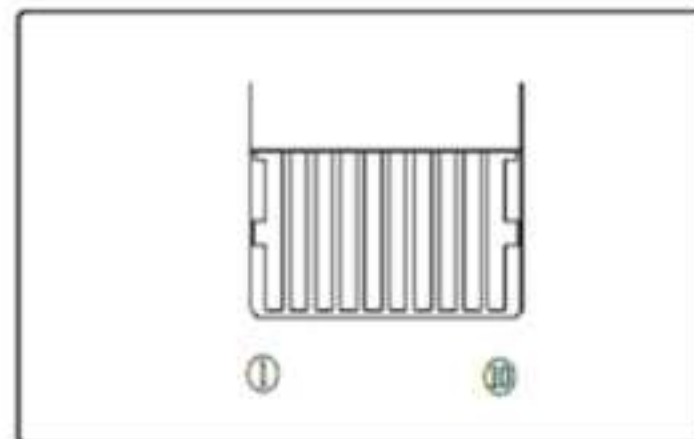


Figure 8-1-2 Pin Assignment 2 (Area A)

| No. | Symbol | Description |
|-----|--------|-----------------------------------|
| 1 | A | Power for LED backlight (Anode) |
| 2 | K | Power for LED backlight (Cathode) |
| 3 | K | Power for LED backlight (Cathode) |
| 4 | A | Power for LED backlight (Anode) |

Table 8-1-3 Backlight terminal

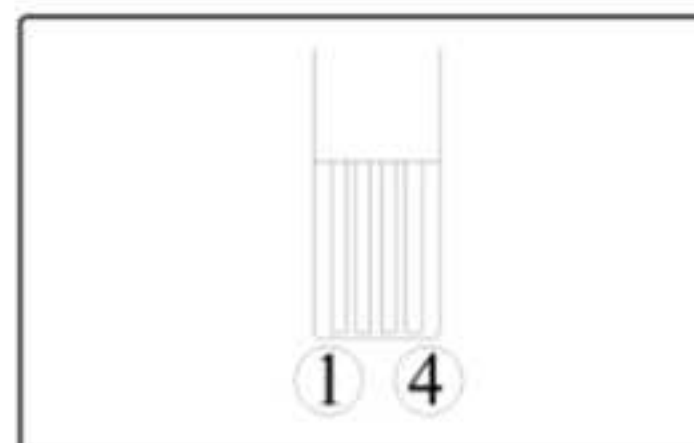


Figure 8-1-4 Pin Assignment 2 (Area B)

8.2 FPC Bending Specification

8-2) FPC

FPC Bend Specification

Table 8-2-1 Recommended Connector

| Product manufacturer | Series | Part number | Contact |
|----------------------|---------|-------------------|------------------|
| Panasonic | Y5B | AYF531035 | Bottom and Upper |
| HRS | FH34SRJ | FH34SRJ-10S-0.5SH | Bottom and Upper |
| | FH28 | FH28-10S-0.5SH | Bottom |
| Molex | 503480 | 503480-1000 | Bottom and Upper |

When bending FPC, bend where specified in Condition (1) and the bend R should be more than R specified in Condition (2). FPC is not to contact glass edge, and there should be no stress to connective area between panel and FPC.

Condition (1) FPC bend recommended area: 0.8 mm – 6.0 mm from glass edge.

Condition (2) Minimum bend R: Inner diameter R 0.45 mm



Figure 8-2-1 FPC Bend Specification

[Note 8-2-1]

Do not bend to the front polarizer film side.

[Note 8-2-2]

Bend frequency: 3 times or less (Repeat bend condition: 180°~ 0°)

[Note 8-2-3]

Do not hang LCD module by FPC or apply force to FPC.

9 Display Qualities and Warranty Period

Please refer to the incoming inspection standard (IIS).
The warranty period is 12 months from the month of shipment. If there is an individual contract, it will be discussed separately.

10 External Capacitors

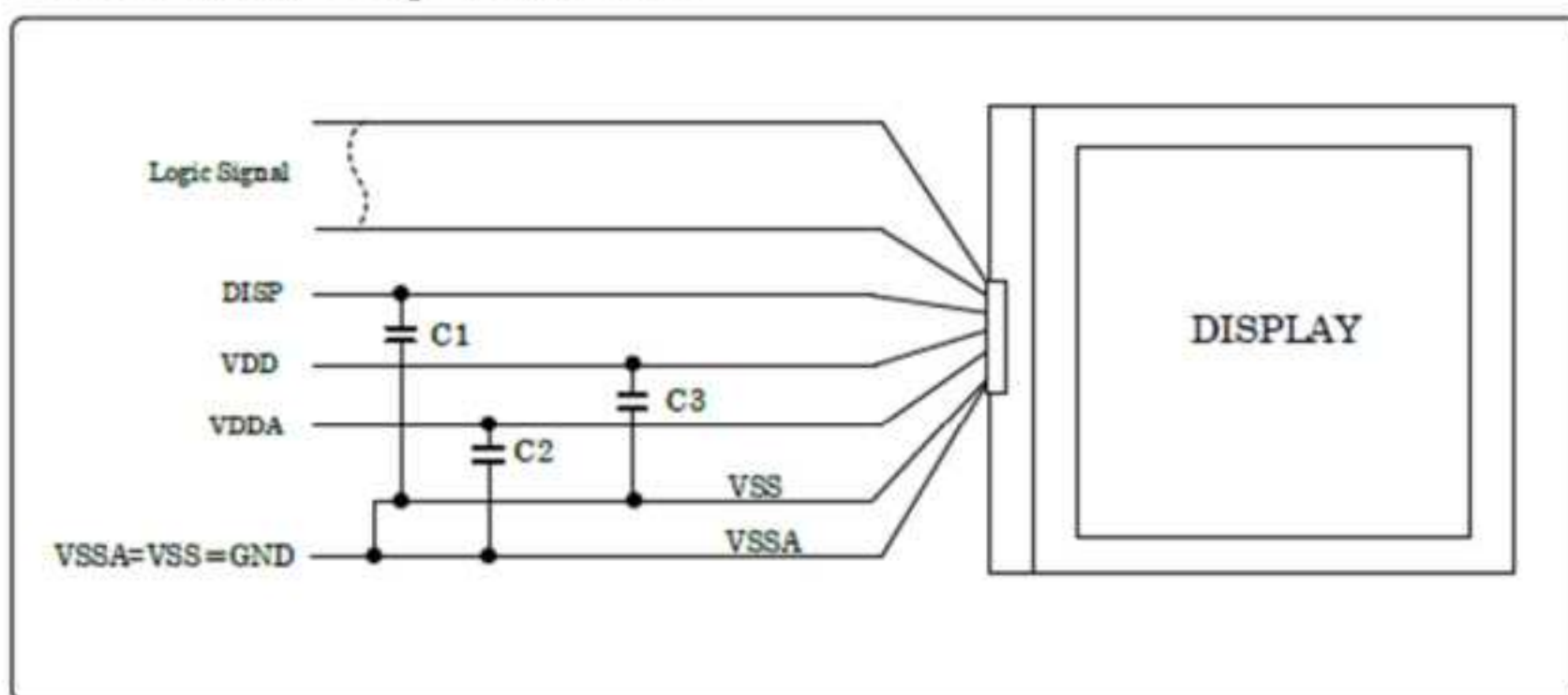


Figure 10-1 External capacitor recommendation capacity value

Recommended capacity value

C1 : DISP – VSS : rank B 560pF Ceramic capacitor

The recommended minimum capacitance value on DISP is 560pF,
However, it should be adjusted to ensure that the DISP rise time limit is not exceeded.

C2 : VDDA- VSSA : rank B 1.0uF Ceramic capacitor

C3 : VDD – VSS : rank B 1.0uF Ceramic capacitor

Above circuit and parts are only recommendation.
For actual use, please evaluate their conformity with your system and design.
(Capacitor value can be larger than value indicated above.)

11 Reliability Test Conditions

Table13-1-1 Reliability Test Items

| No. | Test Item | Condition | Remark |
|-----|---|---|------------------------|
| 1 | Non operating test | High temperature storage test Ta= + 80℃ | 240 h Note 13-1-1 |
| 2 | | Low temperature storage test Ta= -30℃ (No condensation) | 240 h Note 13-1-1 |
| 3 | | Thermal Shock test Ta= -30℃ (1 h) ~ +80 ℃ (1 h) | 5 cycle Note 13-1-1 |
| 4 | | Electro static discharge test ±200 V, 200 pF (0Ω) 1回 each terminal : 1 time | Note 13-1-1 |
| 5 | High temperature and high humidity operating test | Tp= 40℃ / 95%RH (No condensation) | 240 h Note 13-1-1 |
| 6 | High temperature operating test | Tp= + 70 ℃ | 240 h Note 13-1-1 |
| 7 | Low temperature operating test | Tp= -20℃ (No condensation) | 240 h Note 13-1-1 |

[Note 13-1-1]

Ta = Ambient temperature

Tp = Panel surface temperature

Result Evaluation Criteria

Under the display quality test conditions with normal operation state, these shall be no change which may affect practical display function.

(※)

normal operation state:

Temperature : +15 ~ +35℃

Humidity : 45 ~ 75%,

Atmospheric pressure : 86 ~ 106 kpa

12 Outline Dimensions

