DISPLAY Elektronik GmbH

DATA SHEET

TFT MODULE

DEM 640480L VMX-PW-N

(5,7“ TFT with MIPI)

Product Specification

Version: 0

01.04.2026

Revision History

Date	Rev. No.	Page	Summary
01.04.2026	0	ALL	FIRST ISSUE

Contents

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amo rphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit, Backlight Unit. The resolution of a 5.7 " TFT-LCD contains 640X480 pixels, and can display up to 65k/262k/16.7M colors.

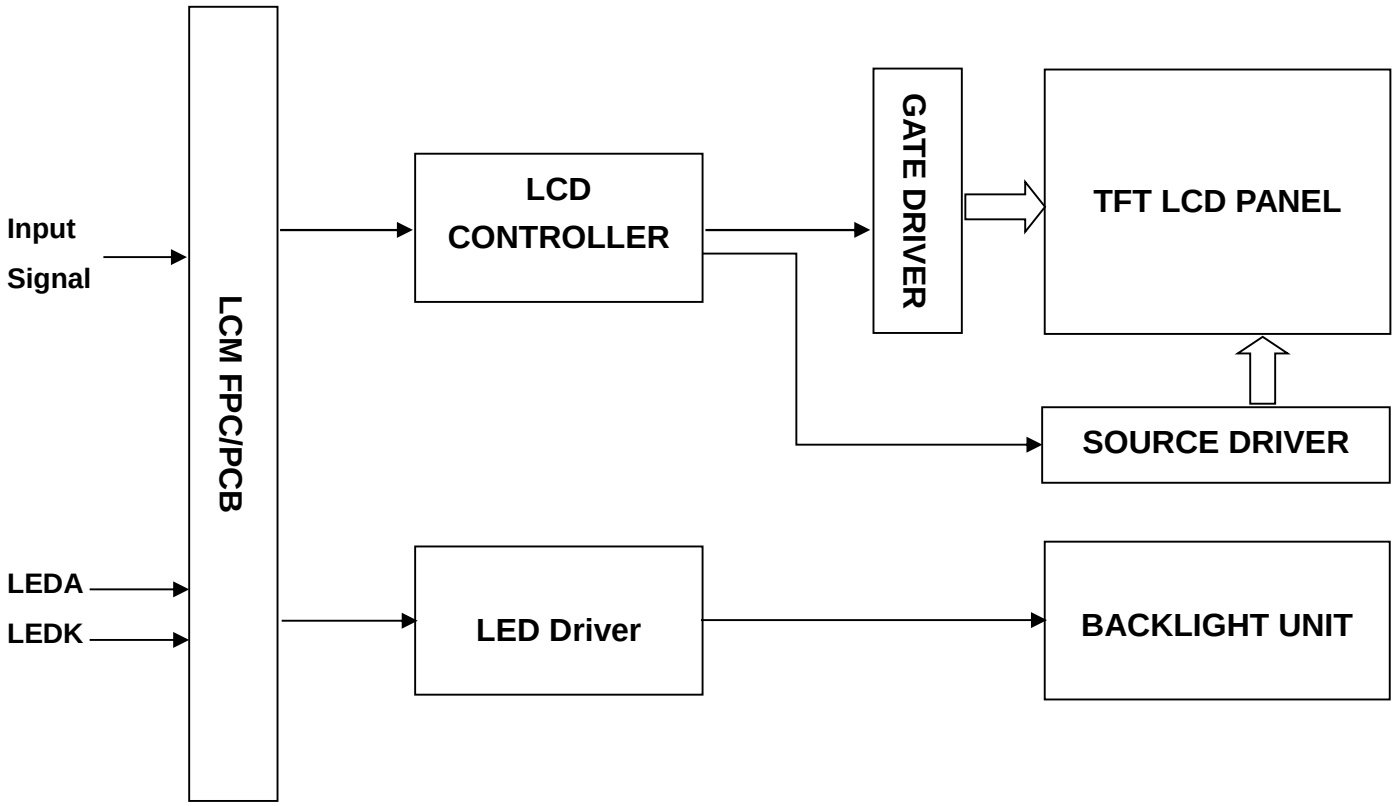
* Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display Area(AA)	115.20 x 86.40 (5.7 Inch)	mm	-
Driver Element	TFT Active Matrix	-	-
Display Colors	65k/262k/16.7M	colors	-
Number of Pixels	640 x (RGB) x 480	dots	-
Pixel Arrangement	RGB Vertical Stripe	-	-
Pixel Pitch	0.18 x 0.18	Mm	-
Viewing Angle	Free	o'clock	-
Controller IC	JD9168S	-	-
Display Mode	Transmissive / Normally Black	-	-
LCM Interface	2/3/4 Lane MIPI	-	-
Operating Temperature	-30 ~ +80	°C	-
Storage Temperature	-30 ~ +80	°C	-

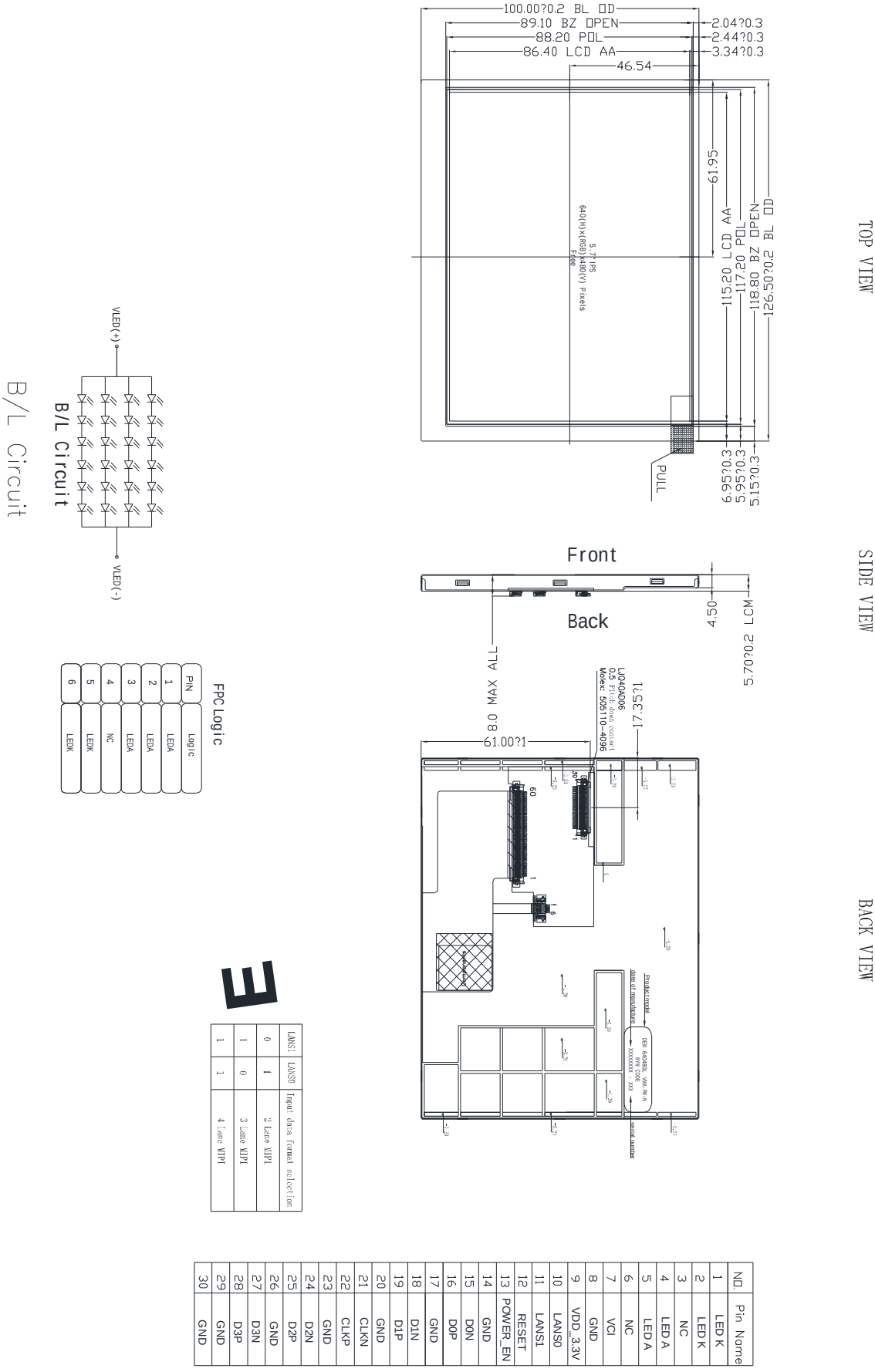
* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	126.5	-	mm	
	Vertical(V)	-	100	-	mm	
	Depth(D)	-	5.7	-	mm	
Weight		-	84	-	g	

1. Block Diagram



2. Outline Dimension



NO.	Pin Name
1	LED K
2	LED K
3	NC
4	LED A
5	LED A
6	NC
7	VCI
8	GND
9	VDD_3.3V
10	LANS0
11	LANS1
12	RESET
13	POWER_EN
14	GND
15	D0N
16	D0P
17	GND
18	D1N
19	D1P
20	GND
21	CLKN
22	CLKP
23	GND
24	D2N
25	D2P
26	GND
27	D3N
28	D3P
29	GND
30	GND

LANS1	LANS0	Input data format selection
0	1	2 Lane MIPI
1	0	3 Lane MIPI
1	1	4 Lane MIPI

3. Input Terminal Pin Assignment

CN3: 0.5 Pitch down contact (Molex: 505110-3096)

NO.	SYMBOL	DISCRIPTION	I/O
1	LEDK	LED Cathode	P
2	LEDK	LED Cathode	P
3	NC	--	--
4	LEDA	LED Anode	P
5	LEDA	LED Anode	P
6	NC	--	--
7	VCI	Power supply for digital circuits (2.85~3.3V)	P
8	GND	--	--
9	VDD_3.3V	Power supply for DC/DC convert circuit	P
10	LANS0	Vertical shift direction (gate output) selection(Note1)	I
11	LANS1	Horizontal shift direction (source output) selection(Note1)	I
12	RESET	Global reset pin. Active low to enter reset state.	I
13	POWER_EN	Display control / standby mode selection. POWER_EN= “Low”: Standby; POWER_EN = “High”: Normal display	I
14	GND	Ground	P
15	D0N	MIPI DSI differential data pair (Data lane 0)	I/O
16	D0P		
17	GND	Ground	P
18	D1N	MIPI DSI differential data pair (Data lane 1)	I/O
19	D1P		
20	GND	Ground	P
21	CLKN	MIPI DSI differential clock pair .	I
22	CLKP		
23	GND	Ground	P
24	D2N	MIPI DSI differential data pair (Data lane 2)	I/O
25	D2P		
26	GND	Ground	P
27	D3N	MIPI DSI differential data pair (Data lane 3) MIPI DSI differential data pair (Data lane 3)	I/O
28	D3P		
29	GND	Ground	P
30	GND	Ground	P

Note1:

LANS1	LANS0	Input data format selection
0	1	2 Lane MIPI
1	0	3 Lane MIPI
1	1	4 Lane MIPI

4. LCD Optical Characteristics

4.1 Optical Specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal Viewing Angle	1000	1200	--		(1)(2)
Response Time	Rising	$T_{R+}T_F$		--	30	35	msec	(1)(3)
	Falling							
Color Gamut		S(%)	--	50	56	--	%	
Color Filter Chromacicity	White	W_X	--	-0.04	0.303	+0.04		(1)(4) CA-310
		W_Y	--		0.343			
	Red	R_X	--		0.622			
		R_Y	--		0.367			
	Green	G_X	--		0.332			
		G_Y	--		0.592			
	Blue	B_X	--		0.152			
		B_Y	--		0.121			
Viewing Angle	Hor.	ΘL	CR>10	80	85	--		(1)(4)
		ΘR		80	85	--		
	Ver.	ΘU		80	85	--		
		ΘD		80	85	--		
Option View Direction		Free						

* The data comes from the LCD specification.

Measuring Condition

Measuring surrounding: dark room

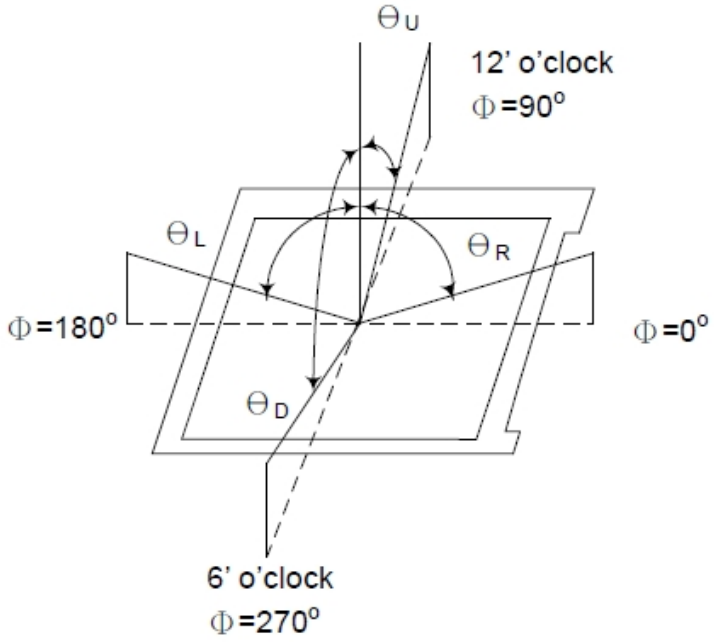
Ambient temperature: 25°C±2°C

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

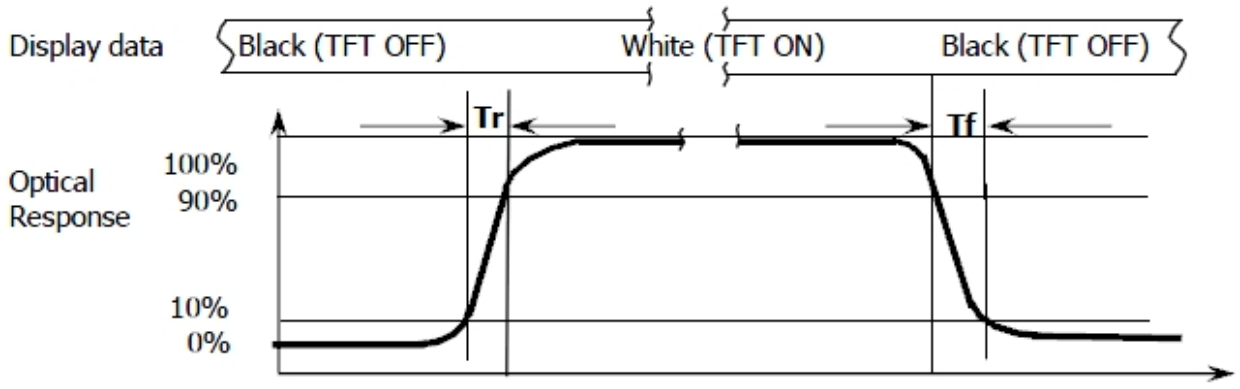
Note (1): Definition of Viewing Angle:



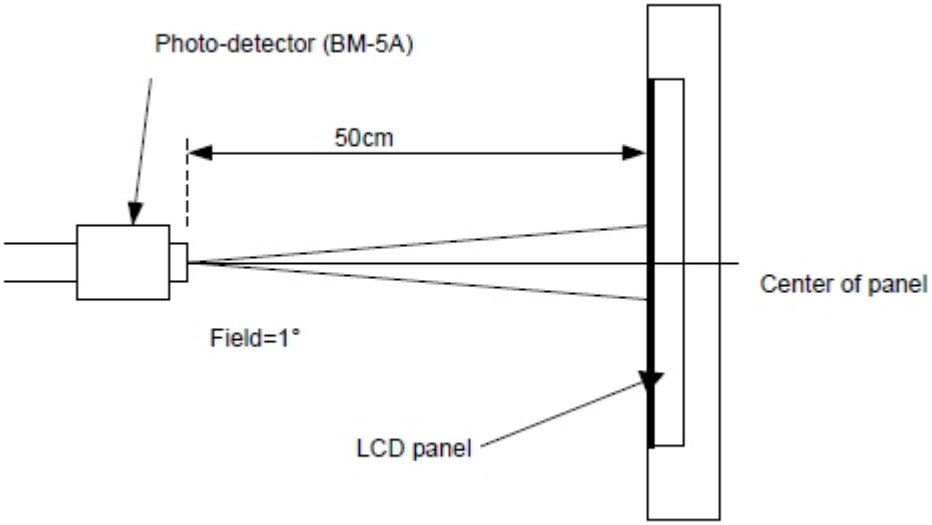
Note (2): Definition of Contrast Ratio (CR): measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



5. Electrical Characteristics

5.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VDD	-0.5	3.6	V	Note1
	VCI	-0.5	3.6	V	Note1
Operating Temperature	T_{OP}	-30	+80	°C	-
Storage Temperature	T_{ST}	-30	+80	°C	-

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.5	3.3	3.6	V	-
	VCI	2.5	3.3	3.6	V	-
Normal Mode Current	IDD	--	40	80	mA	-
Level Input Voltage	V_{IH}	0.7VCI	--	VCI	V	-
	V_{IL}	GND	--	0.3VCI	V	-
Level Output Voltage	V_{OH}	0.8VCI	--	VCI	V	-
	V_{OL}	GND	--	0.2VCI	V	-

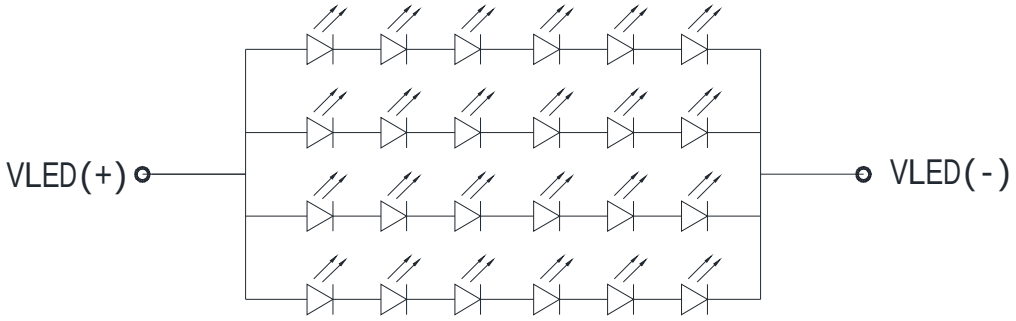
5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 24 chips LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	--	80	--	mA	--
Forward Voltage	V_F	16.2	18	19.8	V	--
LCM Luminance (IF=80mA)	LV	500	650	--	cd/m2	Note3
LED Lifetime	Hr	50000	--	--	H	Note1,2
Uniformity	Avg	80	--	--	%	Note3

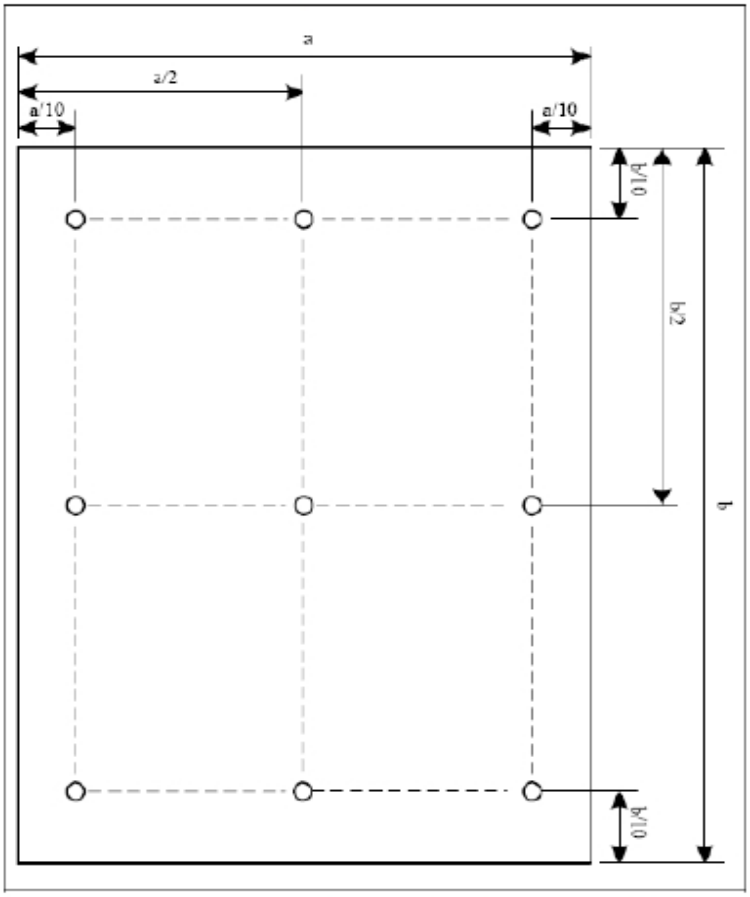
Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25°C±3°C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED Lifetime” is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=80 mA. The LED Lifetime could be decreased if operating IL is larger than 80mA. The constant current driving method is suggested.



B/L Circuit

Note (3) Luminance Uniformity of these 9 points is defined as below:

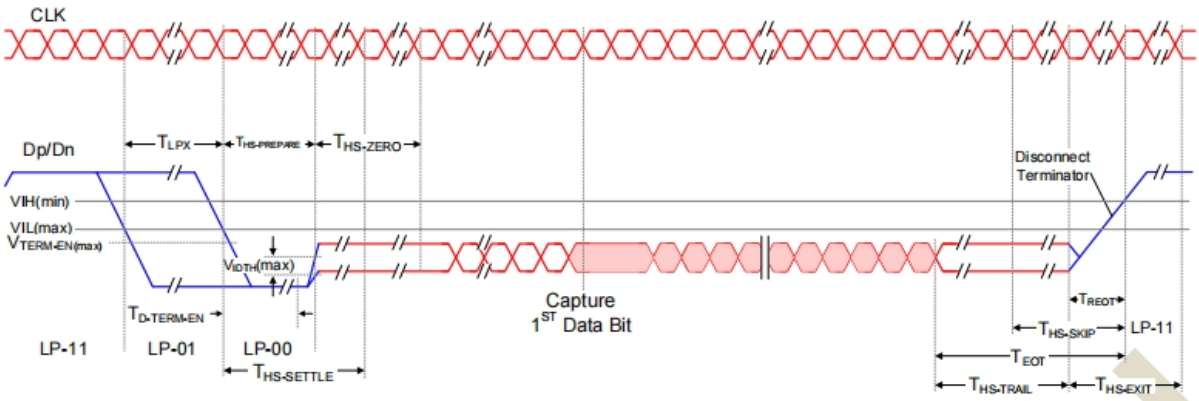


$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

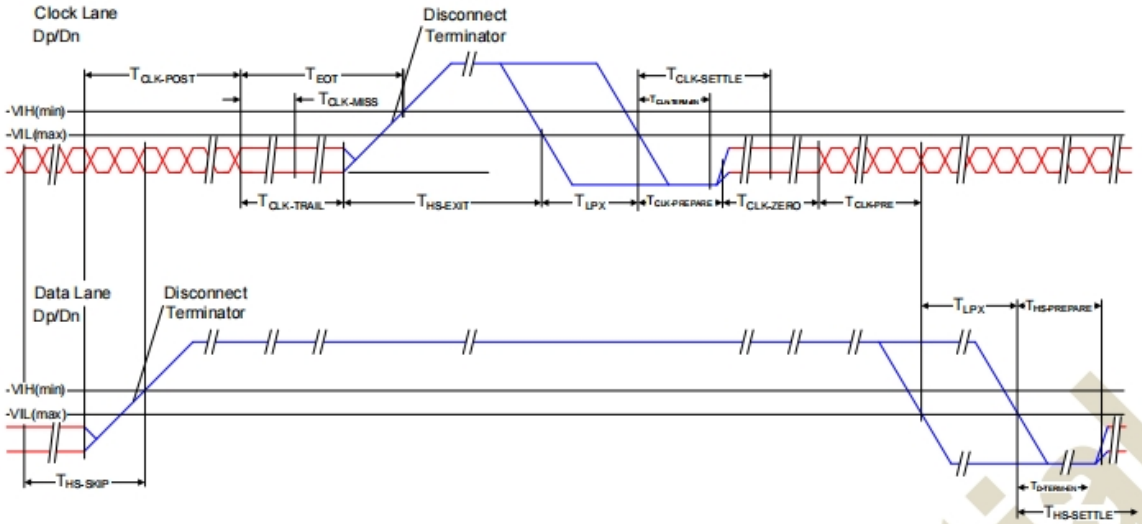
6. AC Characteristic

6.1 Burst Mode Data Transmission



High-Speed Data Transmission in Bursts

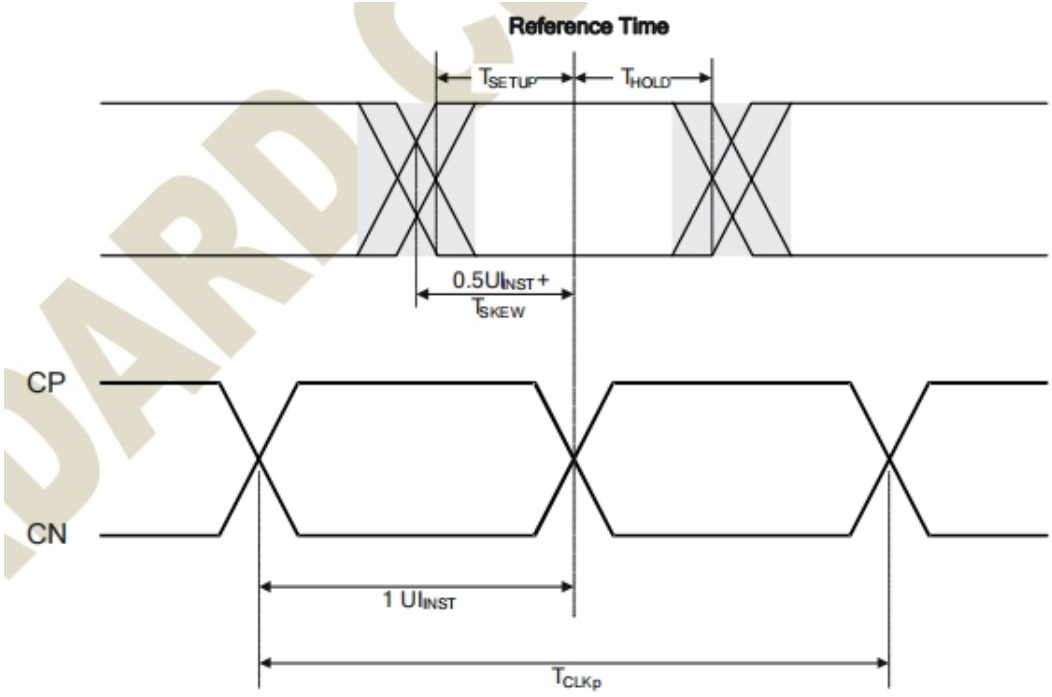
Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	Max(n*8*UI, 60+n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns



Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

6.2 MIPI Data-Clock Timing Specification



Data to Clock Timing Definitions

The UIINST specifications for the Clock signal are summarized in following Table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	3.33	ns	(1), (2), (3), (4), (5)

Note: (1) This value corresponds to a minimum 300 Mbps data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
(3) Maximum total bit rate is 630Mbps/per lane of 2 data lanes 24-bit data format
(4) Maximum total bit rate is 600Mbps/per lane of 3 data lanes 24-bit data format
(5) Maximum total bit rate is 500Mbps/per lane of 4 data lanes 24-bit data format

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [RX]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [RX]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

Note: (1) Total setup and hold window for receiver of 0.3*UIINST.

Data to Clock Timing Specifications

6.3 Timing for DSI Video Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	FCLK	--	(21)	--	MHz
Horizontal display area	HDISP	--	640	--	Clock
Horizontal Sync. Width	hpw	1	10	--	Clock
Horizontal Sync. Back Porch	hbp	1	18	--	Clock
Horizontal Sync. Front Porch	hfp	1	20	--	Clock
Vertical display area	VDISP	--	480	--	Line
Vertical Sync. Width	vs	1	4	--	Line
Vertical Sync. Back Porch	vbp	1	10	--	Line
Vertical Sync. Front Porch	vfp	1	14	--	Line
Frame-Rate		--	60	--	Hz

Note: 1. Typical value are related to the setting frame rate is 60Hz.

6.4 Reset Input Timings

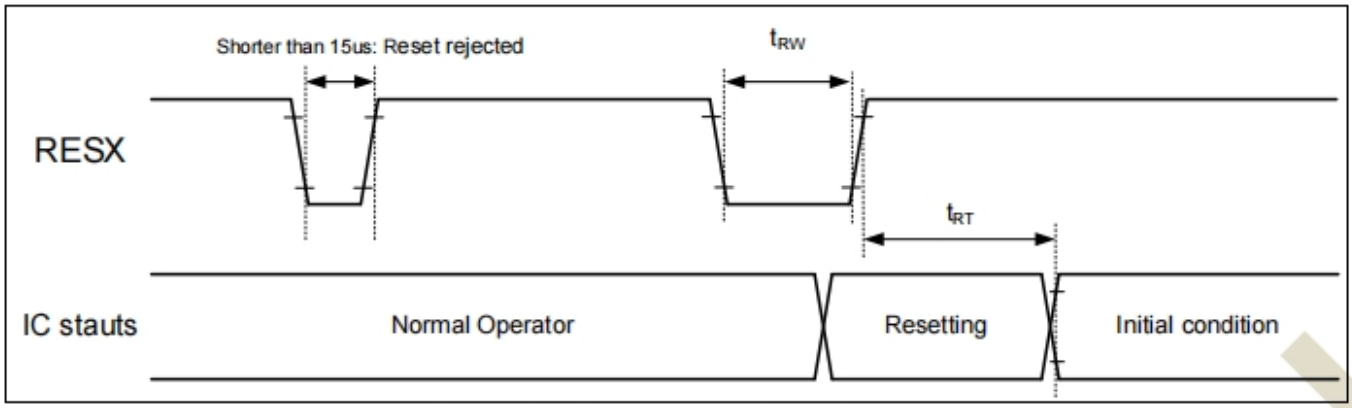


Figure 11.2: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset "L" pulse width(2)	RESX	20	-	µs
t_{RT}	Reset complete time(3)	-	-	5(5)	ms
		-	-	120(6) (7) (8)	ms

Note:

(1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset complete time (t_{RT}) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 15 µs	Reset Rejected
Longer than 20 µs	Reset
Between 15 µs and 20 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:

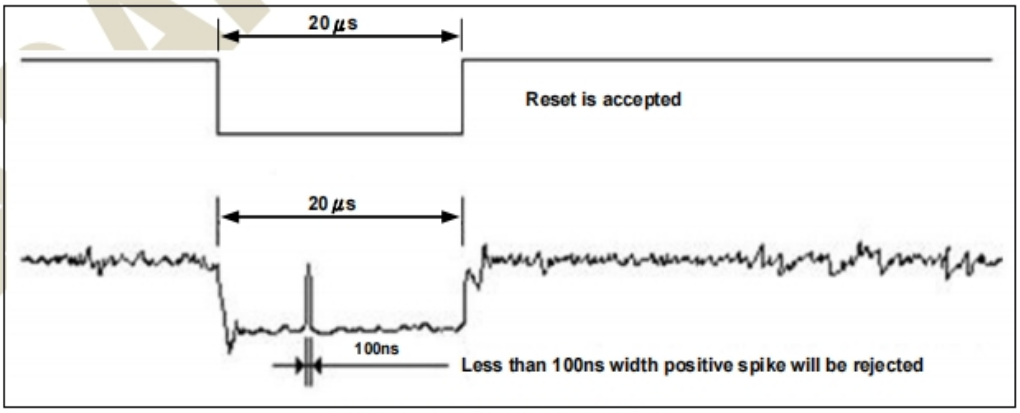


Table 11.4: Reset timings

(5) When Reset is applied during Sleep In Mode.
(6) When Reset is applied during Sleep Out Mode.
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out command, it is necessary to wait 120msec then send RESX.

7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

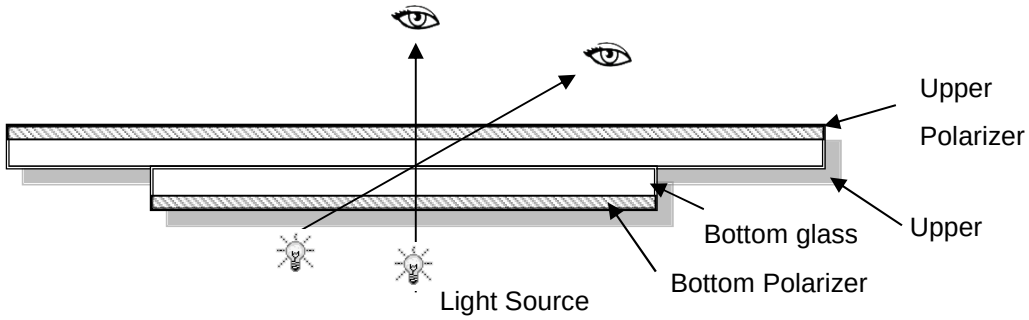
Temperature: 25°C±5°C

Humidity: 65%±10%RH

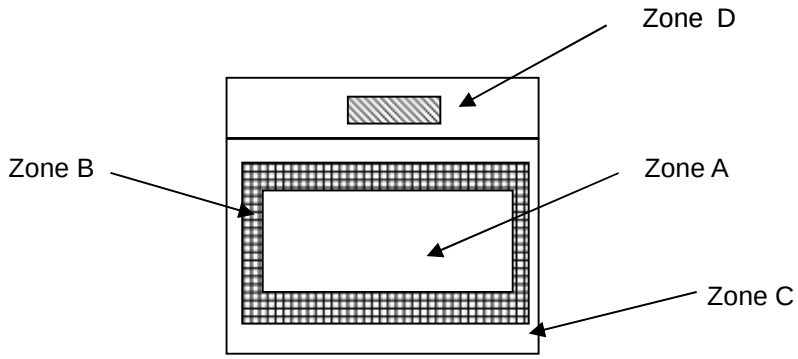
Viewing Angle: Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing Distance: 30-50cm



7.1.2 Definition



Zone A: Effective Viewing Area (Character or Digit can be seen)

Zone B: Viewing Area except Zone A

Zone C: Outside (Zone A+Zone B) which can not be seen after assembly by customer)

Zone D: IC Bonding Area

Note: As a general rule, visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

7.1.3 Sampling Plan

According to GB/T 2828-2003; Normal Inspection, Class Ⅱ

AQL:

Major Defect	Minor Defect
0.65	1.5

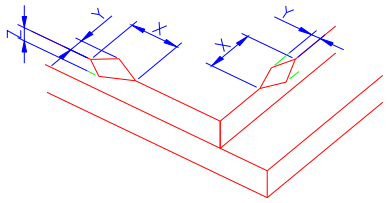
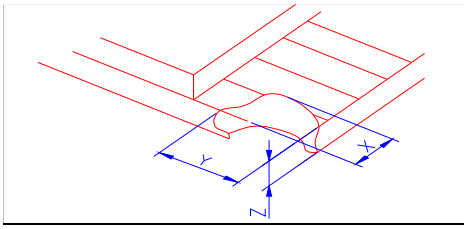
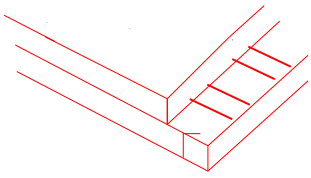
LCD: Liquid Crystal Display, LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc…	Major
2	Missing	Missing components and etc…	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed,deformation and etc…	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot,Dim spot,(Note1) Polarizer Air Bubble, Polarizer accidented spot and etc…	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc…	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

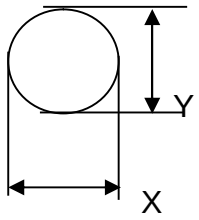
Note1: a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

7.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

2.0 Spot defect



Φ=(X+Y)/2

① light dot（ black/white spot , pinhole, stain，etc.）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧10mm)		
0.25<Φ≤0.4	2(distance≧10mm)		
Φ>0.4	0		

② Dim spot（light leakage、dent、dark spot，etc）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧10mm)		
0.25<Φ≤0.4	2(distance≧10mm)		
Φ>0.4	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.5	2(distance≧10mm)		
Φ>0.5	0		

④Polarizer Bubble

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.4	2(distance≧10mm)		
0.4<Φ≤0.5	1		
Φ>0.5	0		

3.0 LCD Pixel defect

Pixel bad points

Item	Zone A	Acceptable Qty
Bright dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Dark dot	Random	N≤3
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm
Total bright and dark dot		N≤4

Note:

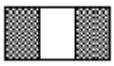
A) Bright dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

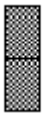
C) 2 dot adjacent = 1 pair = 2 dots

Picture:

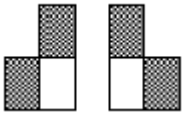
2 dot adjacent



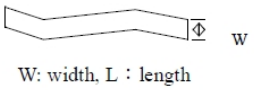
2 dot adjacent



2 dot adjacent (vertical)



2 dot adjacent (slant)

<table>
<tr>
<td>4.0</td>
<td>Line defect (LCD /Polarizer backlight black/white line, scratch, stain)
 

N：Count</td>
<td>
<table>
<tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.05</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L≤5.0</td><td colspan="2">N≤3</td></tr>
<tr><td>0.06<W≤0.08</td><td>L≤4.0</td><td colspan="2">N≤2</td></tr>
<tr><td>W>0.08</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td>
</tr>
<tr>
<td>5.0</td>
<td>Electronic Components SMT.</td>
<td>Not allow missing parts，solderless connection，cold solder joint，mismatch，The positive and negative polarity opposite</td>
</tr>
<tr>
<td>6.0</td>
<td>Display color& Brightness.</td>
<td>1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td>
</tr>
<tr>
<td>7.0</td>
<td>LCD Mura/Waving/ Hot spot</td>
<td>Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.</td>
</tr>
</table>

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

8. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	80°C, 96h	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1. Air bubble in the LCD; 2. Non-display; 3. Missing segments/line; 4. Glass crack; 5. Current IDD is twice higher than initial value.
Low Temperature Operating	-30°C, 96h	
High Temperature Storage	80°C, 96h	
Low Temperature Storage	-30°C, 96h	
High Temperature & High Humidity Operating	+60°C, 90% RH, 96h	
Thermal Shock (Non-operation)	-10°C, 30 min ↔ 60°C, 30 min, Change Time: 5min 20CYC.	
ESD Test	C=150pF, R=330,5points/panel Air:±8kV, 5times; Contact:±6kV, 5 times; (Environment: 15°C~35°C, 30%~60%).	
Vibration (Non-operation)	Frequency Range: 10~55Hz, Stroke: 1.5mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝ (MEDIUM	

Remark:

1. The test samples should be applied to only one test item.
2. Sample size for each test item is 5~10pcs.
3. For Damp Proof Test, Pure water (Resistance > 10MΩ) should be used.
4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
5. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6. The color fading mura of polarizing filter should not care.

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the “Power ON” condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed.
Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.