

Display Elektronik GmbH

# DATA SHEET

*TFT- MODULE*

**DEM 640480H VMH-PW-N**

**5,7" IPS TFT**

Product Specification

Ver.: 1

31.05.2024

**Revision History**

<b>Revision</b>	<b>Date</b>	<b>Originator</b>	<b>Detail</b>	<b>Remarks</b>
0	27.05.2024	LL	Initial Release	-
1	31.05.2024	DFG	Modify Module Parameter Add Chromaticity Transmissive Modify Outline Drawing(B)	P4 P6 P29

**Table of Contents**

No.	Item	Page
1.	General Description .....	4
2.	Module Parameter .....	4
3.	Absolute Maximum Ratings .....	4
4.	DC Characteristics .....	5
5.	Backlight Characteristics .....	5
5.1.	Backlight Characteristics.....	5
5.2.	Backlighting Circuit .....	5
6.	Optical Characteristics .....	6
6.1.	Optical Characteristics .....	6
6.2.	Definition of Response Time .....	6
6.3.	Definition of Contrast Ratio .....	7
6.4.	Definition of Viewing Angles.....	7
6.5.	Definition of Color Appearance .....	8
6.6.	Definition of Surface Luminance, Uniformity and Transmittance.....	8
7.	Block Diagram and Power Supply .....	9
8.	Interface Pins Definition .....	10
9.	AC Characteristics .....	14
9.1.	3-Wire SPI Interface Timing.....	14
9.2.	LVDS Interface .....	15
9.3.	RGB Interface Timing.....	17
9.4.	Reset Timing .....	18
10.	Quality Assurance .....	19
10.1.	Purpose .....	19
10.2.	Standard for Quality Test.....	19
10.3.	Nonconforming Analysis & Disposition .....	19
10.4.	Agreement Items.....	19
10.5.	Standard of the Product Visual Inspection .....	19
10.6.	Inspection Specification .....	20
10.7.	Classification of Defects.....	24
10.8.	Identification/marketing criteria .....	24
10.9.	Packing .....	24
11.	Reliability Specification .....	25
12.	Precautions and Warranty .....	26
12.1.	Safety .....	26
12.2.	Handling .....	26
12.3.	Storage.....	26
12.4.	Metal Pin (Apply to Products with Metal Pins) .....	26
12.5.	Operation .....	27
12.6.	Static Electricity .....	27
12.7.	Limited Warranty .....	27
13.	Outline Drawings.....	28

**1. General Description**

The specification is a transmissive type color active matrix liquid crystal display (LCD) which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT-LCD panel, driver ICs and a backlight unit.

**2. Module Parameter**

Features	Details	Unit
Display Size (Diagonal)	5.7"	-
LCD Type	IPS TFT	-
Display Mode	Normal Black/Transmissive	-
Resolution	640 x RGB x 480	Pixels
View Direction	Full View	Best Image
Module Outline	127.00 x 98.43 x 5.90 (Note1 )	mm
Active Area	115.20 x 86.40	mm
Pixel Size	0.180 x 0.180	mm
Pixel Arrangement	RGB Vertical Stripe	-
Display Colors	16.7 Million	-
Driver IC	JD9168S	-
Interface	MIPI (DSI) LVDS 24-bit&18-bitRGB	-
With or Without Touch Panel	Without	-
Operating Temperature	-20°C to +70°C	°C
Storage Temperature	-30°C to +80°C	°C
Weight	90	g

Note 1: Exclusive hooks, posts, FFC/FPC tail etc.

**3. Absolute Maximum Ratings**

GND=0V, Ta=25°C

Item	Symbol	Min.	Max.	Unit
Supply Voltage	IOVCC	-0.3	6.3	V
	AVDD	-0.3	6.3	V
	AVEE	-0.3	-6.3	V
Storage temperature	T <sub>STG</sub>	-30	80	°C
Operating temperature	T <sub>OP</sub>	-20	70	°C

Note 1: If Ta below 50°C, the maximal humidity is 90%RH, if Ta over 50°C, absolute humidity should be less than 60%RH.

Note 2: The response time will be extremely slow when the operating temperature is around -10°C, and the back ground will become darker at high temperature operating.

4. DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	IOVCC	2.5	3.3	3.3	V
	AVDD	4.5	5.5	6.0	V
	AVEE	-4.5	-5.5	-6.0	V
Logic Low Input Voltage	V <sub>IL</sub>	GND	-	0.3*IOVCC	V
Logic High Input Voltage	V <sub>IH</sub>	0.7*IOVCC	-	IOVCC	V
Output low Voltage	V <sub>OL</sub>	GND	-	GND+0.4	V
Output high Voltage	V <sub>OH</sub>	IOVCC-0.4	-	IOVCC	V
Current Consumption All White	I <sub>CC</sub>	-	75	-	mA

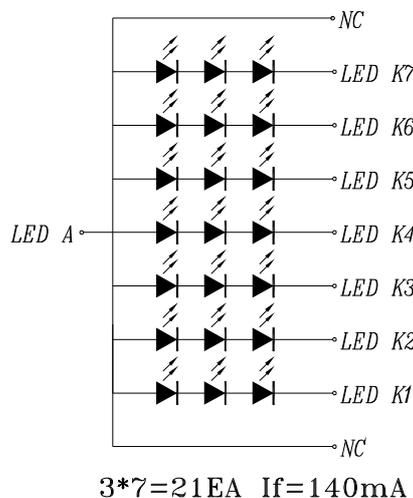
5. Backlight Characteristics

5.1. Backlight Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Backlight Voltage	V <sub>LED</sub>	Ta=25 °C, I <sub>F</sub> =20mA/LED	8.1	9	9.9	V
Backlight Current	I <sub>LED</sub>	Ta=25 °C, V <sub>F</sub> =3.0V/LED	-	140	-	mA
Power Dissipation	P <sub>D</sub>		-	1260	-	mW
Uniformity	Avg		-	80	-	%
LED Lifettime (+25°C)	-		-	30000	-	Hrs
Drive Method	Constant Current					
LED Configuration	21 White LEDs (3 LEDs in one string and 7 groups in parallel)					

Note1: LED lifetime defined as follows: The final brightness is at 50% of original brightness.  
 The environmental conducted under ambient air flow, at Ta=25°C± 2°C, 60%RH± 5%, I<sub>F</sub>=20mA/LED.

5.2. Backlighting Circuit



6. Optical Characteristics

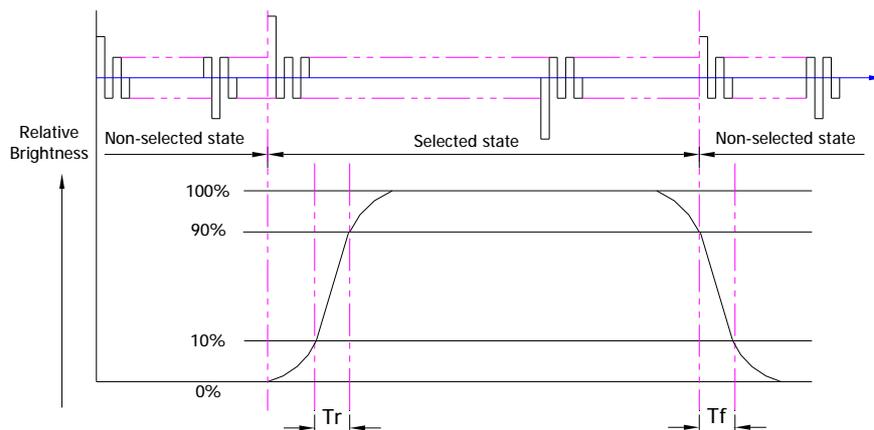
6.1. Optical Characteristics

Ta=25°C, IOVCC=3.3V

	Item	Symbol	Condition	Specification			Unit	
				Min.	Typ.	Max.		
Backlight On (Transmissive Mode)	Luminance on TFT( $I_f=20\text{mA/LED}$ )	Lv	Normally viewing angle $\theta_x = \phi_y = 0^\circ$	488	610	-	cd/m <sup>2</sup>	
	Contrast Ratio(See 6.3)	CR		1000	1200	-	-	
	Response Time (See 6.2)	TR+TF		-	30	35	ms	
	Chromaticity Transmissive (See 6.5)	Red	X <sub>R</sub>	-	0.606	0.656	0.706	-
			Y <sub>R</sub>		0.271	0.321	0.371	-
		Green	X <sub>G</sub>		0.271	0.321	0.371	-
			Y <sub>G</sub>		0.567	0.617	0.667	-
		Blue	X <sub>B</sub>		0.070	0.120	0.170	-
			Y <sub>B</sub>		0.076	0.126	0.176	-
	White	X <sub>W</sub>	0.261	0.311	0.361	-		
Y <sub>W</sub>		0.332	0.382	0.432	-			
Viewing Angle (See 6.4)	Horizontal	$\theta_{x+}$	Center CR≥10	75	80	-	Deg.	
		$\theta_{x-}$		75	80	-		
	Vertical	$\phi_{y+}$		75	80	-		
		$\phi_{y-}$		75	80	-		
NSTC			$\Theta=0^\circ$	55	60	-	%	

6.2. Definition of Response Time

6.2.1. Normally Black Type (Negative)

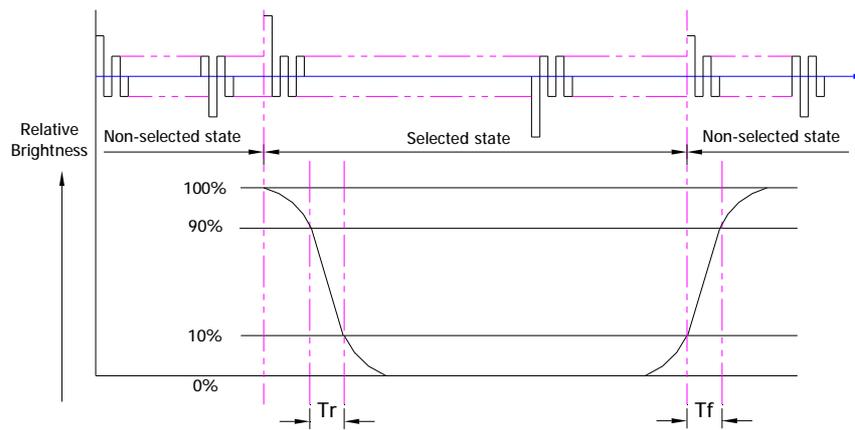


Tr is the time it takes to change from non-selected stage with relative luminance 10% to selected state with relative luminance 90%;

Tf is the time it takes to change from selected state with relative luminance 90% to non-selected state with relative luminance 10%

Note: Measuring machine: LCD-5100

6.2.2. Normally White Type (Positive)



Tr is the time it takes to change from non-selected stage with relative luminance 90% to selected state with relative luminance 10%;

Tf is the time it takes to change from selected state with relative luminance 10% to non-selected state with relative luminance 90%;

Note: Measuring machine: LCD-5100 or EQUI

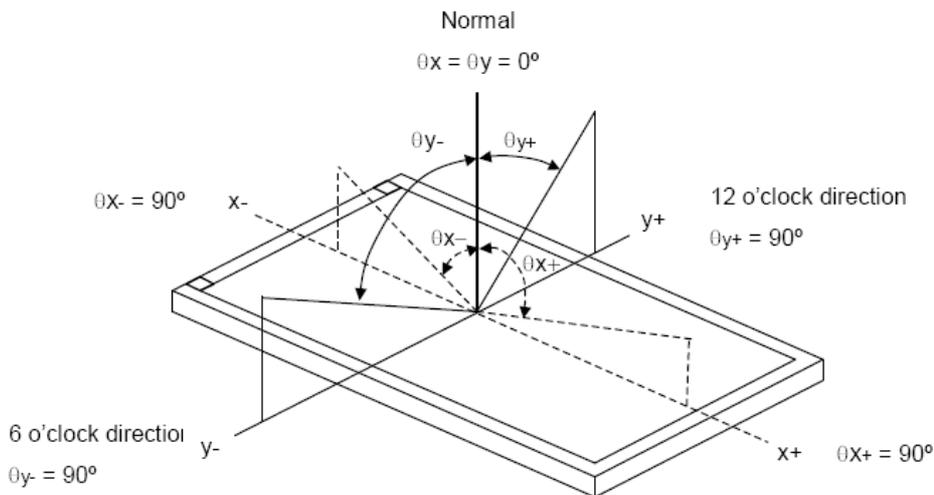
6.3. Definition of Contrast Ratio

Contrast is measured perpendicular to display surface in reflective and transmissive mode. The measurement condition is:

Measuring Equipment	Eldim or Equivalent
Measuring Point Diameter	3mm//1mm
Measuring Point Location	Active Area centre point
Test pattern	A: All Pixels white
	B: All Pixel black
Contrast setting	Maximum

Definitions: CR (Contrast) = Luminance of White Pixel / Luminance of Black Pixel

6.4. Definition of Viewing Angles



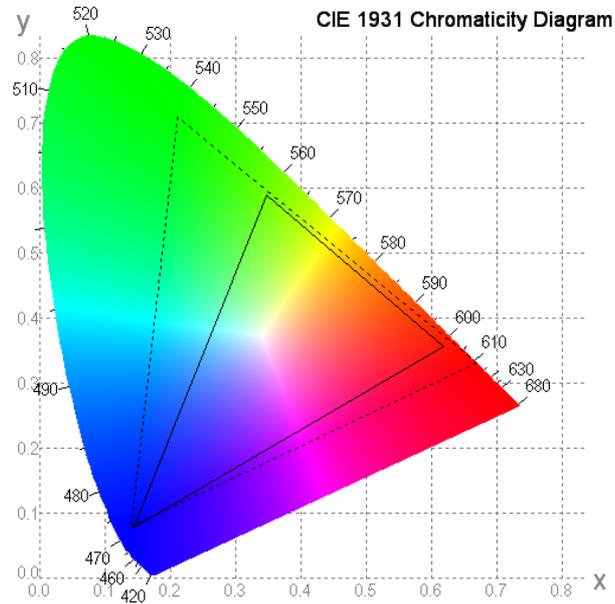
Measuring machine: LCD-5100 or EQUI

**6.5. Definition of Color Appearance**

R,G,B and W are defined by (x, y) on the IE chromaticity diagram

NTSC=area of RGB triangle/area of NTSC triangleX100%

Measuring picture: Red, Green, Blue and White (Measuring machine: BM-7)



**6.6. Definition of Surface Luminance, Uniformity and Transmittance**

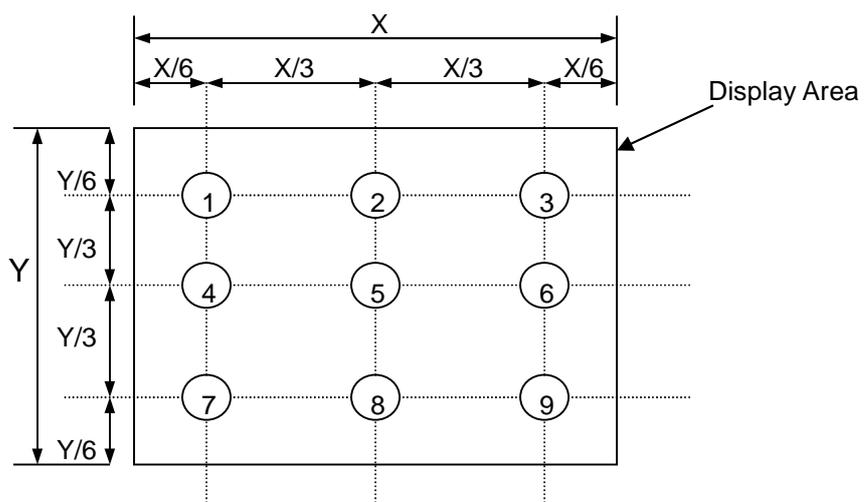
Using the transmissive mode measurement approach, measure the white screen luminance of the display panel and backlight.

6.6.1. Surface Luminance:  $L_v = \text{average} (L_{P1}:L_{P9})$

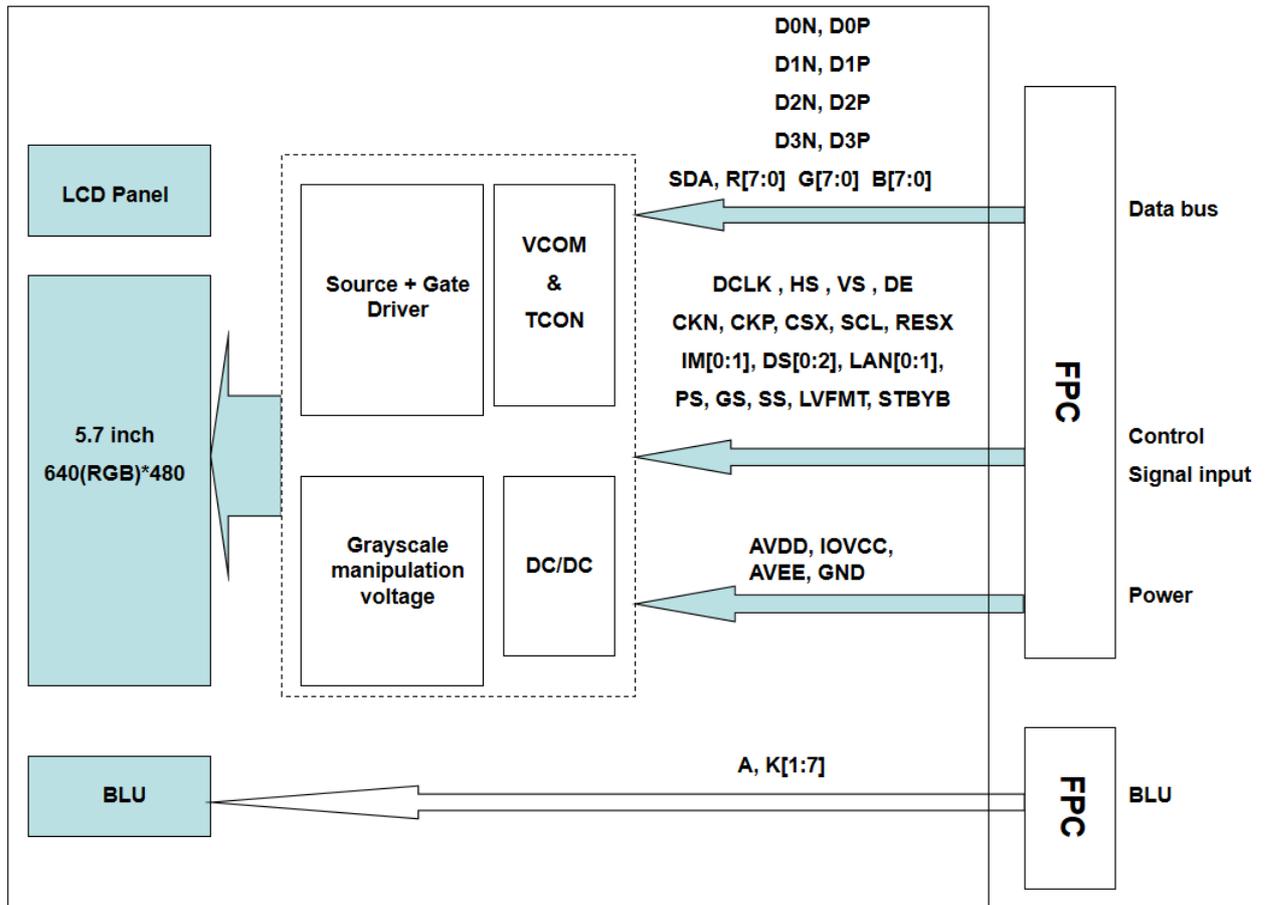
6.6.2. Uniformity =  $\text{Minimal} (L_{P1}:L_{P9}) / \text{Maximal} (L_{P1}:L_{P9}) * 100\%$

6.6.3. Transmittance =  $L_v \text{ on LCD} / L_v \text{ on Backlight} * 100\%$

Note: Measuring machine: BM-7



7. Block Diagram and Power Supply



8. Interface Pins Definition

No.	Symbol	Function						
1	SDA	Serial communication data input and output						
2	CSX	Serial communication chip selection						
3	SCL	Serial communication clock input						
4	RESX	Reset pin						
5	B0	Blue data						
6	B1	Blue data						
7	B2	Blue data						
8	B3	Blue data						
9	B4	Blue data						
10	B5	Blue data						
11	B6	Blue data						
12	B7	Blue data						
13	G0	Green data						
14	G1	Green data						
15	G2	Green data						
16	G3	Green data						
17	G4	Green data						
18	G5	Green data						
19	G6	Green data						
20	G7	Green data						
21	R0	Red data						
22	R1	Red data						
23	R2	Red data						
24	R3	Red data						
25	R4	Red data						
26	R5	Red data						
27	R6	Red data						
28	R7	Red data						
29	GS	<p>Gate driver scan direction on panel module</p> <table border="1"> <thead> <tr> <th>GS</th> <th>Direction</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>G[1, 2, 3 → ... → 1024 ]</td> </tr> <tr> <td>1</td> <td>G[1024, 1023, 1022 → ... → 1 ]</td> </tr> </tbody> </table>	GS	Direction	0	G[1, 2, 3 → ... → 1024 ]	1	G[1024, 1023, 1022 → ... → 1 ]
GS	Direction							
0	G[1, 2, 3 → ... → 1024 ]							
1	G[1024, 1023, 1022 → ... → 1 ]							
30	SS	<p>Source driver scan direction on panel module.</p> <table border="1"> <thead> <tr> <th>SS</th> <th>Direction</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>S[1, 2, 3 → → 1536 ]</td> </tr> <tr> <td>1</td> <td>S[1536, 1535, 1534 → → 1 ]</td> </tr> </tbody> </table>	SS	Direction	0	S[1, 2, 3 → → 1536 ]	1	S[1536, 1535, 1534 → → 1 ]
SS	Direction							
0	S[1, 2, 3 → → 1536 ]							
1	S[1536, 1535, 1534 → → 1 ]							
31	LAN0	<p>Select the lane mode as listed below:</p> <table border="1"> <tr> <td>LANSEL[1:0]</td> <td>DSI IF</td> <td>LVDS IF</td> </tr> </table>	LANSEL[1:0]	DSI IF	LVDS IF			
LANSEL[1:0]	DSI IF	LVDS IF						

32	LAN1																
33	LVFMT	<p>Data format select for LVDS mode.</p> <table border="1"> <thead> <tr> <th>LVFMT</th> <th>Format</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>VESA</td> </tr> <tr> <td>1</td> <td>JEIDA</td> </tr> </tbody> </table>	LVFMT	Format	0	VESA	1	JEIDA									
LVFMT	Format																
0	VESA																
1	JEIDA																
34	STBYB	<p>Standby mode.</p> <table border="1"> <thead> <tr> <th>STBYB</th> <th>IC Status</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Standby Mode</td> </tr> <tr> <td>1</td> <td>Normal Mode</td> </tr> </tbody> </table>	STBYB	IC Status	0	Standby Mode	1	Normal Mode									
STBYB	IC Status																
0	Standby Mode																
1	Normal Mode																
35	IM1	<p>Select the interface mode as listed below:</p> <table border="1"> <thead> <tr> <th colspan="2">IM[1:0]</th> <th>Interface</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>DSI</td> </tr> <tr> <td>0</td> <td>1</td> <td>LVDS</td> </tr> <tr> <td>1</td> <td>0</td> <td>RGB</td> </tr> <tr> <td>1</td> <td>1</td> <td>Not used</td> </tr> </tbody> </table> <p>RGB IF data format (RGB565 / RGB666 / RGB888) is selected by DCS command (0x3A).</p>	IM[1:0]		Interface	0	0	DSI	0	1	LVDS	1	0	RGB	1	1	Not used
IM[1:0]			Interface														
0	0	DSI															
0	1	LVDS															
1	0	RGB															
1	1	Not used															
36	IM0																
37	DCLK	Sample clock															
38	DE	Data Input Enable															
39	VS	Vertical Sync Input															
40	HS	Horizontal Sync Input															

41	DS2	Select for <b>DSI</b> data lane sequence and polarity.	<table border="1"> <thead> <tr> <th>PSWAP</th> <th>DSWAP[2:0]</th> <th>D0N</th> <th>D0P</th> <th>D1N</th> <th>D1P</th> <th>CKN</th> <th>CKP</th> <th>D2N</th> <th>D2P</th> <th>D3N</th> <th>D3P</th> </tr> </thead> <tbody> <tr><td>0</td><td>000</td><td>D2-</td><td>D2+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D0-</td><td>D0+</td><td>D3-</td><td>D3+</td></tr> <tr><td>0</td><td>001</td><td>D2-</td><td>D2+</td><td>D0-</td><td>D0+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D3-</td><td>D3+</td></tr> <tr><td>0</td><td>010</td><td>D3-</td><td>D3+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D0-</td><td>D0+</td><td>D2-</td><td>D2+</td></tr> <tr><td>0</td><td>011</td><td>D3-</td><td>D3+</td><td>D0-</td><td>D0+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td></tr> <tr><td>0</td><td>100</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr> <tr><td>0</td><td>101</td><td>D3-</td><td>D3+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D2-</td><td>D2+</td><td>D0-</td><td>D0+</td></tr> <tr><td>0</td><td>110</td><td>D0-</td><td>D0+</td><td>D2-</td><td>D2+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D3-</td><td>D3+</td></tr> <tr><td>0</td><td>111</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td></tr> <tr><td>1</td><td>000</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D0+</td><td>D0-</td><td>D3+</td><td>D3-</td></tr> <tr><td>1</td><td>001</td><td>D2+</td><td>D2-</td><td>D0+</td><td>D0-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D3+</td><td>D3-</td></tr> <tr><td>1</td><td>010</td><td>D3+</td><td>D3-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D0+</td><td>D0-</td><td>D2+</td><td>D2-</td></tr> <tr><td>1</td><td>011</td><td>D3+</td><td>D3-</td><td>D0+</td><td>D0-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td></tr> <tr><td>1</td><td>100</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr> <tr><td>1</td><td>101</td><td>D3+</td><td>D3-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D2+</td><td>D2-</td><td>D0+</td><td>D0-</td></tr> <tr><td>1</td><td>110</td><td>D0+</td><td>D0-</td><td>D2+</td><td>D2-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D3+</td><td>D3-</td></tr> <tr><td>1</td><td>111</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td></tr> </tbody> </table>	PSWAP	DSWAP[2:0]	D0N	D0P	D1N	D1P	CKN	CKP	D2N	D2P	D3N	D3P	0	000	D2-	D2+	D1-	D1+	CLK-	CLK+	D0-	D0+	D3-	D3+	0	001	D2-	D2+	D0-	D0+	CLK-	CLK+	D1-	D1+	D3-	D3+	0	010	D3-	D3+	D1-	D1+	CLK-	CLK+	D0-	D0+	D2-	D2+	0	011	D3-	D3+	D0-	D0+	CLK-	CLK+	D1-	D1+	D2-	D2+	0	100	D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+	D0-	D0+	0	101	D3-	D3+	D1-	D1+	CLK-	CLK+	D2-	D2+	D0-	D0+	0	110	D0-	D0+	D2-	D2+	CLK-	CLK+	D1-	D1+	D3-	D3+	0	111	D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+	D3-	D3+	1	000	D2+	D2-	D1+	D1-	CLK+	CLK-	D0+	D0-	D3+	D3-	1	001	D2+	D2-	D0+	D0-	CLK+	CLK-	D1+	D1-	D3+	D3-	1	010	D3+	D3-	D1+	D1-	CLK+	CLK-	D0+	D0-	D2+	D2-	1	011	D3+	D3-	D0+	D0-	CLK+	CLK-	D1+	D1-	D2+	D2-	1	100	D3+	D3-	D2+	D2-	CLK+	CLK-	D1+	D1-	D0+	D0-	1	101	D3+	D3-	D1+	D1-	CLK+	CLK-	D2+	D2-	D0+	D0-	1	110	D0+	D0-	D2+	D2-	CLK+	CLK-	D1+	D1-	D3+	D3-	1	111	D0+	D0-	D1+	D1-	CLK+	CLK-	D2+	D2-	D3+	D3-
			PSWAP	DSWAP[2:0]	D0N	D0P	D1N	D1P	CKN	CKP	D2N	D2P	D3N	D3P																																																																																																																																																																																																	
0	000	D2-	D2+	D1-	D1+	CLK-	CLK+	D0-	D0+	D3-	D3+																																																																																																																																																																																																				
0	001	D2-	D2+	D0-	D0+	CLK-	CLK+	D1-	D1+	D3-	D3+																																																																																																																																																																																																				
0	010	D3-	D3+	D1-	D1+	CLK-	CLK+	D0-	D0+	D2-	D2+																																																																																																																																																																																																				
0	011	D3-	D3+	D0-	D0+	CLK-	CLK+	D1-	D1+	D2-	D2+																																																																																																																																																																																																				
0	100	D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+	D0-	D0+																																																																																																																																																																																																				
0	101	D3-	D3+	D1-	D1+	CLK-	CLK+	D2-	D2+	D0-	D0+																																																																																																																																																																																																				
0	110	D0-	D0+	D2-	D2+	CLK-	CLK+	D1-	D1+	D3-	D3+																																																																																																																																																																																																				
0	111	D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+	D3-	D3+																																																																																																																																																																																																				
1	000	D2+	D2-	D1+	D1-	CLK+	CLK-	D0+	D0-	D3+	D3-																																																																																																																																																																																																				
1	001	D2+	D2-	D0+	D0-	CLK+	CLK-	D1+	D1-	D3+	D3-																																																																																																																																																																																																				
1	010	D3+	D3-	D1+	D1-	CLK+	CLK-	D0+	D0-	D2+	D2-																																																																																																																																																																																																				
1	011	D3+	D3-	D0+	D0-	CLK+	CLK-	D1+	D1-	D2+	D2-																																																																																																																																																																																																				
1	100	D3+	D3-	D2+	D2-	CLK+	CLK-	D1+	D1-	D0+	D0-																																																																																																																																																																																																				
1	101	D3+	D3-	D1+	D1-	CLK+	CLK-	D2+	D2-	D0+	D0-																																																																																																																																																																																																				
1	110	D0+	D0-	D2+	D2-	CLK+	CLK-	D1+	D1-	D3+	D3-																																																																																																																																																																																																				
1	111	D0+	D0-	D1+	D1-	CLK+	CLK-	D2+	D2-	D3+	D3-																																																																																																																																																																																																				
42	DS1	Select for <b>LVDS</b> data lane sequence and polarity.	<table border="1"> <thead> <tr> <th>PSWAP</th> <th>DSWAP[2:0]</th> <th>D0N</th> <th>D0P</th> <th>D1N</th> <th>D1P</th> <th>CKN</th> <th>CKP</th> <th>D2N</th> <th>D2P</th> <th>D3N</th> <th>D3P</th> </tr> </thead> <tbody> <tr><td>0</td><td>000</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr> <tr><td>0</td><td>001</td><td>D3-</td><td>D3+</td><td>CLK-</td><td>CLK+</td><td>D2-</td><td>D2+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr> <tr><td>0</td><td>010</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td></tr> <tr><td>0</td><td>011</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td><td>CLK-</td><td>CLK+</td><td>D3-</td><td>D3+</td></tr> <tr><td>0</td><td>100</td><td>CLK-</td><td>CLK+</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td></tr> <tr><td>0</td><td>101</td><td>CLK-</td><td>CLK+</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr> <tr><td>0</td><td>110</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td><td>CLK-</td><td>CLK+</td></tr> <tr><td>0</td><td>111</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td><td>CLK-</td><td>CLK+</td></tr> <tr><td>1</td><td>000</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr> <tr><td>1</td><td>001</td><td>D3+</td><td>D3-</td><td>CLK+</td><td>CLK-</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr> <tr><td>1</td><td>010</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td></tr> <tr><td>1</td><td>011</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td><td>CLK+</td><td>CLK-</td><td>D3+</td><td>D3-</td></tr> <tr><td>1</td><td>100</td><td>CLK+</td><td>CLK-</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td></tr> <tr><td>1</td><td>101</td><td>CLK+</td><td>CLK-</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr> <tr><td>1</td><td>110</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td><td>CLK+</td><td>CLK-</td></tr> <tr><td>1</td><td>111</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td><td>CLK+</td><td>CLK-</td></tr> </tbody> </table>	PSWAP	DSWAP[2:0]	D0N	D0P	D1N	D1P	CKN	CKP	D2N	D2P	D3N	D3P	0	000	D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+	D0-	D0+	0	001	D3-	D3+	CLK-	CLK+	D2-	D2+	D1-	D1+	D0-	D0+	0	010	D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+	D3-	D3+	0	011	D0-	D0+	D1-	D1+	D2-	D2+	CLK-	CLK+	D3-	D3+	0	100	CLK-	CLK+	D0-	D0+	D1-	D1+	D2-	D2+	D3-	D3+	0	101	CLK-	CLK+	D3-	D3+	D2-	D2+	D1-	D1+	D0-	D0+	0	110	D3-	D3+	D2-	D2+	D1-	D1+	D0-	D0+	CLK-	CLK+	0	111	D0-	D0+	D1-	D1+	D2-	D2+	D3-	D3+	CLK-	CLK+	1	000	D3+	D3-	D2+	D2-	CLK+	CLK-	D1+	D1-	D0+	D0-	1	001	D3+	D3-	CLK+	CLK-	D2+	D2-	D1+	D1-	D0+	D0-	1	010	D0+	D0-	D1+	D1-	CLK+	CLK-	D2+	D2-	D3+	D3-	1	011	D0+	D0-	D1+	D1-	D2+	D2-	CLK+	CLK-	D3+	D3-	1	100	CLK+	CLK-	D0+	D0-	D1+	D1-	D2+	D2-	D3+	D3-	1	101	CLK+	CLK-	D3+	D3-	D2+	D2-	D1+	D1-	D0+	D0-	1	110	D3+	D3-	D2+	D2-	D1+	D1-	D0+	D0-	CLK+	CLK-	1	111	D0+	D0-	D1+	D1-	D2+	D2-	D3+	D3-	CLK+	CLK-
			PSWAP	DSWAP[2:0]	D0N	D0P	D1N	D1P	CKN	CKP	D2N	D2P	D3N	D3P																																																																																																																																																																																																	
0	000	D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+	D0-	D0+																																																																																																																																																																																																				
0	001	D3-	D3+	CLK-	CLK+	D2-	D2+	D1-	D1+	D0-	D0+																																																																																																																																																																																																				
0	010	D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+	D3-	D3+																																																																																																																																																																																																				
0	011	D0-	D0+	D1-	D1+	D2-	D2+	CLK-	CLK+	D3-	D3+																																																																																																																																																																																																				
0	100	CLK-	CLK+	D0-	D0+	D1-	D1+	D2-	D2+	D3-	D3+																																																																																																																																																																																																				
0	101	CLK-	CLK+	D3-	D3+	D2-	D2+	D1-	D1+	D0-	D0+																																																																																																																																																																																																				
0	110	D3-	D3+	D2-	D2+	D1-	D1+	D0-	D0+	CLK-	CLK+																																																																																																																																																																																																				
0	111	D0-	D0+	D1-	D1+	D2-	D2+	D3-	D3+	CLK-	CLK+																																																																																																																																																																																																				
1	000	D3+	D3-	D2+	D2-	CLK+	CLK-	D1+	D1-	D0+	D0-																																																																																																																																																																																																				
1	001	D3+	D3-	CLK+	CLK-	D2+	D2-	D1+	D1-	D0+	D0-																																																																																																																																																																																																				
1	010	D0+	D0-	D1+	D1-	CLK+	CLK-	D2+	D2-	D3+	D3-																																																																																																																																																																																																				
1	011	D0+	D0-	D1+	D1-	D2+	D2-	CLK+	CLK-	D3+	D3-																																																																																																																																																																																																				
1	100	CLK+	CLK-	D0+	D0-	D1+	D1-	D2+	D2-	D3+	D3-																																																																																																																																																																																																				
1	101	CLK+	CLK-	D3+	D3-	D2+	D2-	D1+	D1-	D0+	D0-																																																																																																																																																																																																				
1	110	D3+	D3-	D2+	D2-	D1+	D1-	D0+	D0-	CLK+	CLK-																																																																																																																																																																																																				
1	111	D0+	D0-	D1+	D1-	D2+	D2-	D3+	D3-	CLK+	CLK-																																																																																																																																																																																																				
43	DS0	Select for <b>LVDS</b> data lane sequence and polarity.	<table border="1"> <thead> <tr> <th>PSWAP</th> <th>DSWAP[2:0]</th> <th>D0N</th> <th>D0P</th> <th>D1N</th> <th>D1P</th> <th>CKN</th> <th>CKP</th> <th>D2N</th> <th>D2P</th> <th>D3N</th> <th>D3P</th> </tr> </thead> <tbody> <tr><td>0</td><td>000</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr> <tr><td>0</td><td>001</td><td>D3-</td><td>D3+</td><td>CLK-</td><td>CLK+</td><td>D2-</td><td>D2+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr> <tr><td>0</td><td>010</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td></tr> <tr><td>0</td><td>011</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td><td>CLK-</td><td>CLK+</td><td>D3-</td><td>D3+</td></tr> <tr><td>0</td><td>100</td><td>CLK-</td><td>CLK+</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td></tr> <tr><td>0</td><td>101</td><td>CLK-</td><td>CLK+</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr> <tr><td>0</td><td>110</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td><td>CLK-</td><td>CLK+</td></tr> <tr><td>0</td><td>111</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td><td>CLK-</td><td>CLK+</td></tr> <tr><td>1</td><td>000</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr> <tr><td>1</td><td>001</td><td>D3+</td><td>D3-</td><td>CLK+</td><td>CLK-</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr> <tr><td>1</td><td>010</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td></tr> <tr><td>1</td><td>011</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td><td>CLK+</td><td>CLK-</td><td>D3+</td><td>D3-</td></tr> <tr><td>1</td><td>100</td><td>CLK+</td><td>CLK-</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td></tr> <tr><td>1</td><td>101</td><td>CLK+</td><td>CLK-</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr> <tr><td>1</td><td>110</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td><td>CLK+</td><td>CLK-</td></tr> <tr><td>1</td><td>111</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td><td>CLK+</td><td>CLK-</td></tr> </tbody> </table>	PSWAP	DSWAP[2:0]	D0N	D0P	D1N	D1P	CKN	CKP	D2N	D2P	D3N	D3P	0	000	D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+	D0-	D0+	0	001	D3-	D3+	CLK-	CLK+	D2-	D2+	D1-	D1+	D0-	D0+	0	010	D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+	D3-	D3+	0	011	D0-	D0+	D1-	D1+	D2-	D2+	CLK-	CLK+	D3-	D3+	0	100	CLK-	CLK+	D0-	D0+	D1-	D1+	D2-	D2+	D3-	D3+	0	101	CLK-	CLK+	D3-	D3+	D2-	D2+	D1-	D1+	D0-	D0+	0	110	D3-	D3+	D2-	D2+	D1-	D1+	D0-	D0+	CLK-	CLK+	0	111	D0-	D0+	D1-	D1+	D2-	D2+	D3-	D3+	CLK-	CLK+	1	000	D3+	D3-	D2+	D2-	CLK+	CLK-	D1+	D1-	D0+	D0-	1	001	D3+	D3-	CLK+	CLK-	D2+	D2-	D1+	D1-	D0+	D0-	1	010	D0+	D0-	D1+	D1-	CLK+	CLK-	D2+	D2-	D3+	D3-	1	011	D0+	D0-	D1+	D1-	D2+	D2-	CLK+	CLK-	D3+	D3-	1	100	CLK+	CLK-	D0+	D0-	D1+	D1-	D2+	D2-	D3+	D3-	1	101	CLK+	CLK-	D3+	D3-	D2+	D2-	D1+	D1-	D0+	D0-	1	110	D3+	D3-	D2+	D2-	D1+	D1-	D0+	D0-	CLK+	CLK-	1	111	D0+	D0-	D1+	D1-	D2+	D2-	D3+	D3-	CLK+	CLK-
			PSWAP	DSWAP[2:0]	D0N	D0P	D1N	D1P	CKN	CKP	D2N	D2P	D3N	D3P																																																																																																																																																																																																	
0	000	D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+	D0-	D0+																																																																																																																																																																																																				
0	001	D3-	D3+	CLK-	CLK+	D2-	D2+	D1-	D1+	D0-	D0+																																																																																																																																																																																																				
0	010	D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+	D3-	D3+																																																																																																																																																																																																				
0	011	D0-	D0+	D1-	D1+	D2-	D2+	CLK-	CLK+	D3-	D3+																																																																																																																																																																																																				
0	100	CLK-	CLK+	D0-	D0+	D1-	D1+	D2-	D2+	D3-	D3+																																																																																																																																																																																																				
0	101	CLK-	CLK+	D3-	D3+	D2-	D2+	D1-	D1+	D0-	D0+																																																																																																																																																																																																				
0	110	D3-	D3+	D2-	D2+	D1-	D1+	D0-	D0+	CLK-	CLK+																																																																																																																																																																																																				
0	111	D0-	D0+	D1-	D1+	D2-	D2+	D3-	D3+	CLK-	CLK+																																																																																																																																																																																																				
1	000	D3+	D3-	D2+	D2-	CLK+	CLK-	D1+	D1-	D0+	D0-																																																																																																																																																																																																				
1	001	D3+	D3-	CLK+	CLK-	D2+	D2-	D1+	D1-	D0+	D0-																																																																																																																																																																																																				
1	010	D0+	D0-	D1+	D1-	CLK+	CLK-	D2+	D2-	D3+	D3-																																																																																																																																																																																																				
1	011	D0+	D0-	D1+	D1-	D2+	D2-	CLK+	CLK-	D3+	D3-																																																																																																																																																																																																				
1	100	CLK+	CLK-	D0+	D0-	D1+	D1-	D2+	D2-	D3+	D3-																																																																																																																																																																																																				
1	101	CLK+	CLK-	D3+	D3-	D2+	D2-	D1+	D1-	D0+	D0-																																																																																																																																																																																																				
1	110	D3+	D3-	D2+	D2-	D1+	D1-	D0+	D0-	CLK+	CLK-																																																																																																																																																																																																				
1	111	D0+	D0-	D1+	D1-	D2+	D2-	D3+	D3-	CLK+	CLK-																																																																																																																																																																																																				
44	PS		<table border="1"> <thead> <tr> <th>PSWAP</th> <th>DSWAP[2:0]</th> <th>D0N</th> <th>D0P</th> <th>D1N</th> <th>D1P</th> <th>CKN</th> <th>CKP</th> <th>D2N</th> <th>D2P</th> <th>D3N</th> <th>D3P</th> </tr> </thead> <tbody> <tr><td>0</td><td>000</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr> <tr><td>0</td><td>001</td><td>D3-</td><td>D3+</td><td>CLK-</td><td>CLK+</td><td>D2-</td><td>D2+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr> <tr><td>0</td><td>010</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td></tr> <tr><td>0</td><td>011</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td><td>CLK-</td><td>CLK+</td><td>D3-</td><td>D3+</td></tr> <tr><td>0</td><td>100</td><td>CLK-</td><td>CLK+</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td></tr> <tr><td>0</td><td>101</td><td>CLK-</td><td>CLK+</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr> <tr><td>0</td><td>110</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td><td>CLK-</td><td>CLK+</td></tr> <tr><td>0</td><td>111</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td><td>CLK-</td><td>CLK+</td></tr> <tr><td>1</td><td>000</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr> <tr><td>1</td><td>001</td><td>D3+</td><td>D3-</td><td>CLK+</td><td>CLK-</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr> <tr><td>1</td><td>010</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td></tr> <tr><td>1</td><td>011</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td><td>CLK+</td><td>CLK-</td><td>D3+</td><td>D3-</td></tr> <tr><td>1</td><td>100</td><td>CLK+</td><td>CLK-</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td></tr> <tr><td>1</td><td>101</td><td>CLK+</td><td>CLK-</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr> <tr><td>1</td><td>110</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td><td>CLK+</td><td>CLK-</td></tr> <tr><td>1</td><td>111</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td><td>CLK+</td><td>CLK-</td></tr> </tbody> </table>	PSWAP	DSWAP[2:0]	D0N	D0P	D1N	D1P	CKN	CKP	D2N	D2P	D3N	D3P	0	000	D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+	D0-	D0+	0	001	D3-	D3+	CLK-	CLK+	D2-	D2+	D1-	D1+	D0-	D0+	0	010	D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+	D3-	D3+	0	011	D0-	D0+	D1-	D1+	D2-	D2+	CLK-	CLK+	D3-	D3+	0	100	CLK-	CLK+	D0-	D0+	D1-	D1+	D2-	D2+	D3-	D3+	0	101	CLK-	CLK+	D3-	D3+	D2-	D2+	D1-	D1+	D0-	D0+	0	110	D3-	D3+	D2-	D2+	D1-	D1+	D0-	D0+	CLK-	CLK+	0	111	D0-	D0+	D1-	D1+	D2-	D2+	D3-	D3+	CLK-	CLK+	1	000	D3+	D3-	D2+	D2-	CLK+	CLK-	D1+	D1-	D0+	D0-	1	001	D3+	D3-	CLK+	CLK-	D2+	D2-	D1+	D1-	D0+	D0-	1	010	D0+	D0-	D1+	D1-	CLK+	CLK-	D2+	D2-	D3+	D3-	1	011	D0+	D0-	D1+	D1-	D2+	D2-	CLK+	CLK-	D3+	D3-	1	100	CLK+	CLK-	D0+	D0-	D1+	D1-	D2+	D2-	D3+	D3-	1	101	CLK+	CLK-	D3+	D3-	D2+	D2-	D1+	D1-	D0+	D0-	1	110	D3+	D3-	D2+	D2-	D1+	D1-	D0+	D0-	CLK+	CLK-	1	111	D0+	D0-	D1+	D1-	D2+	D2-	D3+	D3-	CLK+	CLK-
			PSWAP	DSWAP[2:0]	D0N	D0P	D1N	D1P	CKN	CKP	D2N	D2P	D3N	D3P																																																																																																																																																																																																	
			0	000	D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+	D0-	D0+																																																																																																																																																																																																	
			0	001	D3-	D3+	CLK-	CLK+	D2-	D2+	D1-	D1+	D0-	D0+																																																																																																																																																																																																	
			0	010	D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+	D3-	D3+																																																																																																																																																																																																	
			0	011	D0-	D0+	D1-	D1+	D2-	D2+	CLK-	CLK+	D3-	D3+																																																																																																																																																																																																	
			0	100	CLK-	CLK+	D0-	D0+	D1-	D1+	D2-	D2+	D3-	D3+																																																																																																																																																																																																	
			0	101	CLK-	CLK+	D3-	D3+	D2-	D2+	D1-	D1+	D0-	D0+																																																																																																																																																																																																	
			0	110	D3-	D3+	D2-	D2+	D1-	D1+	D0-	D0+	CLK-	CLK+																																																																																																																																																																																																	
			0	111	D0-	D0+	D1-	D1+	D2-	D2+	D3-	D3+	CLK-	CLK+																																																																																																																																																																																																	
			1	000	D3+	D3-	D2+	D2-	CLK+	CLK-	D1+	D1-	D0+	D0-																																																																																																																																																																																																	
			1	001	D3+	D3-	CLK+	CLK-	D2+	D2-	D1+	D1-	D0+	D0-																																																																																																																																																																																																	
1	010	D0+	D0-	D1+	D1-	CLK+	CLK-	D2+	D2-	D3+	D3-																																																																																																																																																																																																				
1	011	D0+	D0-	D1+	D1-	D2+	D2-	CLK+	CLK-	D3+	D3-																																																																																																																																																																																																				
1	100	CLK+	CLK-	D0+	D0-	D1+	D1-	D2+	D2-	D3+	D3-																																																																																																																																																																																																				
1	101	CLK+	CLK-	D3+	D3-	D2+	D2-	D1+	D1-	D0+	D0-																																																																																																																																																																																																				
1	110	D3+	D3-	D2+	D2-	D1+	D1-	D0+	D0-	CLK+	CLK-																																																																																																																																																																																																				
1	111	D0+	D0-	D1+	D1-	D2+	D2-	D3+	D3-	CLK+	CLK-																																																																																																																																																																																																				
45	GND	Ground																																																																																																																																																																																																													
46	D0N	Data differential signal input pins																																																																																																																																																																																																													
47	D0P	Data differential signal input pins																																																																																																																																																																																																													
48	D1N	Data differential signal input pins																																																																																																																																																																																																													
49	D1P	Data differential signal input pins																																																																																																																																																																																																													
50	CKN	CLOCK differential signal input pins																																																																																																																																																																																																													
51	CKP	CLOCK differential signal input pins																																																																																																																																																																																																													
52	D2N	Data differential signal input pins																																																																																																																																																																																																													
53	D2P	Data differential signal input pins																																																																																																																																																																																																													
54	D3N	Data differential signal input pins																																																																																																																																																																																																													
55	D3P	Data differential signal input pins																																																																																																																																																																																																													
56	IOVCC	power supply																																																																																																																																																																																																													
57	AVDD	Input positive power from system/ external power IC																																																																																																																																																																																																													
58	AVEE	Input negative power from system/ external power IC																																																																																																																																																																																																													

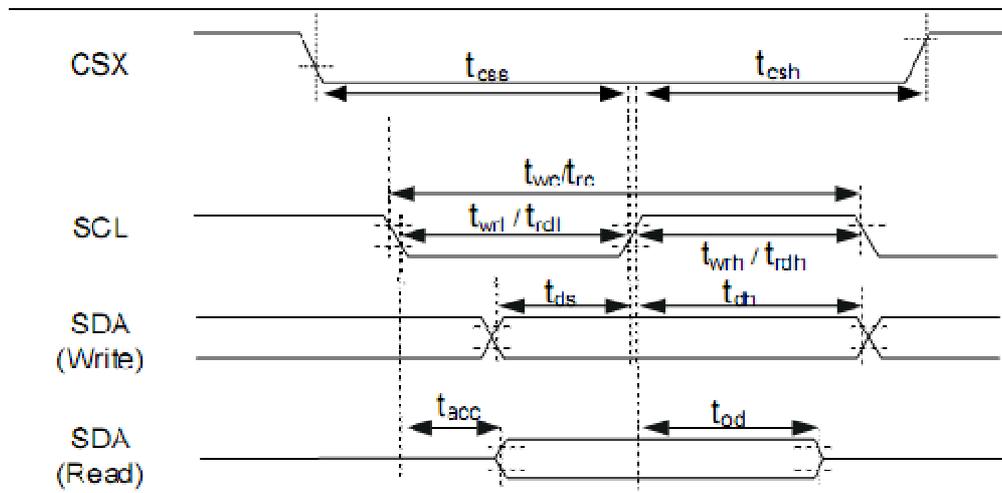
59	VPP	External High voltage pin is used in OTP program mode, the power is operate at 7.8V.If not used, let them open
60	GND	Ground

## BACKLIGHT UNIT PIN:

No.	Symbol	Function
1	NC	No connection
2	A	LED Anode
3	K1	LED Cathode
4	K2	LED Cathode
5	K3	LED Cathode
6	K4	LED Cathode
7	K5	LED Cathode
8	K6	LED Cathode
9	K7	LED Cathode
10	NC	No connection

9. AC Characteristics

9.1. 3-Wire SPI Interface Timing



SPI interface AC characteristics

( $T_A=25^{\circ}C$ , IOVCC=3.3V, VCI=3.3V)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	$t_{oss}$	Chp select setup time (Write)	40	-	ns	-
	$t_{csh}$	Chp select setup time (Read)	40	-	ns	
SCL (Write)	$t_{wc}$	Write cycle	100	-	ns	-
	$t_{wrh}$	Control pulse "H" duration	40	-	ns	
	$t_{wrl}$	Control pulse "L" duration	40	-	ns	
SCL (Read)	$t_{rc}$	Read cycle	150	-	ns	-
	$t_{rdh}$	Control pulse "H" duration	60	-	ns	
	$t_{rdl}$	Control pulse "L" duration	60	-	ns	
SDA (Write)	$t_{ds}$	Data setup time	30	-	ns	Ncte <sup>(1)</sup>
	$t_{dh}$	Data hold time	30	-	ns	
SDA (Read)	$t_{acc}$	Read access time	-	35	ns	
	$t_{od}$	Output disable time	10	50	ns	

Note: (1) For maximum  $C_i=30pF$ , for minimum  $C_i=8pF$ .

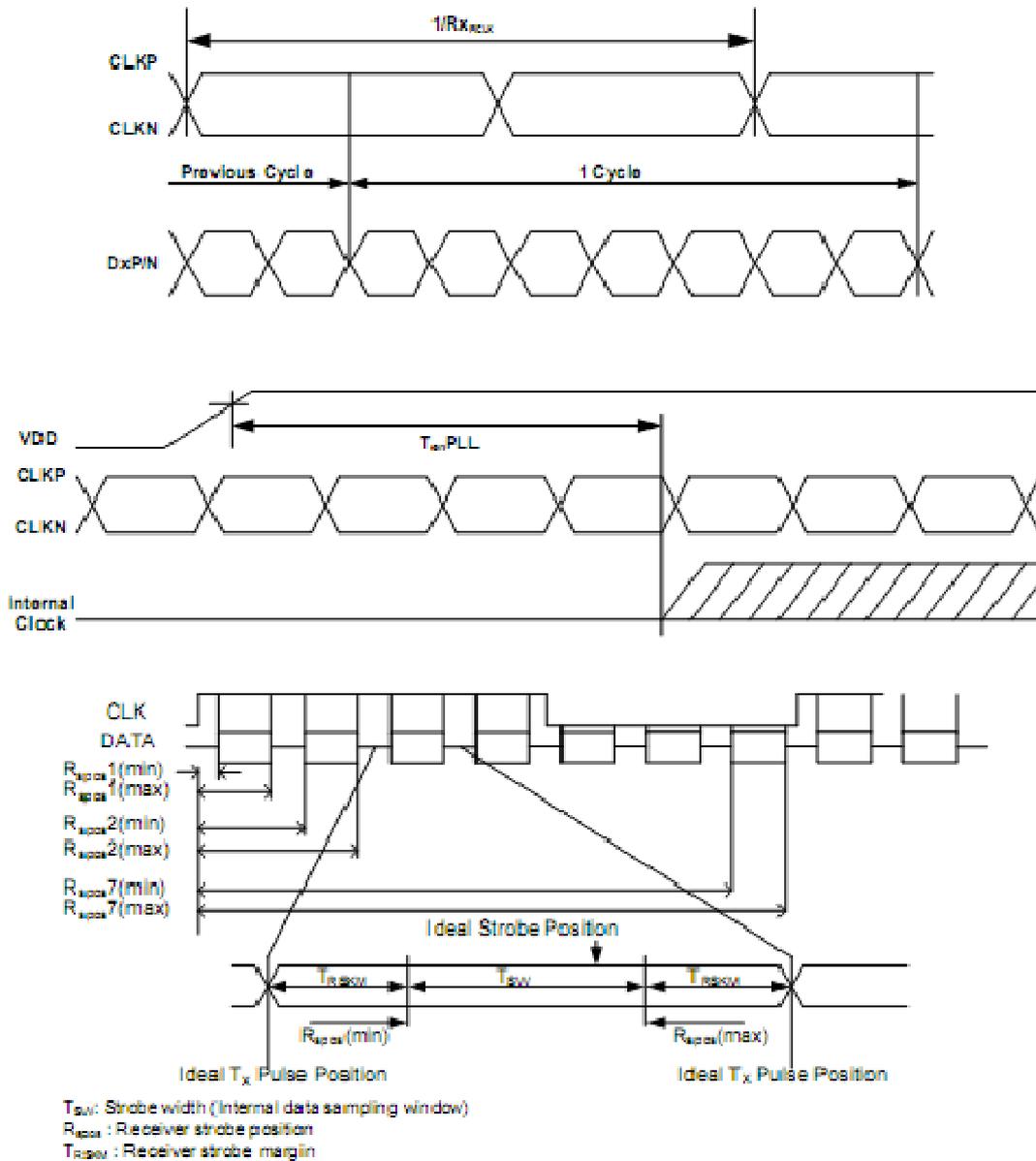
(2) The input signal rise time and fall time ( $t_r$ ,  $t_f$ ) is specified at 15 ns or less.

(3) Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

SPI interface AC characteristics

9.2. LVDS Interface

9.2.1. LVDS Electronic Characteristic

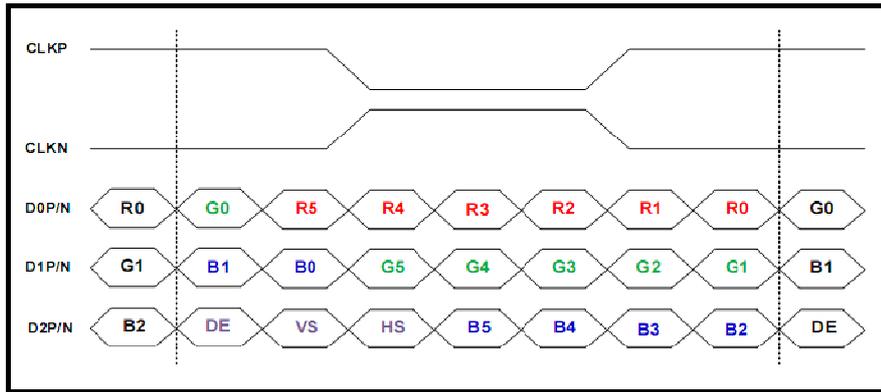


LVDS AC characteristics

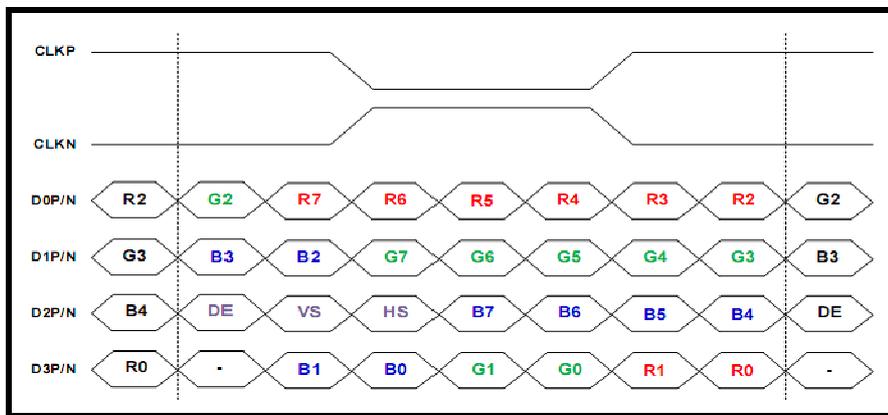
Signal	Symbol	Min.	Typ	Max.	Unit	Description
Clock frequency	$R_{xCLK}$	30	-	75	MHz	-
Input data skew margin	$T_{Rskw}$	500	-	-	ps	$ VID  = 200mV$ $RxVCM = 1.2V$ $@R_{xCLK} = 75MHz$
Clock high time	$T_{LVEH}$	-	$4/(7 \times R_{xCLK})$	-	ns	-
Clock low time	$T_{LVEL}$	-	$3/(7 \times R_{xCLK})$	-	ns	-
PLL wake-up time	$T_{skw,PLL}$	-	-	150	us	-

LVDS AC characteristics

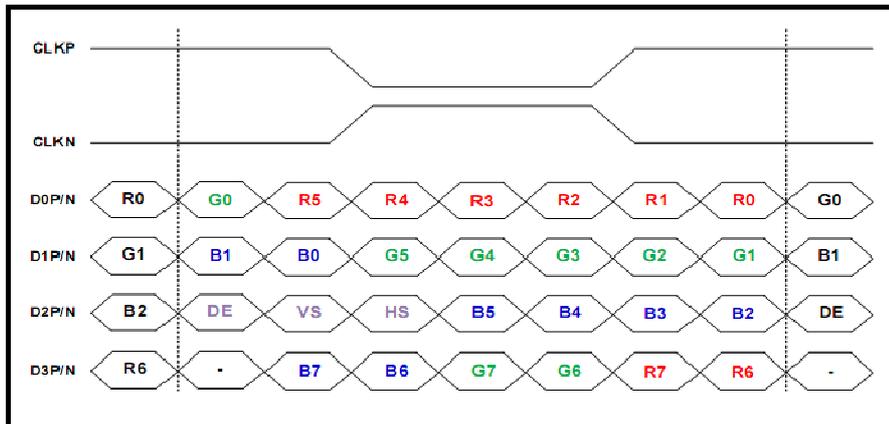
9.2.2. LVDS Data Format



6-bit LVDS input ( IM[1:0]=01, LANSEL[1:0]=10, LVFMT=Don't care )



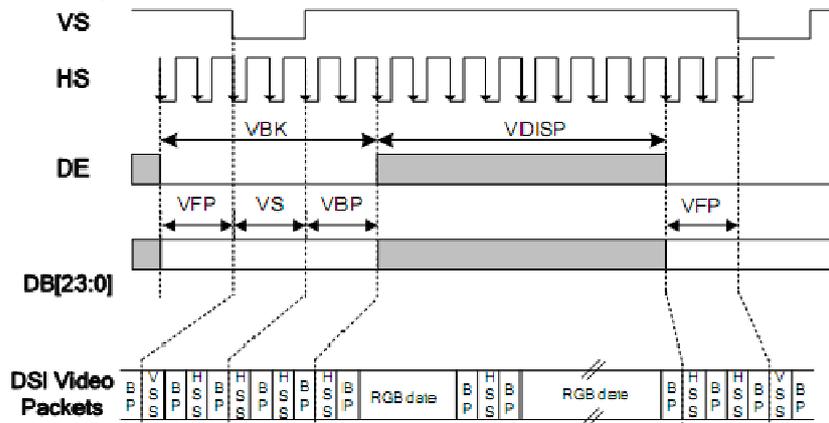
8-bit LVDS input ( IM[1:0]=01, LANSEL[1:0]=11, LVFMT=1(JEIDA) )



8-bit LVDS input ( IM[1:0]=01, LANSEL[1:0]=11, LVFMT=0(VESA) )

9.3. RGB Interface Timing

Vertical Timings



Vertical Timings for DPI I/F

Resolution=800x480 (T<sub>A</sub>=25°C, IOVCC=3.3V, VCI=3.3V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	-	2	-	Note <sup>(1)</sup>	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note <sup>(1)</sup>	Line
Vertical blanking period	VBK	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	480	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse must be set at corresponding position for LCD normal display.

Horizontal Timings

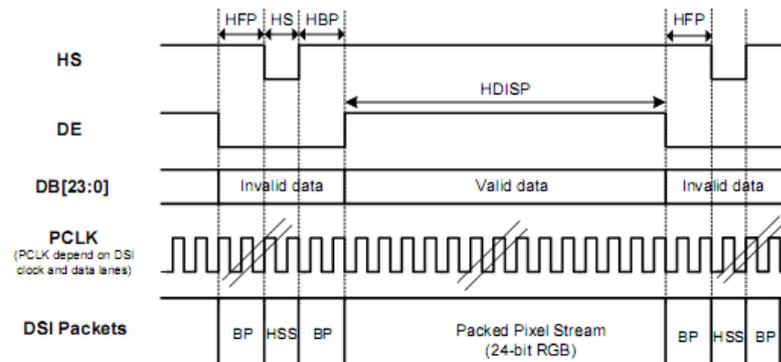


Figure 11.13: Horizontal Timing for DSI Video mode I/F

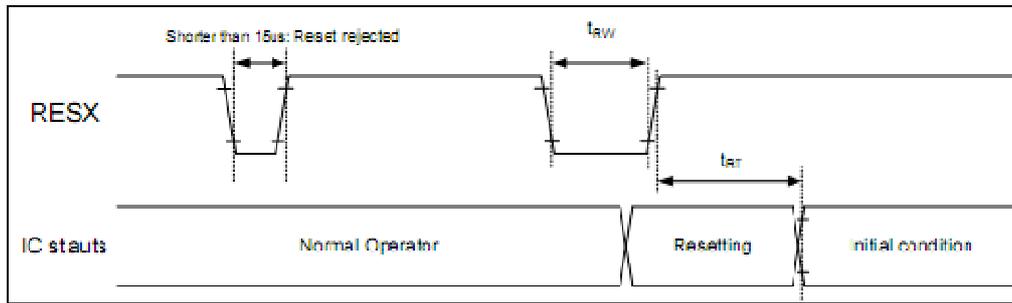
RGB Resolution=800x480 (T<sub>A</sub>=25°C, VCCH=IOVCC=3.3V, VCI=3.3V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	100			ns
Horizontal back porch	HBP	-	100			ns
Horizontal front porch	HFP	-	400			ns
Horizontal blanking period	HBLK	HS+HBP+HFP		900 <sup>(1)</sup>		ns
Horizontal active area	HDISP	640 pixels	-	12 <sup>(2)</sup>	-	us

Note:

- Below time limitation will apply in all DSI speed range.
  - HS+HBP >= 500ns.
  - HFP >= 400ns.
- Base on frame rate = 60HZ,
  - VS=2, VBP=2 and VFP=2.

9.4. Reset Timing



Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
$t_{RW}$	Reset 'L' pulse width <sup>(2)</sup>	RESX	20	-	us
$t_{RT}$	Reset complete time <sup>(3)</sup>	-	-	5 <sup>(5)</sup>	ms
		-	-	120 <sup>(6)</sup> (7) (8)	ms

Note:

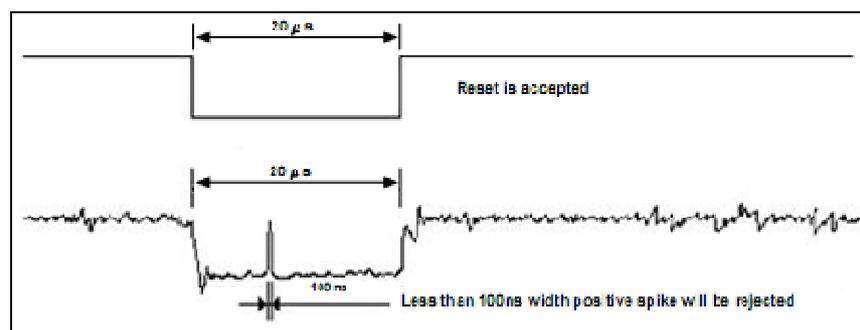
(1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset complete time ( $t_{RT}$ ) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 15 $\mu$ s	Reset Rejected
Longer than 20 $\mu$ s	Reset
Between 15 $\mu$ s and 20 $\mu$ s	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode) and then returns to Default condition for HW reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



Reset timings

(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out command, it is necessary to wait 120msec then send RESX.

## **10. Quality Assurance**

### **10.1.Purpose**

This standard for Quality Assurance assures the quality of LCD module products supplied to customer.

### **10.2.Standard for Quality Test**

#### 10.2.1. Sampling Plan:

GB2828.1-2012

Single sampling, general inspection level II

#### 10.2.2. Sampling Criteria:

Visual inspection: AQL 1.5.

Electrical functional: AQL 0.65.

#### 10.2.3. Reliability Test:

Detailed requirement refer to Reliability Test Specification.

### **10.3.Nonconforming Analysis & Disposition**

#### 10.3.1. Nonconforming analysis:

10.3.1.1. Customer should provide overall information of non-conforming sample for their complaints.

10.3.1.2. After receipt of detailed information from customer, the analysis of nonconforming parts usually should be finished in one week.

10.3.1.3. If cannot finish the analysis on time, customer will be notified with the progress status.

#### 10.3.2. Disposition of nonconforming:

10.3.2.1. Non-conforming product over PPM level will be replaced.

10.3.2.2. The cause of non-conformance will be analyzed. Corrective action will be discussed and implemented.

### **10.4.Agreement Items**

Shall negotiate with customer if the following situation occurs:

10.4.1. There is any discrepancy in standard of quality assurance.

10.4.2. Additional requirement to be added in product specification.

10.4.3. Any other special problem.

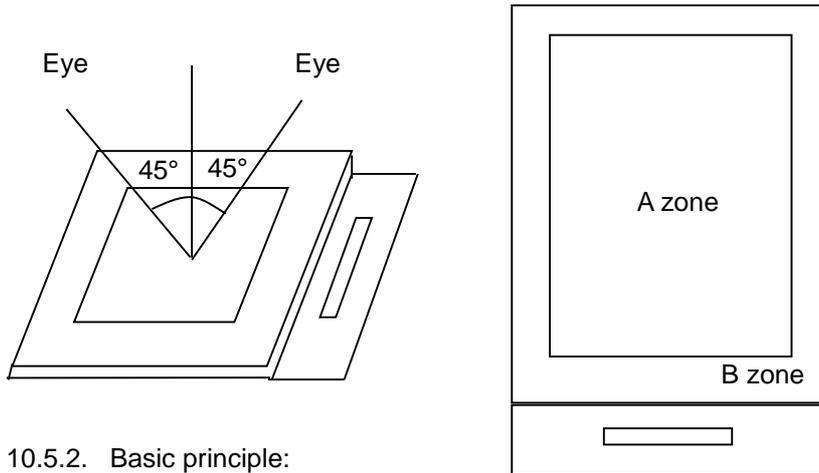
### **10.5.Standard of the Product Visual Inspection**

#### 10.5.1. Appearance inspection:

10.5.1.1. The inspection must be under illumination about 1000 – 1500 lx, and the distance of view must be at 30cm ± 2cm .

10.5.1.2. The viewing angle should be 45° from the vertical line without reflection light or follows customer's viewing angle specifications.

10.5.1.3. Definition of area: A Zone: Active Area, B Zone: Viewing Area,



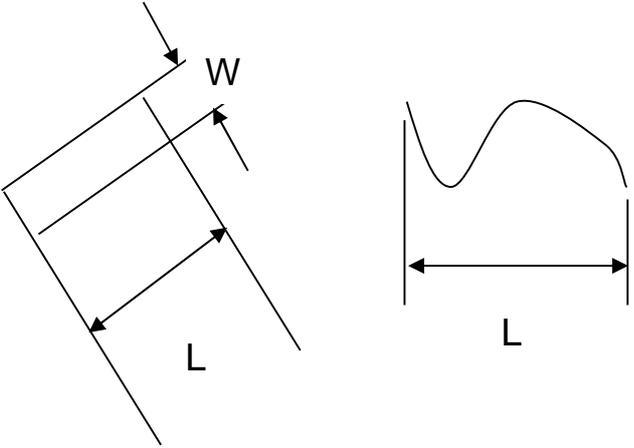
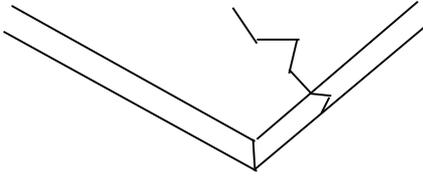
10.5.2. Basic principle:

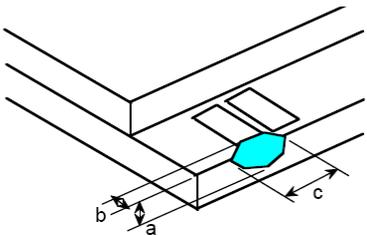
10.5.2.1. A set of sample to indicate the limit of acceptable quality level must be discussed by both us and customer when there is any dispute happened.

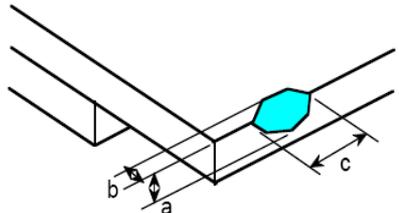
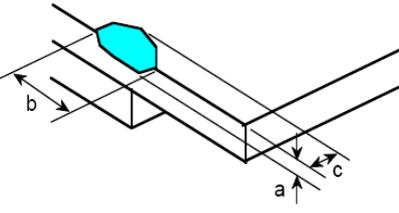
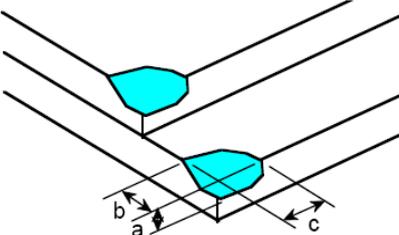
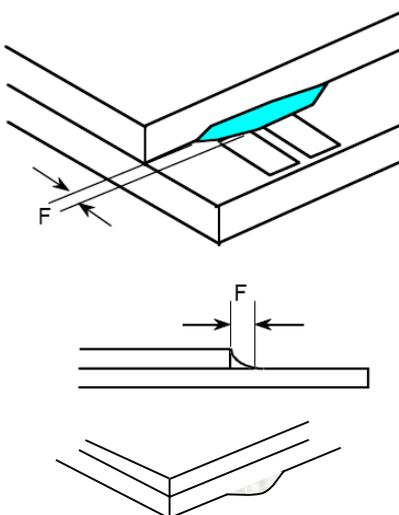
10.5.2.2. New item must be added on time when it is necessary.

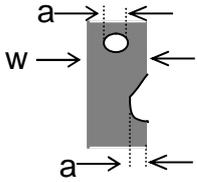
10.6. Inspection Specification

No.	Item	Criteria (Unit: mm)																		
01	Black / White spot Foreign material (Round type) Pinholes Stain Particles inside cell. (Minor defect)	<p><math>\phi = (a + b) / 2</math>                      Distance between 2 defects should more than 5mm apart.</p> <table border="1"> <thead> <tr> <th>Size</th> <th>Area</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>\phi \leq 0.20</math></td> <td></td> <td>Ignore</td> </tr> <tr> <td><math>0.20 &lt; \phi \leq 0.50</math></td> <td></td> <td><math>N \leq 3</math></td> </tr> <tr> <td><math>0.50 &lt; \phi</math></td> <td></td> <td>0</td> </tr> </tbody> </table>	Size	Area	Acc. Qty	$\phi \leq 0.20$		Ignore	$0.20 < \phi \leq 0.50$		$N \leq 3$	$0.50 < \phi$		0						
Size	Area	Acc. Qty																		
$\phi \leq 0.20$		Ignore																		
$0.20 < \phi \leq 0.50$		$N \leq 3$																		
$0.50 < \phi$		0																		
02	Electrical Defect (Minor defect)	<table border="1"> <thead> <tr> <th>Bright dot</th> <th>Display Area</th> <th>Total</th> <th rowspan="3">Note1</th> </tr> </thead> <tbody> <tr> <td></td> <td><math>N \leq 2</math></td> <td><math>N \leq 2</math></td> </tr> <tr> <td>Dark dot</td> <td><math>N \leq 4</math></td> <td><math>N \leq 4</math></td> </tr> <tr> <td>Total dot</td> <td><math>N \leq 4</math></td> <td><math>N \leq 4</math></td> <td></td> </tr> <tr> <td>Mura</td> <td colspan="2">Not visible through 5% ND filters.</td> <td>Note 2</td> </tr> </tbody> </table> <p>Remark:                      1. Bright dot caused by scratch and foreign object accords to item 1.</p>	Bright dot	Display Area	Total	Note1		$N \leq 2$	$N \leq 2$	Dark dot	$N \leq 4$	$N \leq 4$	Total dot	$N \leq 4$	$N \leq 4$		Mura	Not visible through 5% ND filters.		Note 2
Bright dot	Display Area	Total	Note1																	
	$N \leq 2$	$N \leq 2$																		
Dark dot	$N \leq 4$	$N \leq 4$																		
Total dot	$N \leq 4$	$N \leq 4$																		
Mura	Not visible through 5% ND filters.		Note 2																	

<p>03</p>	<p>Black and White line Scratch Foreign material (Line type) (Minor defect)</p>	 <table border="1" data-bbox="566 721 1193 985"> <thead> <tr> <th>Length</th> <th>Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td>/</td> <td><math>W \leq 0.1</math></td> <td>Ignore</td> </tr> <tr> <td><math>L \leq 2.5</math></td> <td><math>0.1 &lt; W \leq 0.2</math></td> <td>3</td> </tr> <tr> <td><math>L &gt; 2.5</math></td> <td><math>0.2 &lt; W</math></td> <td>0</td> </tr> <tr> <td colspan="2">Total</td> <td>3</td> </tr> </tbody> </table> <p>Distance between 2 defects should more than 3mm apart. Scratches not viewable through the back of the display are acceptable.</p>	Length	Width	Acc. Qty	/	$W \leq 0.1$	Ignore	$L \leq 2.5$	$0.1 < W \leq 0.2$	3	$L > 2.5$	$0.2 < W$	0	Total		3
Length	Width	Acc. Qty															
/	$W \leq 0.1$	Ignore															
$L \leq 2.5$	$0.1 < W \leq 0.2$	3															
$L > 2.5$	$0.2 < W$	0															
Total		3															
<p>04</p>	<p>Glass Crack (Minor defect)</p>	 <p>Crack is potential to enlarge, any type is not allowed.</p>															

<p>05</p>	<p>Glass Chipping Pad Area: (Minor defect)</p> 	<table border="1" data-bbox="869 1608 1340 1787"> <thead> <tr> <th>Length and Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>c &gt; 3.0, b &lt; 1.0</math></td> <td>1</td> </tr> <tr> <td><math>c &lt; 3.0, b &lt; 1.0</math></td> <td>3</td> </tr> <tr> <td colspan="2"><math>a &lt; \text{Glass Thickness}</math></td> </tr> </tbody> </table>	Length and Width	Acc. Qty	$c > 3.0, b < 1.0$	1	$c < 3.0, b < 1.0$	3	$a < \text{Glass Thickness}$	
Length and Width	Acc. Qty									
$c > 3.0, b < 1.0$	1									
$c < 3.0, b < 1.0$	3									
$a < \text{Glass Thickness}$										

<p>06</p>	<p>Glass Chipping Rear of Pad Area: (Minor defect)</p> 	<table border="1"> <thead> <tr> <th>Length and Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>c &gt; 3.0, b &lt; 1.0</math></td> <td>1</td> </tr> <tr> <td><math>c &lt; 3.0, b &lt; 1.0</math></td> <td>2</td> </tr> <tr> <td><math>c &lt; 3.0, b &lt; 0.5</math></td> <td>4</td> </tr> <tr> <td colspan="2" style="text-align: center;"><math>a &lt; \text{Glass Thickness}</math></td> </tr> </tbody> </table>	Length and Width	Acc. Qty	$c > 3.0, b < 1.0$	1	$c < 3.0, b < 1.0$	2	$c < 3.0, b < 0.5$	4	$a < \text{Glass Thickness}$	
Length and Width	Acc. Qty											
$c > 3.0, b < 1.0$	1											
$c < 3.0, b < 1.0$	2											
$c < 3.0, b < 0.5$	4											
$a < \text{Glass Thickness}$												
<p>07</p>	<p>Glass Chipping Except Pad Area: (Minor defect)</p> 	<table border="1"> <thead> <tr> <th>Length and Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>c &gt; 3.0, b &lt; 1.0</math></td> <td>1</td> </tr> <tr> <td><math>c &lt; 3.0, b &lt; 1.0</math></td> <td>2</td> </tr> <tr> <td><math>c &lt; 3.0, b &lt; 0.5</math></td> <td>4</td> </tr> <tr> <td colspan="2" style="text-align: center;"><math>a &lt; \text{Glass Thickness}</math></td> </tr> </tbody> </table>	Length and Width	Acc. Qty	$c > 3.0, b < 1.0$	1	$c < 3.0, b < 1.0$	2	$c < 3.0, b < 0.5$	4	$a < \text{Glass Thickness}$	
Length and Width	Acc. Qty											
$c > 3.0, b < 1.0$	1											
$c < 3.0, b < 1.0$	2											
$c < 3.0, b < 0.5$	4											
$a < \text{Glass Thickness}$												
<p>08</p>	<p>Glass Corner Chipping: (Minor defect)</p> 	<table border="1"> <thead> <tr> <th>Length and Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>c &lt; 3.0, b &lt; 3.0</math></td> <td>Ignore</td> </tr> <tr> <td colspan="2" style="text-align: center;"><math>a &lt; \text{Glass Thickness}</math></td> </tr> </tbody> </table>	Length and Width	Acc. Qty	$c < 3.0, b < 3.0$	Ignore	$a < \text{Glass Thickness}$					
Length and Width	Acc. Qty											
$c < 3.0, b < 3.0$	Ignore											
$a < \text{Glass Thickness}$												
<p>09</p>	<p>Glass Burr: (Minor defect)</p> 	<table border="1"> <thead> <tr> <th>Length</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>F &lt; 1.0</math></td> <td>Ignore</td> </tr> </tbody> </table> <p>Glass burr don't affect assemble and module dimension.</p>	Length	Acc. Qty	$F < 1.0$	Ignore						
Length	Acc. Qty											
$F < 1.0$	Ignore											

10	<p>FPC Defect: (Minor defect)</p> 	<p>10.1 Dent, pinhole width <math>a &lt; w/3</math>. (w: circuitry width.) 10.2 Open circuit is unacceptable. 10.3 No oxidation, contamination and distortion.</p>								
11	<p>Bubble on Polarizer (Minor defect)</p>	<table border="1" data-bbox="743 566 1214 741"> <thead> <tr> <th>Diameter</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>\phi \leq 0.30</math></td> <td>Ignore</td> </tr> <tr> <td><math>0.30 &lt; \phi \leq 0.50</math></td> <td><math>N \leq 2</math></td> </tr> <tr> <td><math>0.50 &lt; \phi</math></td> <td><math>N = 0</math></td> </tr> </tbody> </table>	Diameter	Acc. Qty	$\phi \leq 0.30$	Ignore	$0.30 < \phi \leq 0.50$	$N \leq 2$	$0.50 < \phi$	$N = 0$
Diameter	Acc. Qty									
$\phi \leq 0.30$	Ignore									
$0.30 < \phi \leq 0.50$	$N \leq 2$									
$0.50 < \phi$	$N = 0$									
12	<p>Dent on Polarizer (Minor defect)</p>	<table border="1" data-bbox="743 842 1214 1016"> <thead> <tr> <th>Diameter</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>\phi \leq 0.25</math></td> <td>Ignore</td> </tr> <tr> <td><math>0.25 &lt; \phi \leq 0.50</math></td> <td><math>N \leq 4</math></td> </tr> <tr> <td><math>0.50 &lt; \phi</math></td> <td>None</td> </tr> </tbody> </table>	Diameter	Acc. Qty	$\phi \leq 0.25$	Ignore	$0.25 < \phi \leq 0.50$	$N \leq 4$	$0.50 < \phi$	None
Diameter	Acc. Qty									
$\phi \leq 0.25$	Ignore									
$0.25 < \phi \leq 0.50$	$N \leq 4$									
$0.50 < \phi$	None									
13	<p>Bezel</p>	<p>13.1 No rust, distortion on the Bezel. 13.2 No visible fingerprints, stains or other contamination.</p>								
14	<p>PCB</p>	<p>14.1 No distortion or contamination on PCB terminals. 14.2 All components on PCB must same as documented on the BOM/component layout. 14.3 Follow IPC-A-600F.</p>								
15	<p>Soldering</p>	<p>Follow IPC-A-610C standard</p>								
16	<p>Electrical Defect (Major defect)</p>	<p>The below defects must be rejected. 16.1 Missing vertical / horizontal segment, 16.2 Abnormal Display. 16.3 No function or no display. 16.4 Current exceeds product specifications. 16.5 LCD viewing angle defect. 16.6 No Backlight. 16.7 Dark Backlight. 16.8 Touch Panel no function.</p>								

Remark: LCD Panel Broken shall be rejected. Defect out of LCD viewing area is acceptable.

**10.7. Classification of Defects**

- 10.7.1. Visual defects (Except no / wrong label) are treated as minor defect and electrical defect is major.
- 10.7.2. Two minor defects are equal to one major in lot sampling inspection.

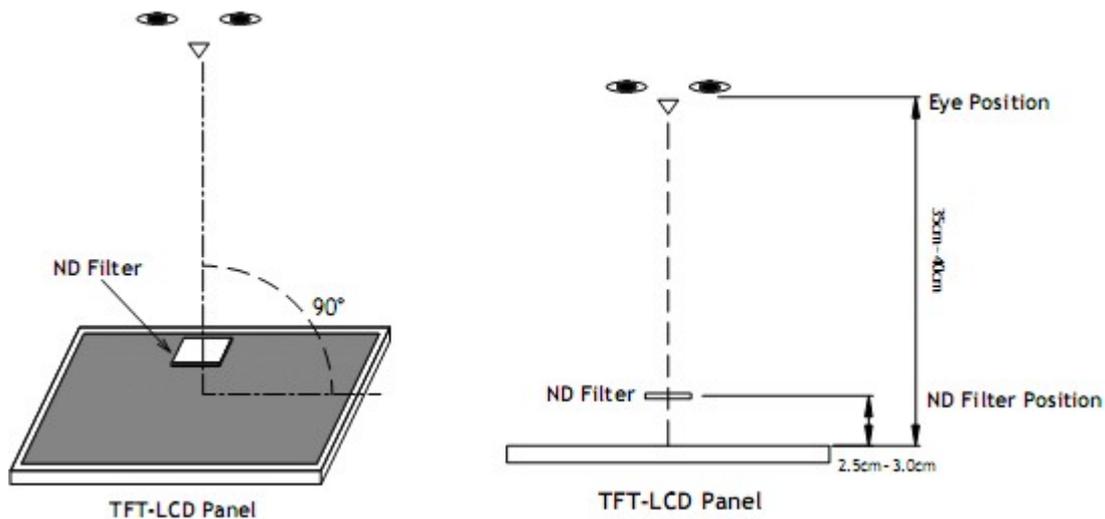
**10.8. Identification/marketing criteria**

Any unit with illegible / wrong /double or no marking/ label shall be rejected.

**10.9. Packing**

- 10.9.1. There should be no damage of the outside carton box, each packaging box should have one identical label.
- 10.9.2. Modules inside package box should have compliant mark.
- 10.9.3. All direct package materials shall offer ESD protection.

**Note1:** Bright dot is defined as the defective area of the dot is larger than 50% of one sub-pixel area.



Bright dot: The bright dot size defect at black display pattern. It can be recognized by 2% transparency of filter when the distance between eyes and panel is 350mm± 50mm.

Dark dot: Cyan, Magenta or Yellow dot size defect at white display pattern. It can be recognized by 5% transparency of filter when the distance between eyes and panel is 350mm± 50mm.

**Note2:** Mura on display which appears darker / brighter against background brightness on parts of display area.

**11. Reliability Specification**

No	Item	Condition	Quantity	Criteria
1	High Temperature Operating	+70°C, 96Hrs	2	GB/T2423.2-2008
2	Low Temperature Operating	-20°C, 96Hrs	2	GB/T2423.1-2008
3	High Humidity Storage	+50°C, 90%RH, 96Hrs	2	GB/T2423.3-2016
4	High Temperature Storage	+80°C, 96Hrs	2	GB/T2423.2-2008
5	Low Temperature Storage	-30°C, 96Hrs	2	GB/T2423.1-2008
6	Thermal Cycling Test Storage	-20°C, 60min ~ +70°C, 60min, 20 cycles.	2	GB/T2423.22-2012
7	Packing vibration	Frequency range:10Hz~50Hz Acceleration of gravity: 5G X, Y, Z 30 min for each direction.	-	GB/T5170.14-2009
8	Electrical Static Discharge	Air: ± 4kV 150pF/330 Ω 5 times	2	GB/T17626.2-2018
		Contact: ± 2kV 150pF/330 Ω 5 times		
9	Drop Test (Packaged)	Height:80 cm,1 corner, 3 edges, 6 surfaces.	-	GB/T2423.7-2018

Note1. No deflection cosmetic and operational function allowable.

Note2. Total current Consumption should be below double of initial value

**12. Precautions and Warranty**

**12.1.Safety**

- 12.1.1. The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.
- 12.1.2. Since the liquid crystal cells are made of glass, do not apply strong impact on them. Handle with care.

**12.2.Handling**

- 12.2.1. Reverse and use within ratings in order to keep performance and prevent damage.
- 12.2.2. Do not wipe the polarizer with dry cloth, as it might cause scratch. If the surface of the LCD needs to be cleaned, wipe it swiftly with cotton or other soft cloth soaked with petroleum IPA, do not use other chemicals.

**12.3.Storage**

- 12.3.1. Do not store the LCD module beyond the specified temperature ranges.
- 12.3.2. Strong light exposure causes degradation of polarizer and color filter.

**12.4.Metal Pin (Apply to Products with Metal Pins)**

12.4.1. Pins of LCD and Backlight

12.4.1.1. Solder tip can touch and press on the tip of Pin LEAD during the soldering

12.4.1.2. Recommended Soldering Conditions

Solder Type: Sn96.3~94-Ag3.3~4.3-Cu0.4~1.1

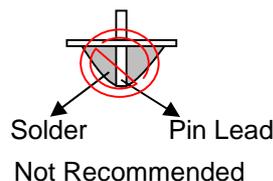
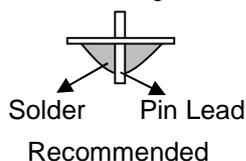
Maximum Solder Temperature: 370°C

Maximum Solder Time: 3s at the maximum temperature

Recommended Soldering Temp: 350±20°C

Typical Soldering Time: ≤3s

12.4.1.3. Solder Wetting



12.4.2. Pins of EL

12.4.2.1. Solder tip can touch and press on the tip of EL leads during soldering.

12.4.2.2. No Solder Paste on the soldering pad on the motherboard is recommended.

12.4.2.3. Recommended Soldering Conditions

Solder type: Nippon Alimit Leadfree SR-34, size 0.5mm

Recommended Solder Temperature: 270~290°C

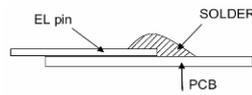
Typical Soldering Time: ≤2s

Minimum solder distance from EL lamp (body):2.0mm

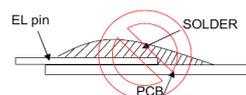
12.4.2.4. No horizontal press on the EL leads during soldering.

12.4.2.5. 180° bend EL leads three times is not allowed.

12.4.2.6. Solder Wetting

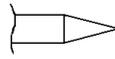


Recommended

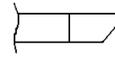


Not Recommended

12.4.2.7. The type of the solder iron:

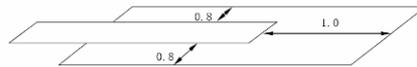


Recommended



Not Recommended

12.4.2.8. Solder Pad



**12.5.Operation**

- 12.5.1. Do not drive LCD with DC voltage
- 12.5.2. Response time will increase below lower temperature
- 12.5.3. Display may change color with different temperature
- 12.5.4. Mechanical disturbance during operation, such as pressing on the display area, may cause the segments to appear “fractured”.
- 12.5.5. Do not connect or disconnect the LCM to or from the system when power is on.
- 12.5.6. Never use the LCM under abnormal condition of high temperature and high humidity.
- 12.5.7. Module has high frequency circuits. Sufficient suppression to the electromagnetic interface shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- 12.5.8. *Do not display the fixed pattern for long time (we suggest the time not longer than one hour) because it will develop image sticking due to the TFT structure.*

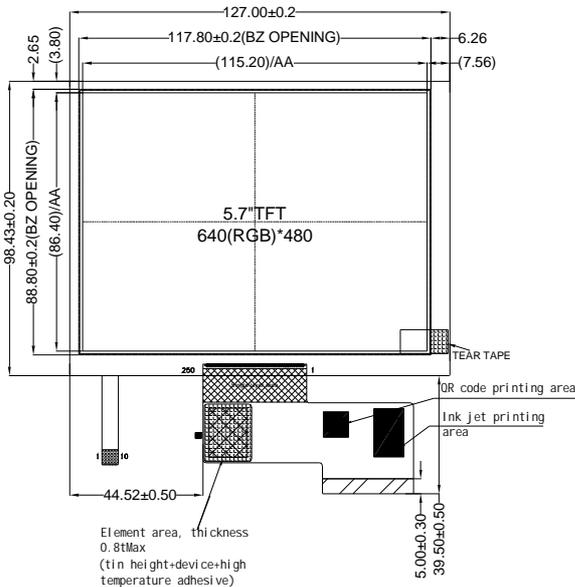
**12.6.Static Electricity**

- 12.6.1. CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro-static charge, by ground human body, etc.
- 12.6.2. The normal static prevention measures should be observed for work clothes and benches.
- 12.6.3. The module should be kept into anti-static bags or other containers resistant to static for storage.

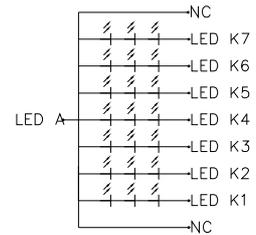
**12.7.Limited Warranty**

- 12.7.1. Our warranty liability is limited to repair and/or replacement. We will not be responsible for any consequential loss.
- 12.7.2. If possible, we suggest customer to use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used.
- 12.7.3. After the product shipped, any product quality issues must be feedback within three months, otherwise, we will not be responsible for the subsequent or consequential events.

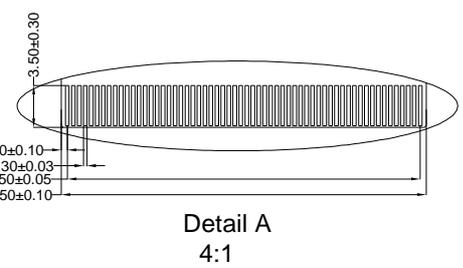
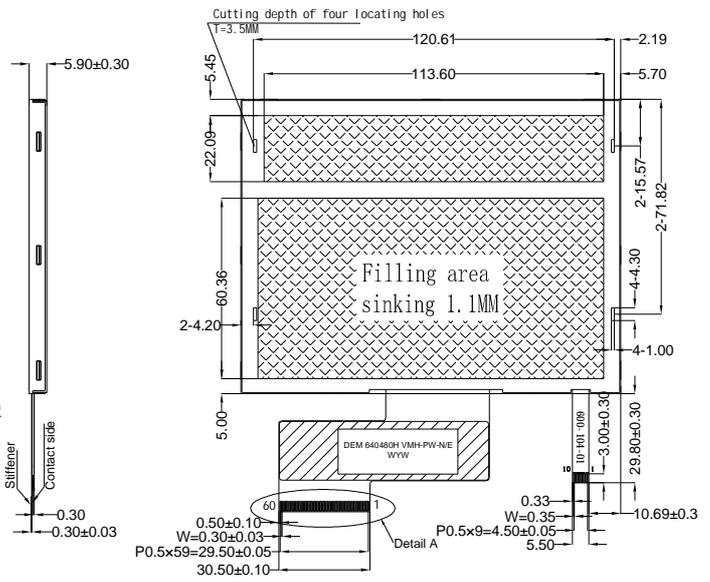
13. Outline Drawings



Element area, thickness 0.8tMax (tin height+device+high temperature adhesive)



Backlight LED Circuit: 3 × 7 = 21(LED)  
If = 140mA; Vf = 8.1 ~ 9.9V



Detail A  
4:1