Display Elektronik GmbH

DATA SHEET

TFT MODULE

DEM 480480F VMH-PW-N

(C-TOUCH)

ROUND 2,1“ TFT

Product Specification

Version: 0

17.01.2024

Revision History

Date	Rev. No.	Page	Summary
2025.01.17	V1.0	ALL	FIRST ISSUE

Contents

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This module is composed of a transmissive type TFT-LCD Panel, capacitance touch panel, driver circuit, backlight unit. The resolution of this 2.1" TFT-LCD contains 480xRGBx480 Pixels, and can display up to 16.7 Million colors.

* Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display Area(AA)	53.28 x 53.28 (2.1 Inch)	mm	-
Driver Element	TFT Active Matrix	-	-
Display Colors	16.7 Million	colors	-
Number of Pixels	480 x RGB x 480	dots	-
TFT Pixel Arrangement	RGB Vertical Stripe	-	-
Pixel Pitch	0.111 x 0.111	mm	-
Viewing Angle	ALL	o'clock	-
TFT Controller IC	ST7701S (Sitronix)	-	-
LCM Interface	2-Lane MIPI	-	-
Display Mode	IPS, Transmissive / Normally Black	-	-
Operating Temperature	-20°C ~ +70°C	°C	-
Storage Temperature	-30°C ~ +80°C	°C	-
Module Bonding Technology	Use Optical bonding between LCM and CTP	–	-

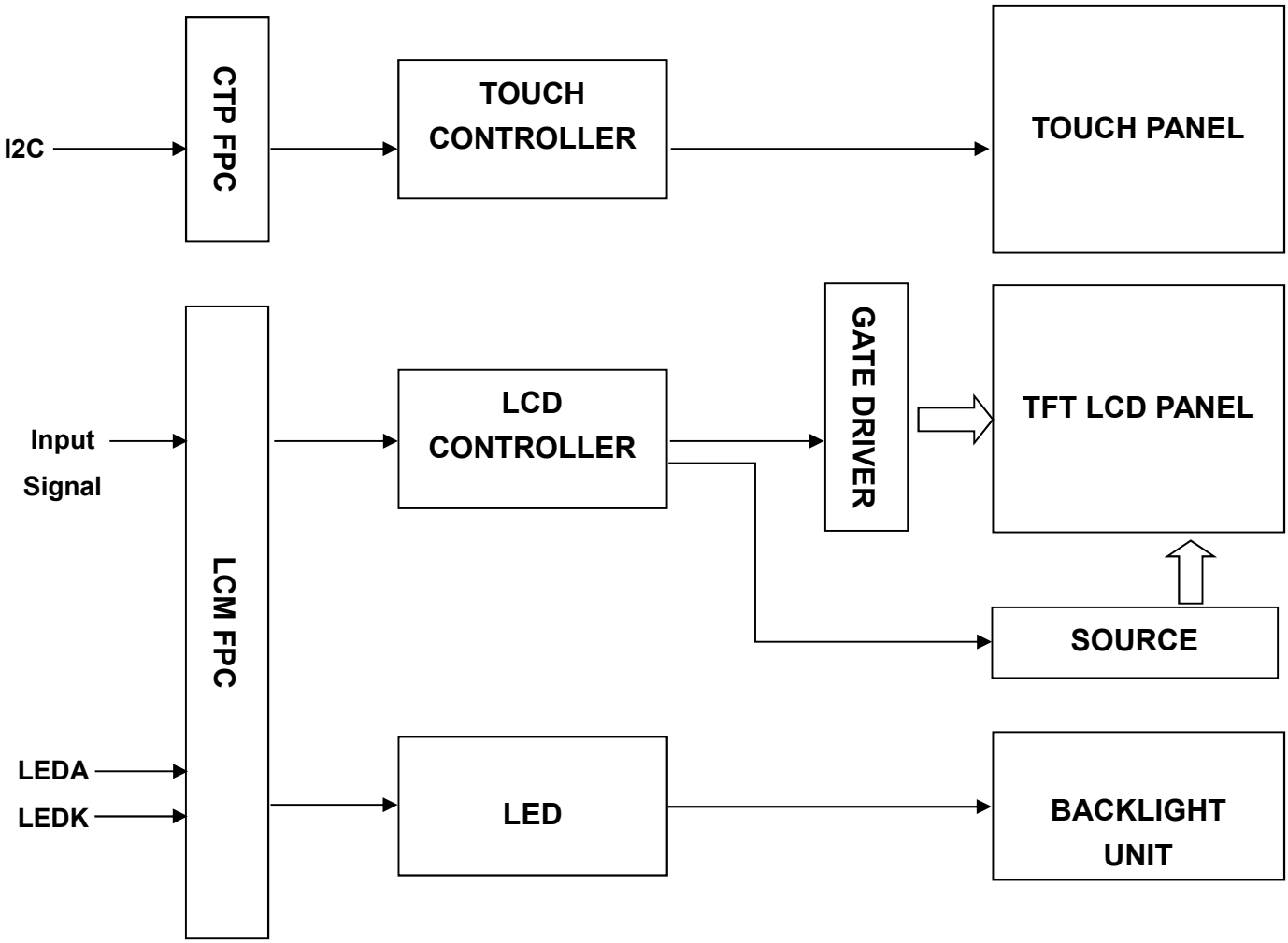
***CTP Features**

General Information Items	Specification	Unit	Note
	Main Panel		
Resolution	480 x 480	-	-
Structure	G+F+F	-	-
Controller IC	ST1633i (Sitronix)	-	-
Interface	I2C	-	-
Slave Address	0x55	-	Note1
Touch Mode	Five Points	-	-
Logic Level	3.3	V	-

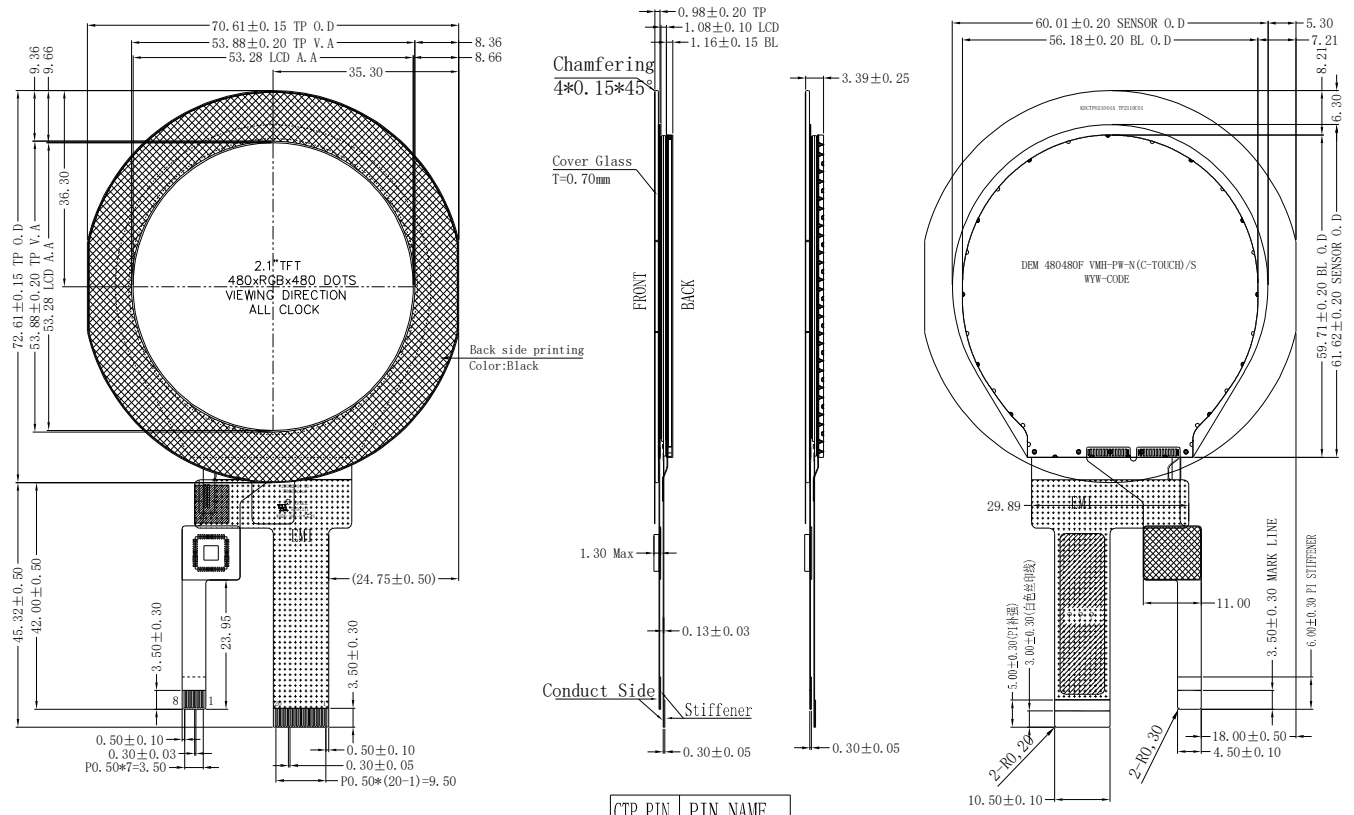
*** Mechanical Information**

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	-	70.61	-	mm	-
	Vertical(V)	-	72.61	-	mm	-
	Depth(D)	-	3.39	-	mm	-
Weight		-	21	-	g	-

1. Block Diagram

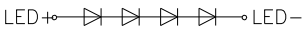


2. Outline Dimension



NOTE:
1. DISPLAY TYPE:2.1″,TFT-LCD,16.7M COLORS
2. DISPLAY MODE:NORMALLY BLACK/IPS
3. VIEWING DIRECTION:ALL
4. LCM DRIVER IC:ST7701 (COG)
   LCM Interface:2-Lane MIPI
5. Touch Mode:CTP
   Touch Driver IC:ST1633i
   Touch Interface:IIC
   Touch And LCM Bonding Technology:Optical Bonding
6. VDD/VCI:3.3V(TYP.),IOVCC:1.65-3.3V
7. OPERATING TEMP: -20° C TO 70° C
   STORAGE TEMP: -30° C TO 80° C
8. BACK LIGHT:LED WHITE, 4 LED,20mA,11.2-12.8V
9. RoHS COMPLIANT.

CTP PIN	PIN NAME
1	GND
2	NC
3	VDD-3.3V
4	SCL
5	SDA
6	INT
7	RST
8	GND



B/L Circuit

NO.	Pin Name
1	NC
2	LEDK
3	NC
4	LEDA
5	NC
6	VDD/VCI
7	IOVCC
8	TE
9	RESET
10	GND
11	MIPI_D1P
12	MIPI_D1N
13	GND
14	MIPI_CLP
15	MIPI_CLN
16	GND
17	MIPI_D0P
18	MIPI_D0N
19	GND
20	GND

Note:The opening of top case must less than LCD POL 0.3mm at least,the LCD V.A is the Recommended opening of Lens.

3. Input terminal Pin Assignment

3.1 TFT PIN Assignment

NO	SYMBOL	DISCRIPTION	I/O
1	NC		
2	LEDK	Cathode pin of backlight.	P
3	NC		
4	LEDA	Anode pin of backlight.	P
5	NC		
6	VCI	Supply Voltage (3.3V).	P
7	IOVCC	I/O power supply voltage.	P
8	TE	-Tearing effect output Leave the pin to open when not in use.	O
9	RESET	- The external reset input. Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.	I
10	GND	Ground.	P
11	MIPI_D1P	MIPI DSI differential data pair (DSI-Dn+/-). If MIPI are not used, they should be connected to DGND	I/O
12	MIPI_D1N		I/O
13	GND	Ground.	P
14	MIPI_CLP	MIPI DSI differential clock pair (DSI-CLK+/-). If MIPI are not used, they should be connected to DGND.	I
15	MIPI_CLN		I
16	GND	Ground.	P
17	MIPI_D0P	MIPI DSI differential data pair (DSI-Dn+/-). If MIPI are not used, they should be connected to DGND	I/O
18	MIPI_D0N		I/O
19	GND	Ground.	P
20	GND	Ground.	P

3.2 CTP PIN Assignment

NO	SYMBOL	DISCRIPTION	I/O
1	GND	Ground	P
2	NC	No Connection	--
3	VDD	Supply voltage	P
4	SCL	I2C clock input	I
5	SDA	I2C data input and output	I
6	INT	External interrupt to the host	I
7	RST	External Reset, Low is active	I
8	GND	Ground	P

4. LCD Optical Characteristics

4.1 Optical Specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal Viewing Angle	800	1000	--		(1)(2)
Response Time	Rising	$T_{R+}T_F$		--	30	35	msec	
	Falling							(1)(3)
Color Gamut		S(%)	-	58	62	--	%	
Color Filter Chromacicity	White	W_X	-	-0.04	0.3062	+0.04	-	(1)(4) CF glass
		W_Y	-		0.3435			
	Red	R_X	-		0.6248			
		R_Y	-		0.3481			
	Green	G_X	-		0.3103			
		G_Y	-		0.5753			
	Blue	B_X	-		0.1484			
		B_Y	-		0.0646			
Viewing Angle	Hor.	ΘL	CR>10	80	85	--	-	(1)(4)
		ΘR		80	85	--		
	Ver.	ΘU		80	85	--		
		ΘD		80	85	--		
Option View Direction		ALL						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding: dark room

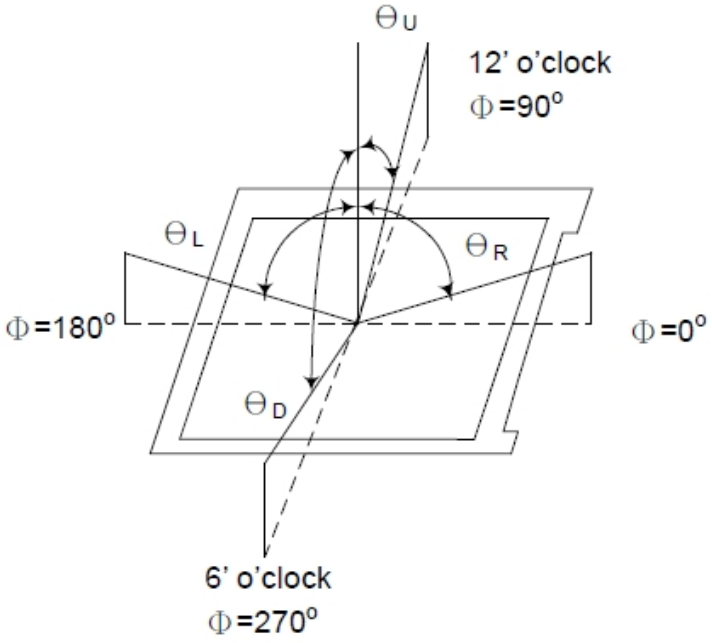
Ambient temperature: 25°C±2°C

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

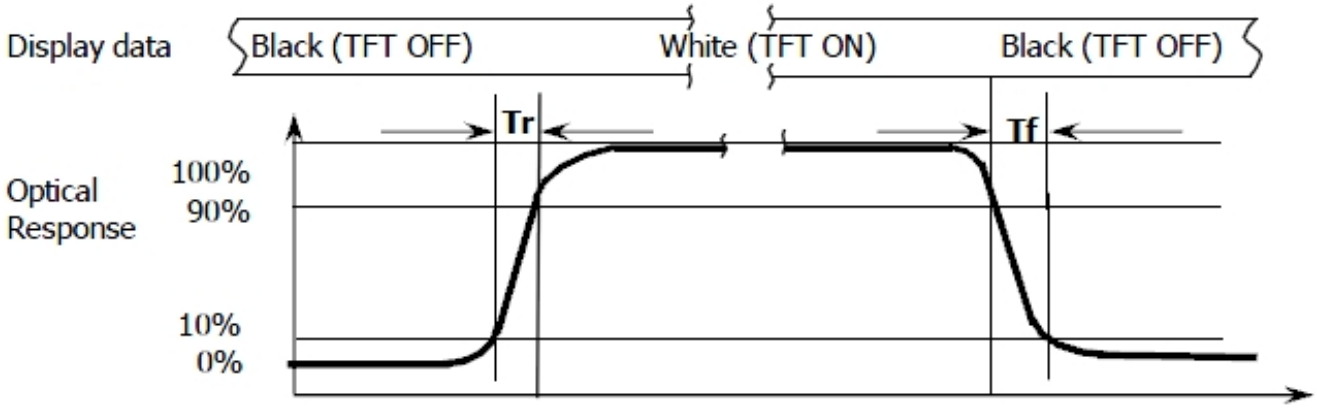
Note (1): Definition of Viewing Angle:



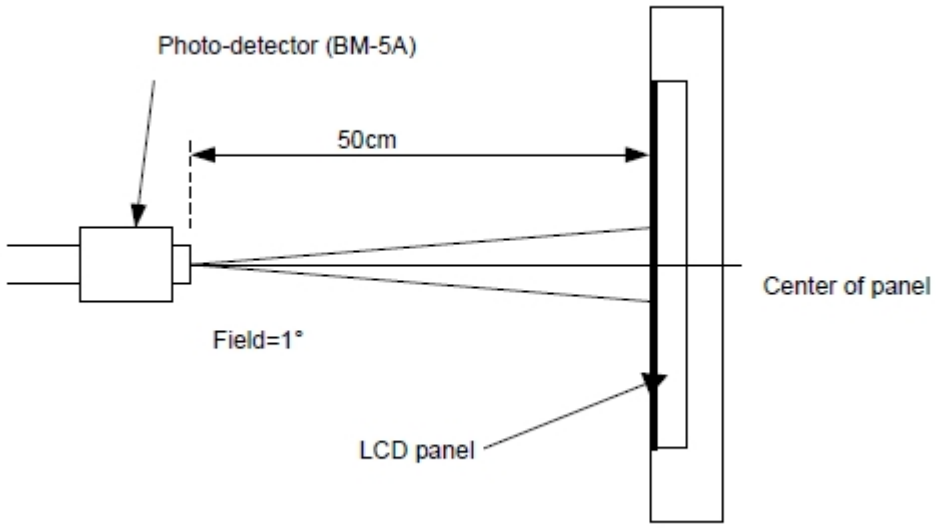
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VDD/VCI	-0.3	4.6	V	Note1
Digital Supply Voltage	IOVCC	-0.3	4.6	V	-
Operating Temperature	T_{OP}	-20	+70	°C	-
Storage Temperature	T_{ST}	-30	+80	°C	-

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged.
Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.5	3.3	3.6	V	--
Digital Supply Voltage	IOVCC	1.65	1.8	3.3	V	--
Normal Mode Current Consumption	IDD	--	19	30	mA	--
Level Input Voltage	V_{IH}	0.7 IOVCC	--	IOVCC	V	--
	V_{IL}	-0.3	--	0.3 IOVCC	V	--
Level Output Voltage	V_{OH}	0.8* IOVCC	--	IOVCC	V	--
	V_{OL}	GND	--	0.2 IOVCC	V	--

5.3 LED Backlight Characteristics

The backlight system is edge-lighting type with 4 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	--	20	--	mA	
Forward Voltage	V_F	--	12.8	--	V	--
LCM Luminance	L_V	450	500	--	cd/m2	IF=20mA
LED Lifetime	Hr	50000			Hour	
Uniformity	AVg	80	--	--	%	Note3

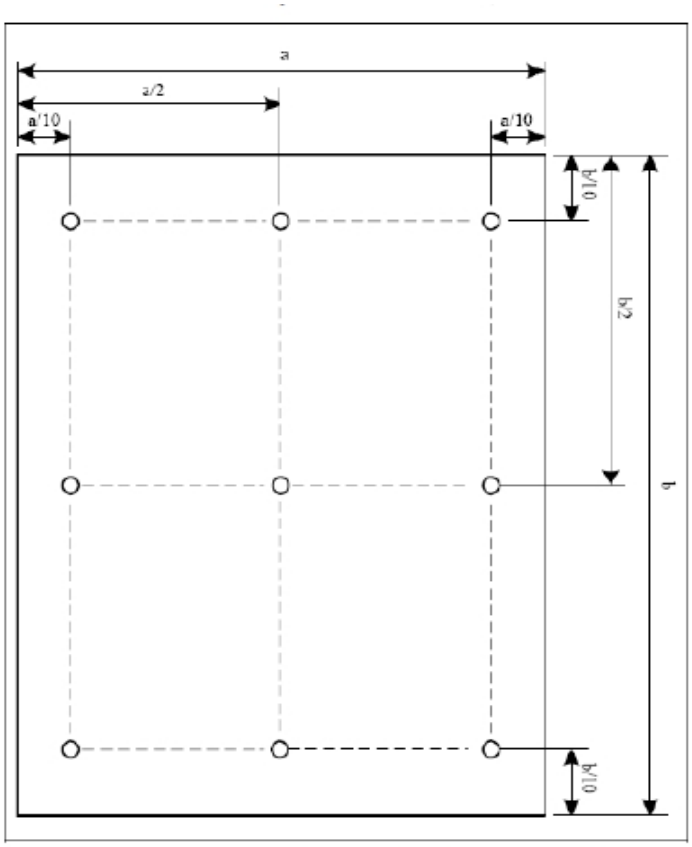
Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25°C±3°C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 20mA.

The constant current driving method is suggested.

CIRCUIT DIAGRAM

NOTE 3：Luminance Uniformity of these 9 points is defined as below:



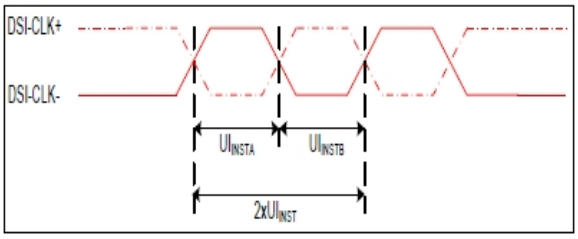
$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

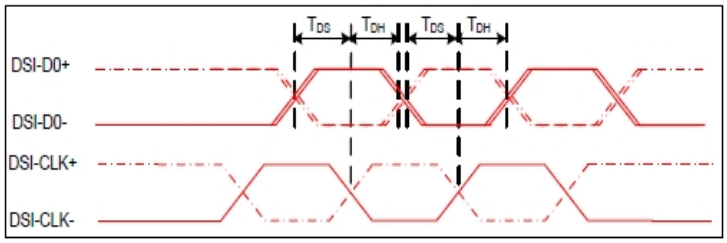
$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

6. AC Characteristics

6.1 MIPI Interface Characteristics:

6.1.1 High Speed Mode



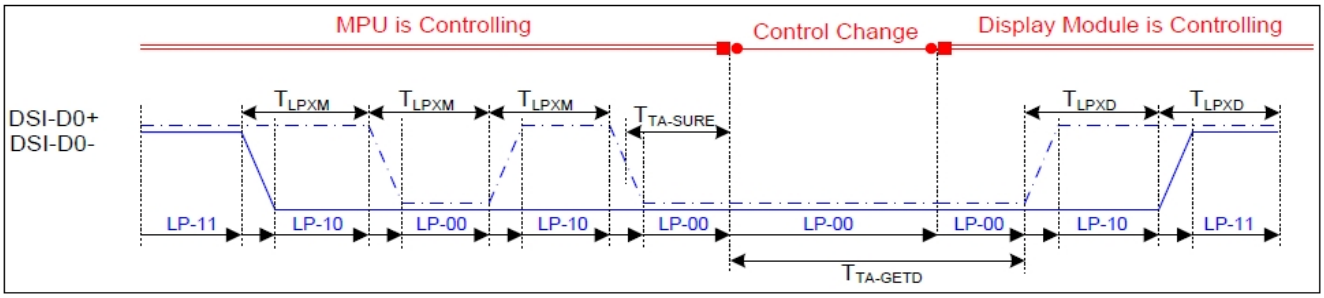


***DSI clock channel timing**

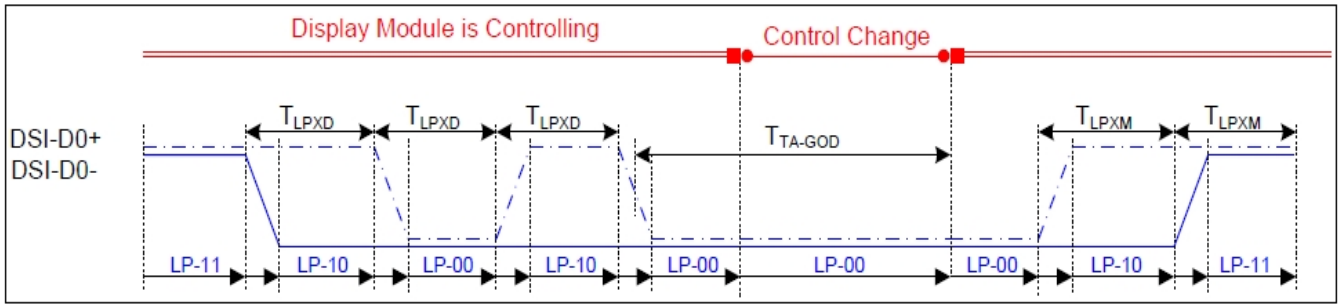
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	12.5	ns	UI = UI_{INSTA}= UI_{INSTB}
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

*** MIPI Interface-High Speed Mode Timing Characteristics**

6.1.2 Low Power Mode



*** Bus Turnaround (BTA) from display module to MPU Timing**

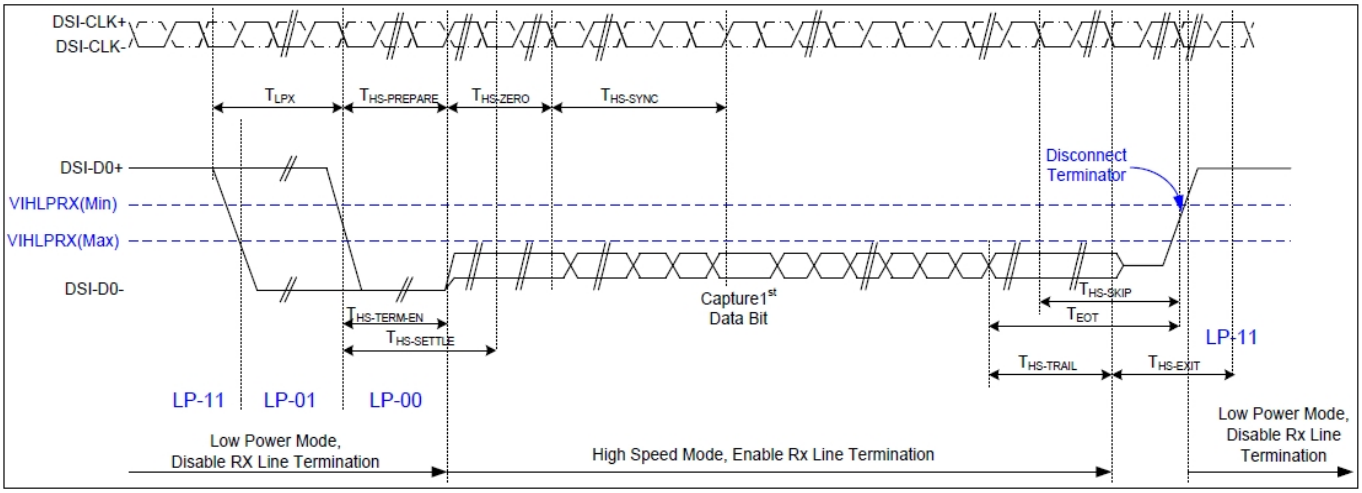


***Bus Turnaround (BTA) from MPU to display module Timing**

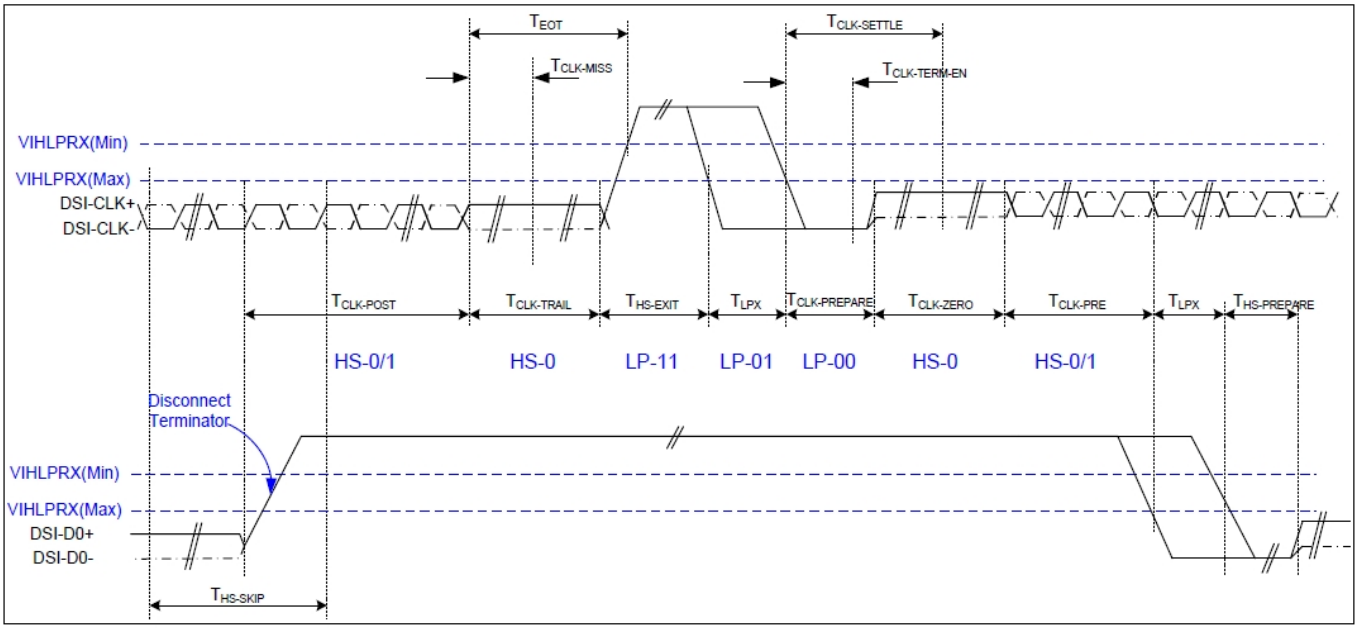
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

***MIPI Interface Low Power Mode Timing Characteristics**

6.1.3 Burst Mode



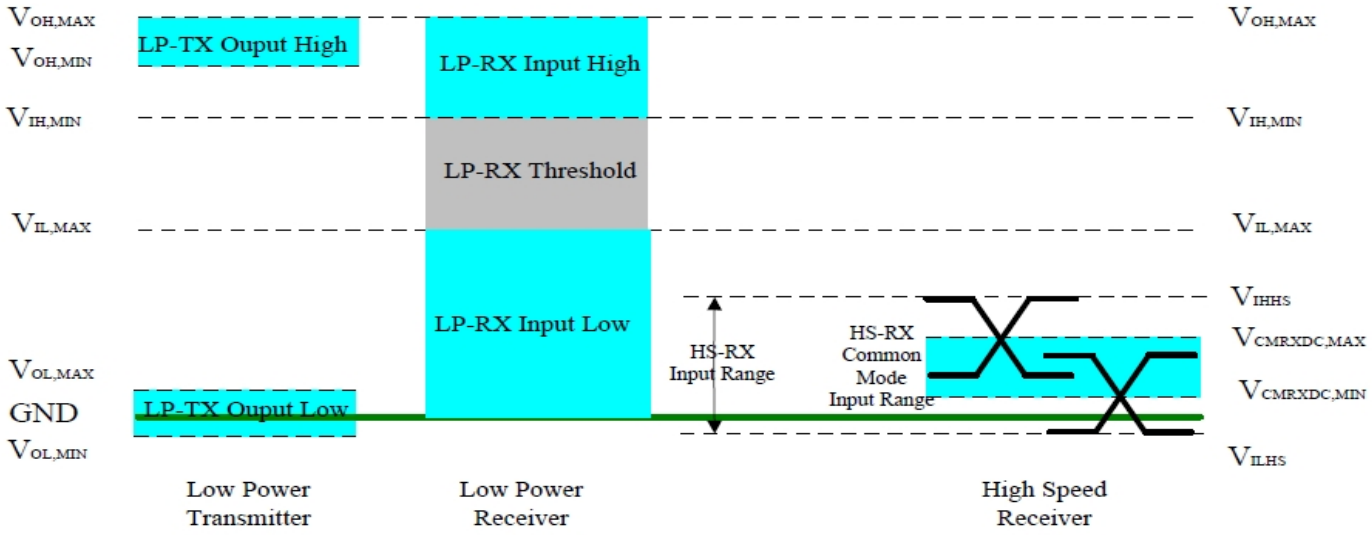
***Data lanes-Low Power Mode to/from High Speed Mode Timing**



***Clock lanes- High Speed Mode to/from Low Power Mode Timing**

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

6.2 MIPI DC Electrical Characteristics



Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Operation Voltage for MIPI Receiver					
Low power mode operating voltage	V_{LPH}	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CMRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}	80	100	125	ohm
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V_I	-50	-	1350	mV
Logic 0 input threshold	V_{IL}	0-	-	550	mV
Logic 1 input threshold	V_{IH}	880	-	1350	mV
Output low level	V_{OL}	-50	-	50	mV
Output high level	V_{OH}	1.1	1.2	1.3	V

6.3 Reset Timing

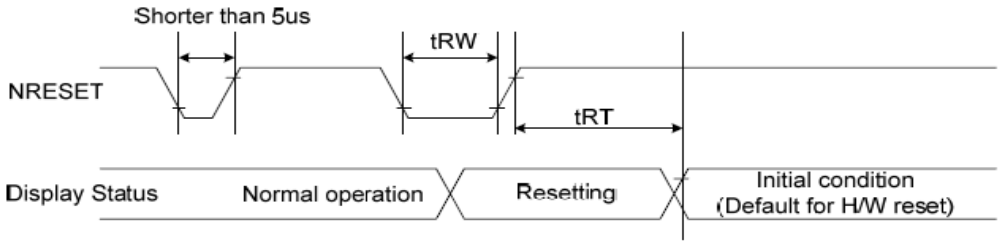


Figure 102 Reset Timing

Table 41 Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5(note 1,5)	ms
				120 (note 1,6,7)	ms

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from OTP to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 43.

Table 42 Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

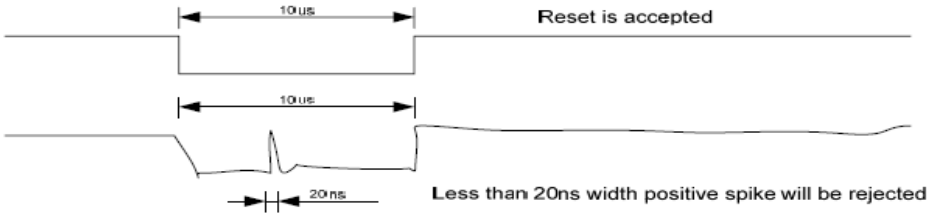


Figure 103 Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	-0.3	6	V	-
Operating Temperature	T_{OP}	-20	+70	°C	-
Storage Temperature	T_{ST}	-30	+80	°C	-

7.1.2 DC Electrical Characteristics (Ta=25°C)

(Ambient Temperature: 25°C, VDD=2.8V, VDDIO=1.8V or VDDIO=VDD)

Item	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage/VDD	2.7	3.3	3.6	V	-
Normal mode operating current	--	8.1	12.2	mA	-
Green mode operating current	--	3.3	--	mA	-
Sleep mode operating current	70	--	120	uA	-
Doze mode operating current	--	0.78	--	mA	-
Digital Input low voltage/VIL	-0.3	--	0.25*VDD	V	-
Digital Input high voltage/VIH	0.75*VDD	--	VDD+0.3	V	-
Digital Output low voltage/VOL	--	--	0.15*VDD	V	-
Digital Output high voltage/VOH	0.85*VDD	--	--	V	-

7.1.3 AC Characteristics

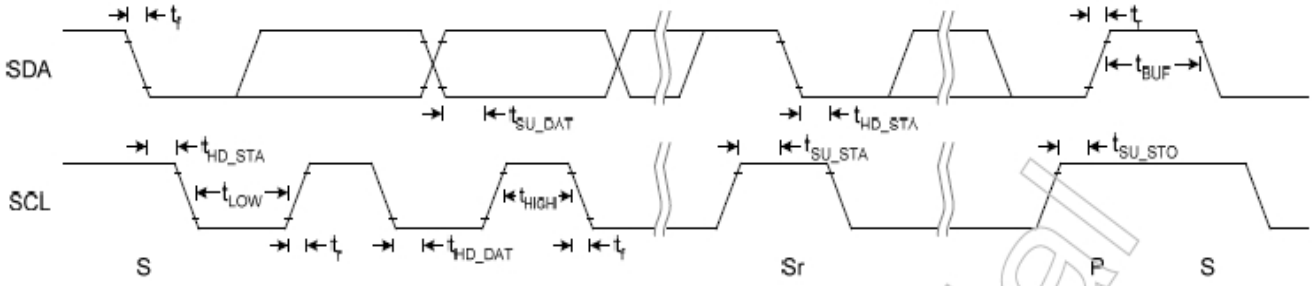


Figure 5-1 I2C Fast Mode Timing

Table 5-3 I2C Fast Mode Timing Characteristic

Conditions: VDD = 3.3V, GND = 0V, T_A = 25°C

Symbol	Parameter	Rating			Unit
		Min.	Typ	Max.	
f_{SCL}	SCL clock frequency	0		400	kHz
t_{LOW}	Low period of the SCL clock	1.3	-	-	us
t_{HIGH}	High period of the SCL clock	0.6	-	-	us
t_f	Signal falling time	-	-	300	ns
t_r	Signal rising time	-	-	300	ns
t_{SU_STA}	Set up time for a repeated START condition	0.6	-	-	us
t_{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6	-	-	us
t_{SU_DAT}	Data set up time	100	-	-	ns
t_{HD_DAT}	Data hold time	0	-	0.9	us
t_{SU_STO}	Set up time for STOP condition	0.6	-	-	us
t_{BUF}	Bus free time between a STOP and START condition	1.3	-	-	us
C_b	Capacitive load for each bus line	-	-	400	pF

7.2 SYSTEM MANAGEMENT

7.2.1 Power Down

In power down mode, all of the clocks of ST1633i are stopped. The way to exit power down mode is by a hardware reset or I2C.

7.2.2 Reset

Master can reset ST1633i through RESET pin. RESET pin is low active and needs hold low for 1us to take effect.

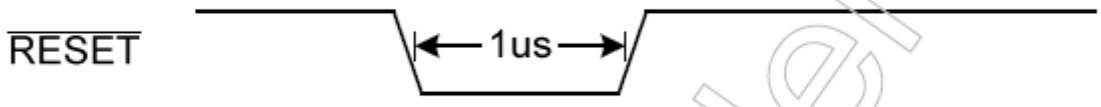


Figure 3-1 $\overline{\text{RESET}}$ Pin Low Pulse Width

7.2.3 Power On/Off Sequence

RESET pin should be held low before power on and power off. During power on, after both VDD and IOVDD reach normal voltage, RESET pin needs to be held low for 5ms to ensure internal block stable.
Note: IOVDD and VDD had connected together.

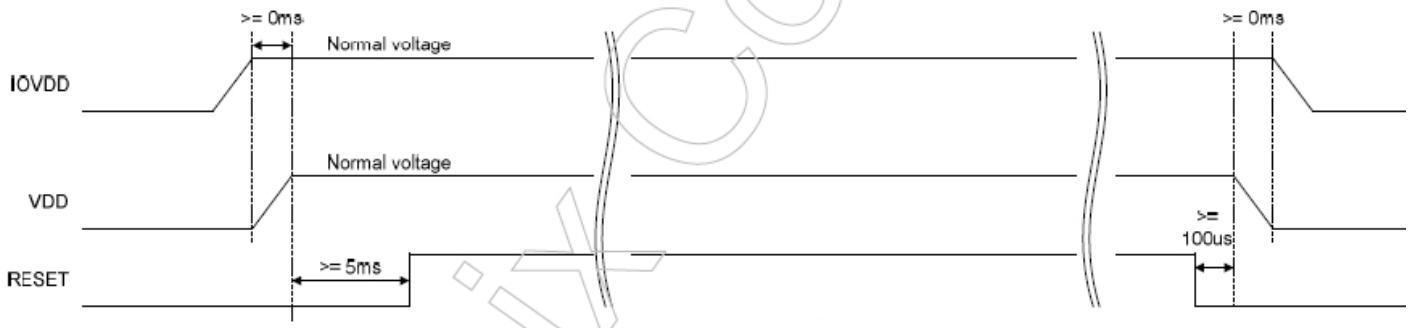


Figure 3-2 Power On/Off Sequence

8. LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

8.1.1 Inspection Conditions

Inspection performed under the following conditions is recommended.

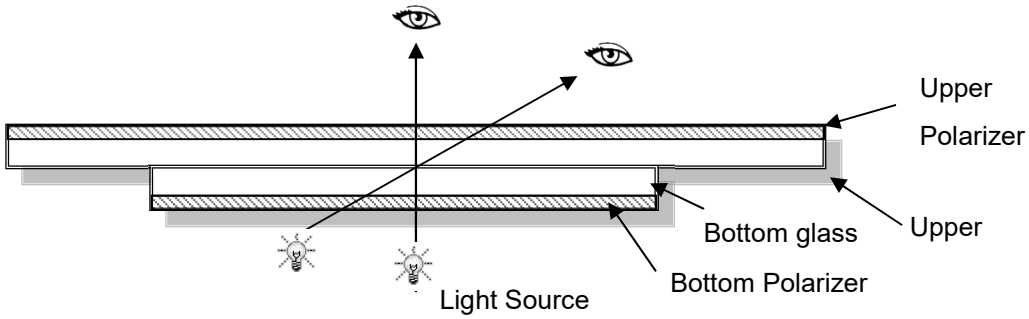
Temperature: 25°C±5°C

Humidity: 65%±10%RH

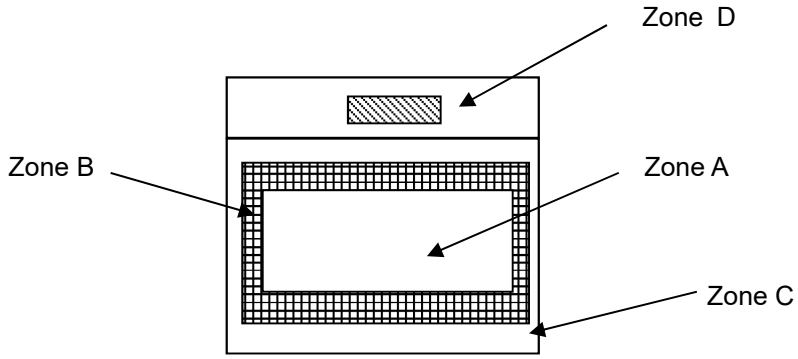
Viewing Angle: Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance: 30-50cm



8.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

Note: As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

8.1.3 Sampling Plan

According to GB/T 2828-2012, normal inspection, Class Ⅱ

AQL:

Major Defect	Minor Defect
0.65	1.5

LCD: Liquid Crystal Display, LCM: Liquid Crystal Module

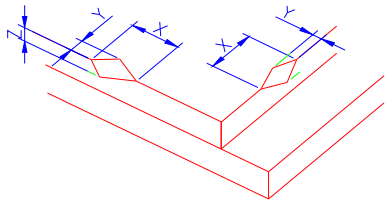
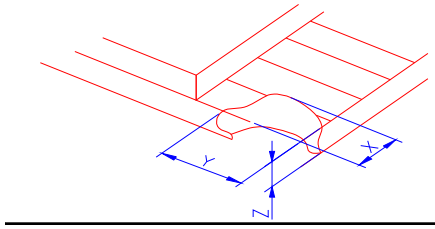
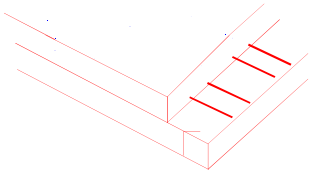
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc…	Major
2	Missing	Missing components and etc…	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed,deformation and etc…	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot,Dim spot,(Note1) Polarizer Air Bubble, Polarizer accidented spot and etc…	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc…	
7	LCD/Polarizer/CTP	Black/White spot/line, scratch, crack, etc.	

Note1:

a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

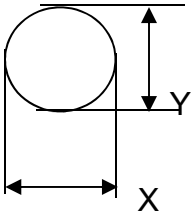
b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

8.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

2.0

Spot defect



Φ=(X+Y)/2

① light dot（ black/white spot , pinhole, stain，etc.）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧10mm)		
0.25<Φ≤0.4	2(distance≧10mm)		
Φ>0.4	0		

② Dim spot（light leakage、dent、dark spot，etc）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧10mm)		
0.25<Φ≤0.4	2(distance≧10mm)		
Φ>0.4	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.5	2(distance≧10mm)		
Φ>0.5	0		

④Polarizer Bubble

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.4	2(distance≧10mm)		
0.4<Φ≤0.5	1		
Φ>0.5	0		

3.0 LCD Pixel defect

Pixel bad points

Item	Zone A	Acceptable Qty
Bright dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Dark dot	Random	N≤3
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm
Total bright and dark dot		N≤4

Note:

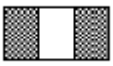
A) Bright dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

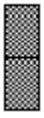
C) 2 dot adjacent = 1 pair = 2 dots

Picture:

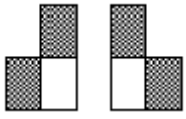
2 dot adjacent



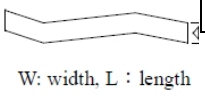
2 dot adjacent



2 dot adjacent (vertical)



2 dot adjacent (slant)

<table>
<tr>
<td>4.0</td>
<td>Line defect (LCD /Polarizer backlight black/white line, scratch, stain)
 
W: width, L：length
N：Count</td>
<td>
<table>
<tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.05</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L≤5.0</td><td colspan="2">N≤3</td></tr>
<tr><td>0.06<W≤0.08</td><td>L≤4.0</td><td colspan="2">N≤2</td></tr>
<tr><td>W>0.08</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td>
</tr>
<tr>
<td>5.0</td>
<td>Electronic Components SMT.</td>
<td>Not allow missing parts，solderless connection，cold solder joint，mis match，The positive and negative polarity opposite</td>
</tr>
<tr>
<td>6.0</td>
<td>Display color & Brightness.</td>
<td>1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td>
</tr>
<tr>
<td>7.0</td>
<td>LCD Mura Waving Hot spot</td>
<td>Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.</td>
</tr>
<tr>
<td>8.0</td>
<td>CTP Related</td>
<td>CTP Cover sensor accidented black/white spot</td>
<td>
<table>
<tr><th rowspan="2">Size Φ(mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.15</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.15<Φ≤0.25</td><td colspan="2">1 (distance ≥10mm)</td></tr>
<tr><td>0.25<Φ≤0.35</td><td colspan="2">2 (distance ≥10mm)</td></tr>
<tr><td>Φ>0.35</td><td colspan="2">0</td><td></td></tr>
</table>
</td>
</tr>
</table>

CTP Cover scratch

Width(mm)	Ignore(mm)	Acceptable Qty		
		A	B	C
Φ≤0.05	Ignore	Ignore		
0.05<W≤0.06	L≤4.0	N≤3		
0.06<W≤0.08	L≤3.0	N≤2		
0.08<W	Define as spot defect			

CTP Cover Pinhole/ Lack of ink

Zone / Size (mm)	Acceptable Qty
	C
Φ≤0.2	Ignore
0.2<Φ≤0.3	4(distance≥10mm)
0.3<Φ≤0.4	2(distance≥10mm)
Φ>0.4	0

CTP Bonding bubble/ accidented spot

Size Φ(mm)	Acceptable Qty	
	A	B
Φ≤0.1	Ignore	
0.1<Φ≤0.2	3(distance≥10mm)	
0.2<Φ≤0.3	2(distance≥10mm)	
Φ>0.3	0	

Assembly deflection

beyond the edge of backlight ≤0.2mm

CTP cover broken

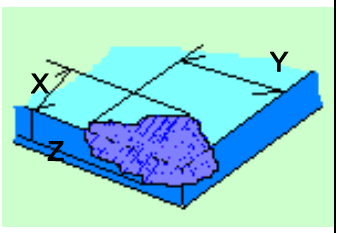
X : length

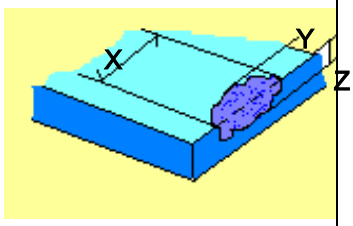
Y : width

Z : height

X	Y	Z
X≤0.5mm	Y≤0.5mm	Z<cover thickness

Circuitry broken is not allowed.



		CTP cover broken X：length Y：width Z：height	X: X≤0.3mm; Y: Y≤0.3mm; Z: Z<cover thickness * Circuitry broken is not allowed.	

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

9. Reliability Test Result

Remark:

Item	Condition	Inspection after test
High Temperature Operating	70°C,96h	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1. Air bubble in the LCD; 2. Non-display; 3. Missing segments/line; 4. Glass crack; 5. Current IDD is twice higher than initial value.
Low Temperature Operating	-20°C, 96h	
High Temperature Storage	80°C, 96h	
Low Temperature Storage	-30°C, 96h	
High Temperature & High Humidity Operating	+60°C, 90% RH ,96h	
Thermal Shock (Non-operation)	-10°C, 30 min ↔ +60°C, 30 min, Change time: 5min 20CYC.	
ESD test	C=150pF, R=330, 5points/panel Air:±8kV, 5times; Contact:±6kV, 5 times; (Environment: 15°C~35°C, 30%~60%).	
Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.5mm Sweep: 10Hz~55Hz ~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX)	

1. The test samples should be applied to only one test item.
2. Sample size for each test item is 5~10pcs.
3. For Damp Proof Test, Pure water (Resistance > 10MΩ) should be used.
4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
5. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6. The color fading mura of polarizing filter should not care.

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the “Power ON” condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0°C to 35°C
and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed.
Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.