Display Elektronik GmbH

DATA SHEET

TFT MODULE

DEM 400960B VMX-PW-N 3,99" TFT

Product Specification

Version: 0

Revision History

Date	Rev. No.	Page	Summary
28.12.2024	0	ALL	FIRST ISSUE

Product Specification

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* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This module is composed of a transmissive type TFT-LCD Panel, driver circuit, backlight unit. The resolution of a 4.0 " TFT-LCD contains 400xRGBx960 pixels, and can display up to 65k/262k/16.7Million colors.

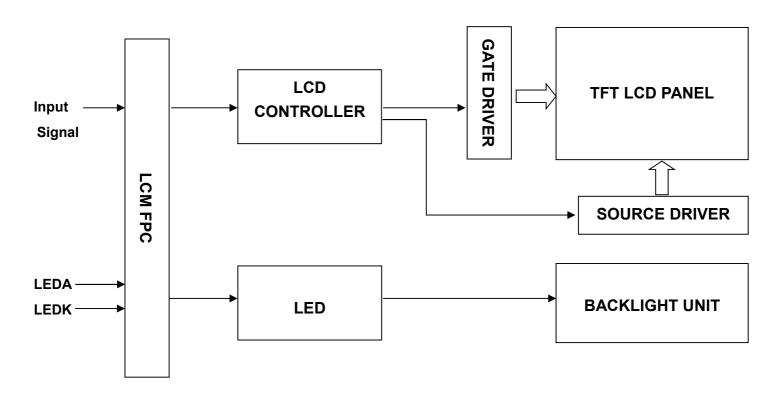
* Features

General Information	Specification	l læi4	Note	
Items	Main Panel	Unit		
Display Area(AA)	39.18 x 94.03 (3,99 Inch)	mm	-	
Driver Element	TFT Active Matrix	-	-	
Display Colors	65k / 262k / 16.7Million	colors	-	
Number of Pixels	400 x RGB x 960	dots	-	
Pixel Arrangement	RGB Vertical Stripe	-	-	
Pixel Pitch	0.3265 x 0.9795	mm	-	
Viewing Angle	ALL	o'clock	-	
Controller IC	ST7701S (Sitronix)	-	-	
LCM Interface	3SPI + 16/18/24-BIT-RGB	-	-	
Display Mode	IPS, Transmissive / Normally Black	-	-	
Operating Temperature	-30 ~ +85	°C	-	
Storage Temperature	-30 ~ +85	°C	-	

* Mechanical Information

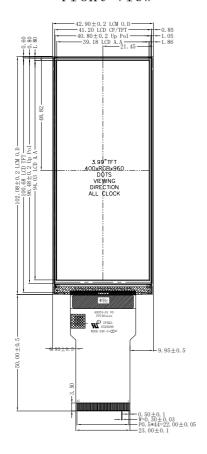
	Item	Min.	Тур.	Max.	Unit	Note
	Horizontal(H)	-	42.90	-	mm	-
Module Size	Vertical(V)	-	102.80	-	mm	-
	Depth(D)	-	2.17	-	mm	-
Weight		-	20	-	g	-

1. Block Diagram

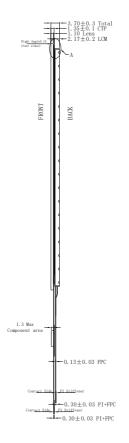


2. Outline Dimension

Front View



Side View



Bottom View



NOTE: RGB interface DB Used.

RGB Interface	DB Pin in use	
16 Bit RGB interface	DB20-DB16, DB13-DB8,	DB4-DB0
18 Bit RGB interface	DB21-DB16, DB13-DB8,	DB5-DB0
24 Bit RGB interface	DB23-DB0	

NOTE: If used RGB mode must select serial interface!

NOTE:

- 1. DISPLAY TYPE: 4.0", TFT-LCD, 16.7M COLORS
- 2. DISPLAY MODE: NORMALLY BLACK/IPS
- 3. VIEWING DIRECTION: ALL
- 4. LCM DRIVER IC:ST7701SI (COG)

LCM Interface:3SPI+16/18/24BIT RGB Interface

- 5. VCI: 3. 3V (TYP.), IOVCC: 1. 65-3. 3V
- 6. OPERATING TEMP: -30° C TO 85° C STORAGE TEMP: -30° C TO 85° C
- 7. BACK LIGHT: LED WHITE, 8 LED, 20mA, $22.4^27.2\text{V}$
- 8. RoHS COMPLIANT.

B/L Circuit

1	XIVING
2	YD/NC
3	XL/NC
4	YU/NC
5	GND
6	GND
7	VCI
8	IOVCC
9	SDO
10	SDI
11	SCL
12	CS
13	RESET
14	DB23(R7)
15	DB22(R6)
16	DB21(R5)
17	DB20(R4)
18	DB19(R3)
19	DB18(R2)
20	DB17(R1)
21	DB16(R0)
22	DB15(G7)
23	DB14(G6)
24	DB13(G5)
25	DB12(G4)
26	DB11(G3)
27	DB10(G2)
28	DB9(G1)
29	DB8(G0)
30	DB7(B7)
31	DB6(B6)
32	DB5(B5)
33	DB4(B4)
34	DB3(B3)
35	DB2(B2)
36	DB1(B1)
37	DB0(B0)
38	DE
39	PCLK
40	HSYNC
41	VSYNC
42	NC
43	LEDK
44	NC
45	LEDA

1 XR/NC

3. Input Terminal Pin Assignment

<u>3. Inpu</u>	<u>t Terminal</u>	Pin Assignment				
NO.	SYMBOL	DISCRIPTION	I/O			
1	XR/NC	Touch panel Right Glass Terminal	A/D			
2	YD/NC	Touch panel Bottom Film Terminal	A/D			
3	XL/NC	Touch panel LIFT Glass Terminal	A/D			
4	YU/NC	Touch panel Top Film Terminal	A/D			
5	GND	Ground.	Р			
6	GND	Ground.	Р			
7	VCI	Supply voltage (3.3V).	Р			
8	IOVCC	Supply Voltage (Logic)(1.8~3.3V).	Р			
9	SDO	Serial data output pin used for the SPI Interface.	0			
9	300	Leave the pin open when not in use.	U			
10	SDI	SDI: Serial data input/output bidirectional pin for SPI Interface.	1/0			
10	ODI	Fix to GND level when not in use.	1,0			
11	SCL	SCL: Serial clock input for SPI interface.	ı			
	002	Fix to IOVCC or GND level when not in use.	'			
		A chip select signal				
12	CS	Low: the chip is selected and accessible				
		High: the chip is not selected and not accessible				
		Fix to IOVCC or GND level when not in use.				
		- The external reset input				
13	RESET	- Initializes the chip with a low input. Be sure to execute	I			
		a power-on reset after supplying power.				
14-37	DB23-DB0	24-bit parallel data bus for RGB Interface.	I/O			
		Fix to IOVCC or GND level when not in use.				
		Data enable signal for RGB interface operation				
38	DE	Low: access enabled	1			
		High: access inhibited				
		Fix to IOVCC or GND level when not in use.				
39	PCLK	Dot clock signal for RGB interface operation	ı			
		Fix to IOVCC or GND level when not in use.				
40	HSYNC	Line synchronizing signal for RGB interface operation	ı			
		Fix to IOVCC or GND level when not in use.				
41	VSYNC	Frame synchronizing signal for RGB interface operation				
41	VOTING	Fix to IOVCC or GND level when not in use.	'			
42	NC	Not Connected	-			
43	LEDK	Cathode pin of backlight.	Р			
44	NC	Not Connected	-			
45	LEDA	Anode pin of backlight.	Р			
	1					

4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Тур.	Max.	Unit.	Note
Contrast Ratio		CR		1000	1300			(1)(2)
Response Time	Rising Falling	$T_{R+}T_{F}$			25	35	msec	(1)(3)
Color Gam	ut	S(%)		-	59.97		%	C-light
		Wx	Θ=0		0.2955			(1)(4)
	White	W_{Y}	Normal		0.3381	+0.04		CF glass
		R _X	Viewing Angle	-0.04	0.6227			
Color Filter	Red	R _Y			0.3410			
Chromacicity	Green	G _X			0.3070			
		G _Y			0.5673			
		B _X			0.1476			
	Blue	B _Y			0.0805			
		ΘL		80	85			(1)(4)
	Hor.	ΘR		80	85			
Viewing Angle		ΘU	CR>10	80	85			
	Ver.	ΘD		80	85			
Option View Dir	ection				ALL			

^{*}The data comes from the LCD specification.

Measuring Condition

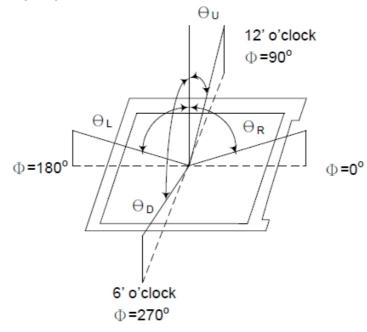
Measuring surrounding: dark room Ambient temperature: 25°C ± 2°C

15min. warm-up time.

Measuring Equipment

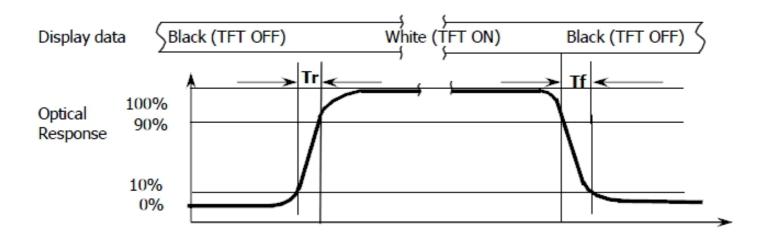
FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

Note (1): Definition of Viewing Angle:

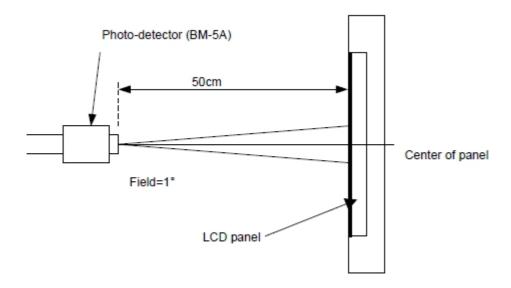


Note (2): Definition of Contrast Ratio(CR): measured at the center point of panel

Note (3): Response Time



Note (4): Definition of optical measurement setup



5. Electrical Characteristics

5.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VCI	-0.3	4.6	V	Note1
Digital Interface Supply Voltage	IOVCC	-0.3	4.6	V	-
Operating Temperature	Тор	-30	+85	°C	-
Storage Temperature	Tst	-30	+85	°C	-

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Тур.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.5	2.8	3.6	V	-
Digital Interface Supply Voltage	IOVCC	1.65	1.8	3.3	V	-
Normal Mode Current	ICC		35		mA	-
Loyal Input Valtage	VIH	0.7* lovcc		lovcc	V	-
Level Input Voltage	VIL	GND		0.3* lovcc	V	-
Laval Output Valtaria	Vон	0.8*lovcc		lovcc	V	-
Level Output Voltage	VoL	GND		0.2*lovcc	V	-

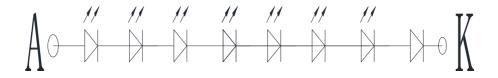
5.3 LED Backlight Characteristics

The Backlight system is edge-lighting type with 8 chips LED

Item	Symbol	Min.	Тур.	Max.	Unit	Note
Forward Current	l _F		20		mA	-
Forward Voltage	VF	22.4	22.33	27.2	V	-
LCM Luminance (I _F =20mA)	LV	450	500		cd/m2	IF=20mA
LED Lifetime	Hr		50000		Hour	Note 1,2
Uniformity	Avg	80			%	Note 3

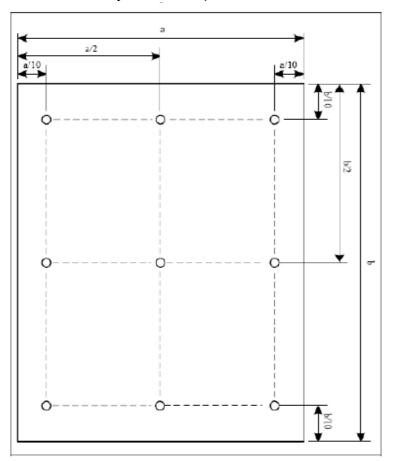
Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25°C±3°C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 20mA. The constant current driving method is suggested.





Note (3) Luminance Uniformity of these 9 points is defined as below:



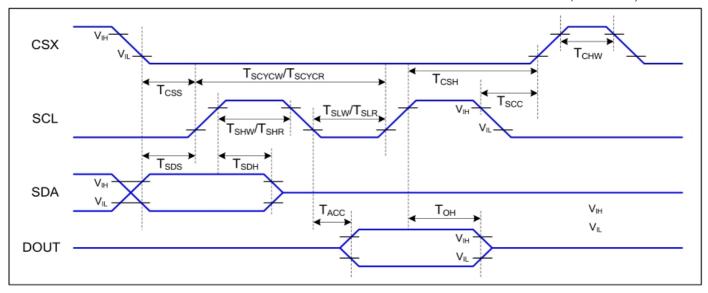
Uniformity = $\frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$

$$Luminance = \frac{Total\ Luminance\ of\ 9\ points}{9}$$

6. AC Characteristics

6.1 Serial Interface Characteristics (3-Line Serial):

IOVCC=1.8V,VCI=2.8V,Ta=25°C



3-Line Serial Interface Timing Characteristics

3-Line Serial Interface Characteristics

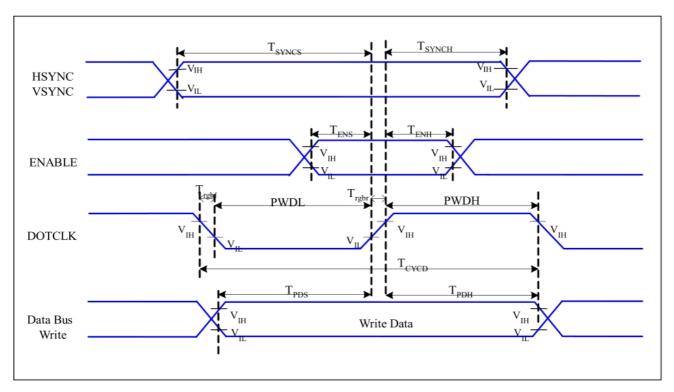
Note: The rising time and falling time (Tr, Tf) of input signal are specified

Signal	Symbol	Parameter	Min	Max	Unit	Description
	T _{CSS}	Chip select setup time (write)	15		ns	
	T _{CSH}	Chip select hold time (write)	15		ns	
csx	T _{CSS}	Chip select setup time (read)	60		ns	
	T _{SCC}	Chip select hold time (read)	60		ns	
	T _{CHW}	Chip select "H" pulse width	40		ns	
	T _{SCYCW}	Serial clock cycle (Write)	66		ns	
	T _{SHW}	SCL "H" pulse width (Write)	15		ns	
SCL	T _{SLW}	SCL "L" pulse width (Write)	15		ns	
SCL	T _{SCYCR}	Serial clock cycle (Read)	150		ns	
	T _{SHR}	SCL "H" pulse width (Read)	60		ns	
	T _{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA	T _{SDS}	Data setup time	10		ns	
(DIN)	T _{SDH}	Data hold time	10		ns	

at 15 ns or less. Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

6.2 RGB Interface Characteristics:

IOVCC=1.8V,VCI=2.8V,Ta=25°C

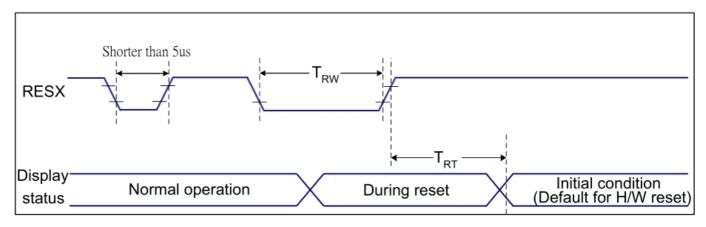


RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC,	т	VCVNC UCVNC Setus Time	5			
VSYNC	T _{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T _{ENS}	Enable Setup Time	5	-	ns	
ENABLE	T _{ENH}	Enable Hold Time	5	-	ns	
	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
DOTCLK	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
DOTCLK	T _{CYCD}	DOTCLK Cycle Time	33	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T _{PDS}	PD Data Setup Time	5	-	ns	
	T_PDH	PD Data Hold Time	5	-	ns	

18/16 Bits RGB Interface Timing Characteristics

6.3 Reset Input Timing:



Reset Timing

Related Pins	Symbol	Parameter	MIN	MAX	Unit
	TRW	Reset pulse duration	10	-	us
RESX	TDT	Deset sensel	-	5 (Note 1, 5)	ms
	TRT	Reset cancel		120(Note 1, 6, 7)	ms

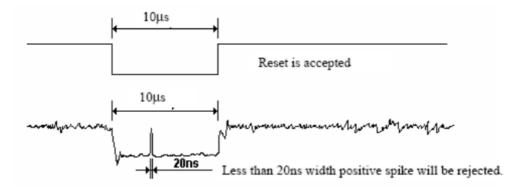
Reset Timing

Notes:

- 1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
 - 2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

- 3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
 - 4. Spike Rejection also applies during a valid reset pulse as shown below:



- 5. When Reset applied during Sleep In Mode.
- 6. When Reset applied during Sleep Out Mode.
- 7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. RGB Interface

The ST7701 support RGB interface Mode 1 and Mode 2. The interface signals as shown in ST7701S datasheet table 6.3.1.

The Mode 1 and Mode 2 function is select by setting in the Command 2, please reference application note.

In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D[23:0]), when DE is high state.

The external clocks (PCLK, VS and HS) are used for internal displaying clock. So controller must always transfer PCLK, VS and HS signal to ST7701.

In RGB Mode 2, back porch of Vsync is defined by VBP[5:0] of RGBPRCTR command. And back porch of Hsync is defined by HBP[5:0] of RGBPRCTR command. Front porch of Vsync is defined by VFP[5:0] of RGBPRCTR command.

And front porch of Hsync is defined by HFP[5:0] of RGBPRCTR command.

RGB I/F Mode	PCLK	DE	VS	HS	DB[23:0]	Register for Blanking Porch setting
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

Symbol	Name	Description
PCLK	Pixel clock	Pixel clock for capturing pixels at display interface
HS	Horizontal sync	Horizontal synchronization timing signal
VS	Vertical sync	Vertical synchronization timing signal
DE	Data enable	Data enable signal (assertion indicates valid pixels)
DB[23:0]	Pixel data	Pixel data in 16-bit,18-bit and 24-bit format

The interface signals of RGB interface

7.1.1 RGB Color Format

ST7701 supports two kinds of RGB interface, DE mode (mode 1) and HV mode (mode 2), and 16bit/18bit and 24 bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, D[17:0] pins can be used; when HV mode is selected and the VSYNC, HSYNC, DOTCLK, D[17:0] pins can be used. When using RGB interface, only serial interface can be selected.

Pad name	24 bits configuration VIPF[3:0]=0111	18 bits cor VIPF[3:	16 bits configuration VIPF[3:0]=0101	
	VII 1 [0:0]=0111	MDT=0	MDT=1	VII 1 [0.0]=0101
DB[23]	R7	Not used	Not used	Not used
DB[22]	R6	Not used	Not used	Not used
DB[21]	R5	R5	Not used	Not used
DB[20]	R4	R4	Not used	R4
DB[19]	R3	R3	Not used	R3
DB[18]	R2	R2	Not used	R2
DB[17]	R1	R1	R5	R1
DB[16]	Ro	Ro	R4	R0
DB[15]	G7	Not used	R3	Not used
DB[14]	G6	Not used	R2	Not used
DB[13]	G5	G5	R1	G5
DB[12]	G4	G4	R0	G4
DB[11]	G3	G3	G5	G3
DB[10]	G2	G2	G4	G2
DB[09]	G1	G1	G3	G1
DB[08]	G0	G0	G2	G0
DB[07]	B7	Not used	G1	Not used
DB[06]	B6	Not used	Go	Not used
DB[05]	B5	B5	B5	Not used
DB[04]	B4	B4	B4	B4
DB[03]	В3	В3	В3	В3
DB[02]	B2	B2	B2	B2
DB[01]	B1	B1	B1	B1
DB[00]	Во	Во	Во	Во

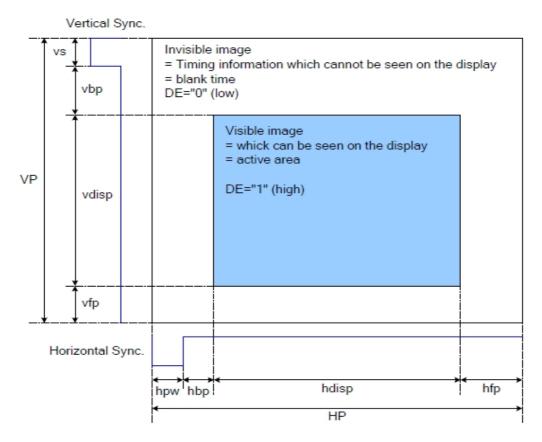
The Interface Color Mapping of RGB Interface

7.1.2 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals.

The data can be written only within the specified area with low power consumption by using window address function.

The back porch and front porch are used to set the RGB interface timing.



DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Тур.	Max.	Unit
DCLK Frequency	FCLK	-	(32)	-	MHz
Horizontal Sync. Width	hpw	1	(10)	255	Clock
Horizontal Sync. Back Porch	hbp	1	(30)	255	Clock
Horizontal Sync. Front Porch	hfp	1	(62)		Clock
Vertical Sync. Width	VS	1	(10)	254	Line
Vertical Sync. Back Porch	vbp	1	(30)	254	Line
Vertical Sync. Front Porch	vfp	1	(62)		Line

Note: 1. Typical value are related to the setting frame rate is 60Hz.

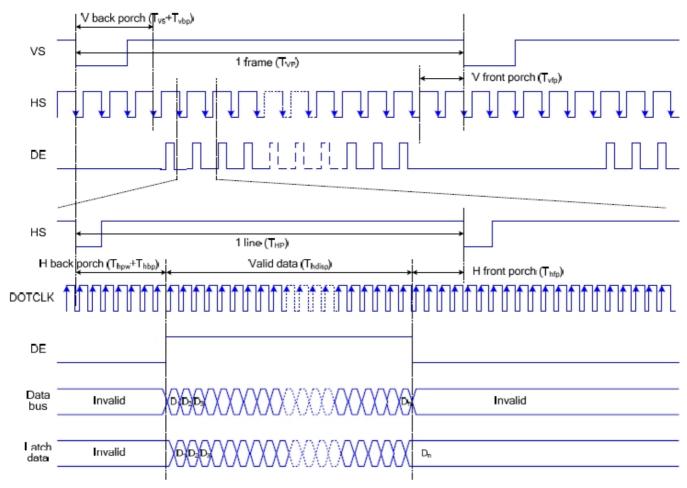
7.1.3 RGB Interface Mode Selection

ST7701 supports two kinds of RGB interface, DE mode and HV mode. The table shown below uses command C3h to select RGB interface mode.

DE/Sync	RGB Mode
0	DE mode
1	HV mode

7.1.4 RGB Interface Timing

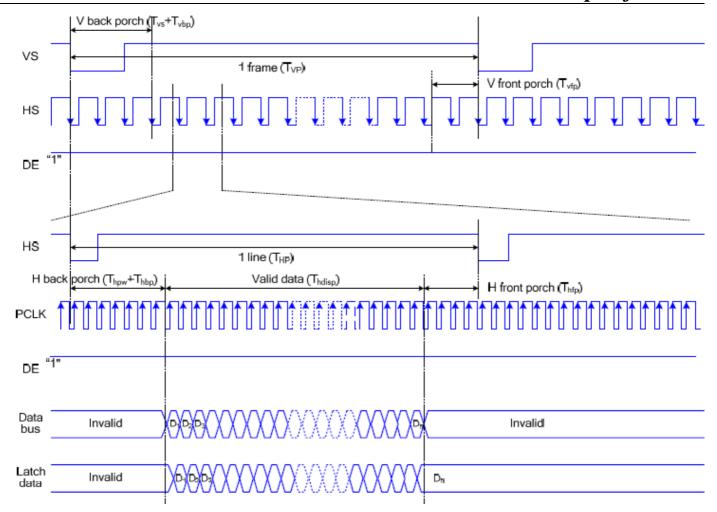
The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.



Timing chart of RGB interface HV mod

8. LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

8.1.1 Inspection Conditions

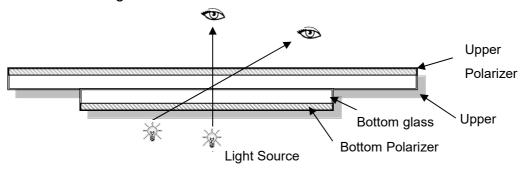
Inspection performed under the following conditions is recommended.

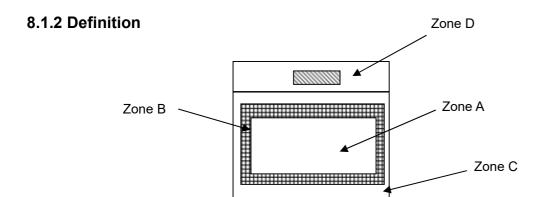
Temperature: 25°C± 5°C Humidity: 65%±10%RH

Viewing Angle: Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance: 30-50cm





Zone A: Effective Viewing Area(Character or Digit can be seen)

Zone B: Viewing Area except Zone A

Zone C: Outside (Zone A+Zone B) which can not be seen after assembly by customer.)

Zone D: IC Bonding Area

Note: As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

8.1.3 Sampling Plan

According to GB/T 2828-2003, normal inspection, Class $\rm II$ AQL:

Major Defect	Minor Defect
0.65	1.5

LCD: Liquid Crystal Display, LCM: Liquid Crystal Module,

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	 No display, Open or miss line Display abnormally, Short Backlight no lighting, abnormal lighting. etc 	Major
2	Missing	Missing components and etc	aje.
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed, deformation and etc	
4	Color tone	Color unevenness, refer to limited sample	
5	Spot/Line defect	Light dot,Dim spot,(Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	Minor
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc.	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

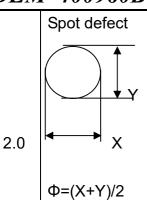
8.1.4 Criteria (Visual)

Number nems Citeria(min)		Number	Items	Criteria(mm)
------------------------------	--	--------	-------	--------------

DEM 400960B VMX-PW-N

Product Specification

LM 400700D	V 1V1/X-1 VV-1 V	Ττυμμεί Βρεείμεμιο
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height	(1) The edge of LCD broken	
L: Length of ITO,		X Y Z
T: Height of LCD		≤3.0mm <inner border="" line="" of="" seal="" td="" the="" ≤t<=""></inner>
	(2)LCD corner broken	X Y Z ≤3.0mm ≤L ≤T
	(3) LCD crack	Crack Not allowed



① light dot (black/white spot , pinhole, stain, etc.)

Zone	Acceptable Qty			
Size (mm)	A	В	С	
Ф≤0.15	Ignore			
0.15<Φ≤0.25	3(distance ≧ 10mm)	lanoro		
0.25<Φ≤0.4	2(distance ≧ 10mm)	Ignore		
Ф>0.4	0			

② Dim spot (light leakage、dent、dark spot, etc)

Zone	Acceptable Qty			
Size (mm)	A	В	С	
Ф≤0.15	Ignore			
0.15<Φ≤0.25	3(distance ≥ 10mm)	Ignore		
0.25<Φ≤0.4	2(distance ≥ 10mm)	.9.10.0		
Ф>0.4	0			

③ Polarizer accidented spot

Zone	Acceptable Qty		
Size (mm)	A B		С
Ф≤0.2	Ignore		
0.2<Φ≤0.5	2(distance ≧ 10mm)		Ignore
Ф>0.5	0		

3 Polarizer Bubble

Zone	Acceptable Qty		
Size (mm)	А	В	С
Ф≤0.2	Ignore		
0.2<Φ≤0.4	3(distance≧10mm)		Ignore
Ф>0.4	0		

		Item	Zone A	Acceptable Qty
		Random	N≤2	
	Bright dot	2 dots adjacent	N≤0	
			3 dots adjacent	N≤0
			Random	N≤2
		Dark dot	2 dots adjacent	N≤0
			3 dots adjacent	N≤0
	Distance	 Minimum Distance Between Bright dots. Minimum Distance Between dark dots Minimum Distance Between dark and bright dot. 	5mm	
		Total bright a	and dark dot	N≤4
		Note:		
		A) Bright dot	: Dots appear bright and unchanged	d in size in which
		LCD pane	el is displaying under black pattern.	
		B) Dark dot:	Dots appear dark and unchanged in	size in which LC
		panel is d	isplaying under pure red, green, blue	e picture.
	C) 2 dot adja Picture:	cent = 1 pair = 2 dots		
	2 dot adja	cent 2 dot adjacent		

Product Specification

	Line defect (LCD					
	/Polarizer backlight		Length(mm)	Acceptable Qty		
	black/white line,	Width(mm)		Α	В	С
	scratch, stain)	Ф≤0.05	Ignore	Ignore		
4.0	$\overline{\Phi}$ W: width, L: length	0.05 <w≤0.06< td=""><td>L≤4.0</td><td>N≤3</td><td colspan="2">N≤3 Ignore</td></w≤0.06<>	L≤4.0	N≤3	N≤3 Ignore	
		0.06 <w≤0.08< td=""><td>L≤3.0</td><td>N≤2</td><td></td><td></td></w≤0.08<>	L≤3.0	N≤2		
N : Count		W>0.08	W>0.08 Define as spot defect			
	Electronic Compone	Not allow missing parts, solderless connection, cold solder joint, m				er joint, mis
5.0	nts SMT.	match, The positive and negative polarity opposite				
6.0	Display color& Brigh tness.	 Color: Measuring the color coordinates, The measurement standar d according to the datasheet or samples. Brightness: Measuring the brightness of White screen, The measu rement standard according to the datasheet or Samples. 				
7.0	LCD Mura/Waving/	Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.				
	Hot spot					

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

9. Reliability Test Result

Item	Condition	Inspection			
		after test			
High Temperature Operating	+85°C,96h				
Low Temperature Operating	-30°C, 96h				
High Temperature Storage	+85°C, 96h	Increation ofter Abours			
Low Temperature Storage	-30°C, 96h	Inspection after ~4hours storage at room			
High Temperature & High +60°C, 90% RH ,96h		temperature, the sample			
Humidity Operating		shall be free from defects:			
Thermal Shock (Non-operation)	-30°C, 30 min ↔ +80°C, 30 min, Change time: 5min 20CYC.	 Air bubble in the LCD; Non-display; 			
	gg	z. Non-display,			
	C=150pF, R=330,5points/panel	3. Missing segments/line;			
ESD test	Air:±8kV, 5times; Contact:±6kV, 5 times;	4. Glass crack;			
	(Environment: 15°C~35°C, 30%~60%).	5. Current IDD is twice			
	Frequency range: 10~55Hz, Stroke: 1.5mm	higher than initial value.			
Vibration (Non-operation)	Sweep:10Hz~55Hz~10Hz 2 hours for each direction				
	of X.Y.Z. (6 hours for total) (Package condition).				
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM BOX)				

Remark:

- 1. The test samples should be applied to only one test item.
- 2. Sample size for each test item is 5~10pcs.
- 3. For Damp Proof Test, Pure water (Resistance > $10M\Omega$) should be used.
- 4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.

 Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.

 If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
 Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.

10.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0°C to 35°C and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.