Display Elektronik GmbH

DATA SHEET

TFT MODULE

DEM 4001280B VMH-PW-N

7,84“ TFT

Product Specification

Version: 1

17.04.2025

Revision History

Date	Rev. No.	Page	Summary
15.04.2025	0	ALL	FIRST ISSUE
17.04.2025	1	P4	UPDATE DISPLAY MODE

Contents

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This module is composed of a transmissive type TFT-LCD Panel, driver circuit, backlight unit. The resolution of a 7.84'' TFT-LCD contains 400x1280 pixels, and can display up to 16.7Million colors.

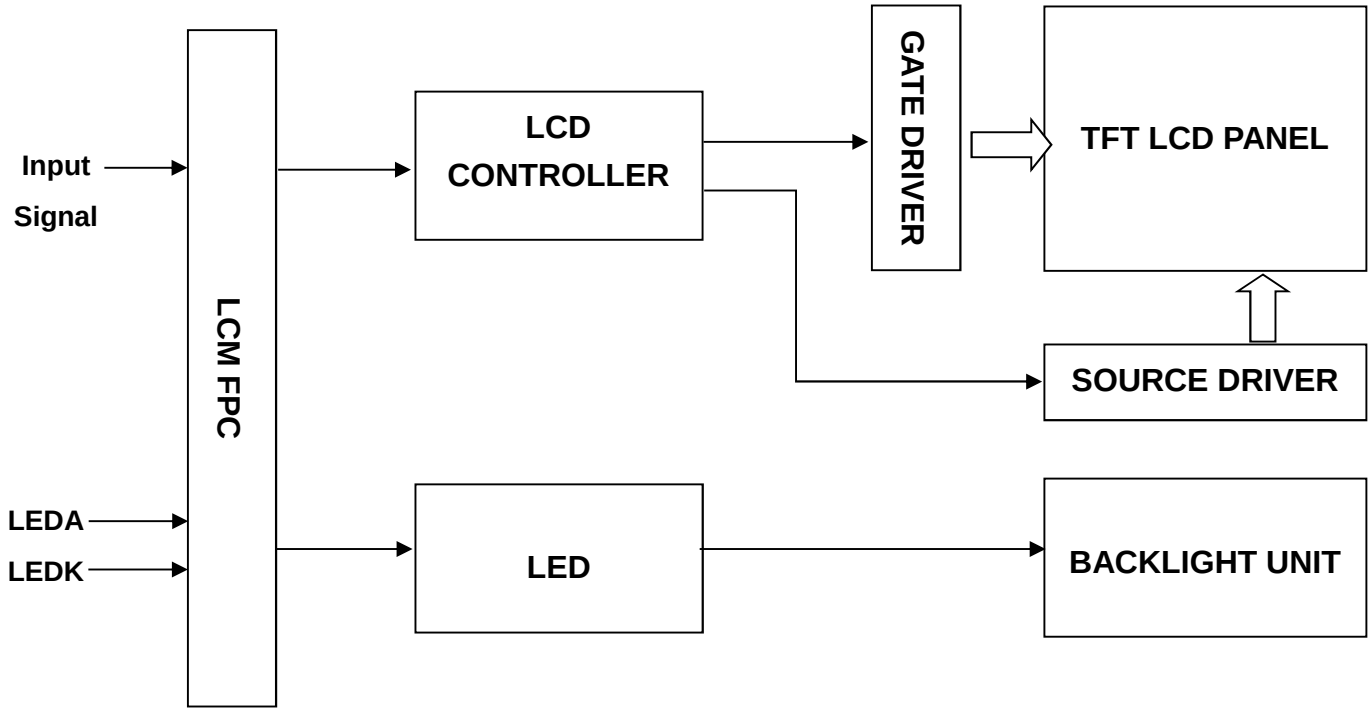
* Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display Area(AA)	59.40 x 190.08 (7.84 Inch)	mm	-
Driver Element	TFT Active Matrix	-	-
Display Colors	16.7 Million	colors	-
Number of Pixels	400 x RGB x 1280	dots	-
TFT Pixel Arrangement	RGB Vertical Stripe	-	-
Pixel Pitch	0.0495 x 0.1485	mm	-
Viewing Angle	ALL	o'clock	-
TFT Controller IC	GC9703C (Galaxycore)	-	-
LCM Interface	3/4-Lane MIPI	-	-
Display Mode	IPS, Transmissive, Normally Black	-	-
Operating Temperature	-20°C to +70°C	°C	-
Storage Temperature	-30°C to +80°C	°C	-

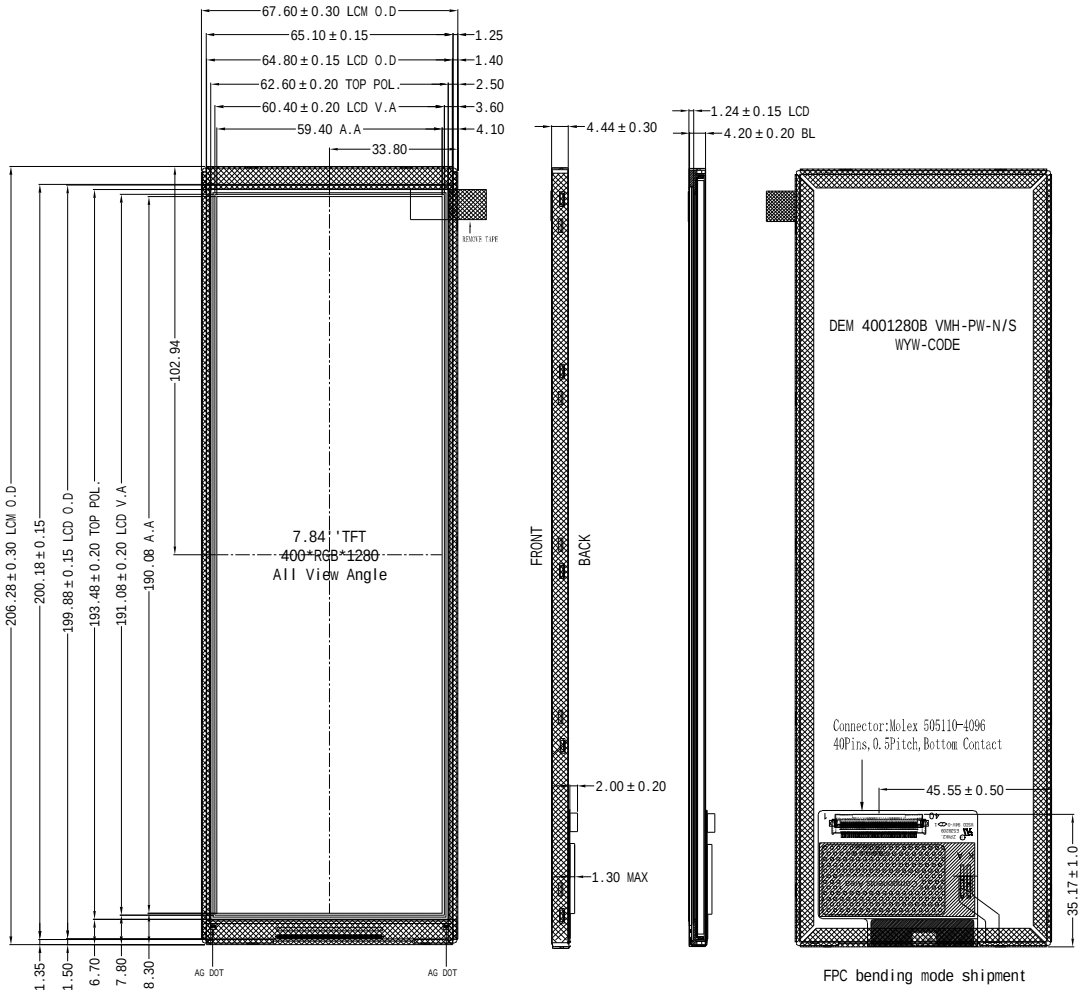
* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	-	67.60	-	mm	-
	Vertical(V)	-	206.28	-	mm	-
	Depth(D)	-	4.44	-	mm	-
Weight		-	84	-	g	-

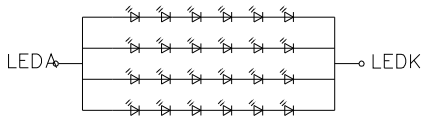
1. Block Diagram



2. Outline Dimension



NOTE:
1.DISPLAY TYPE:7.84",TFT-LCD,16.7M COLORS
2.DISPLAY MODE:ADS Normal Black
3.VIEWING DIRECTION:ALL
4.LCM DRIVER IC:GC9703C (COG)
LCM Interface:MIPI-3/4 Lane
5.VCI:3.3V(TYP.),IOVCC:1.65~3.3V
6.OPERATING TEMP: -20°C TO 70°C
STORAGE TEMP: -30°C TO 80°C
7.BACK LIGHT:LED WHITE, 24 LED,160mA,16.8~20.4V
8.RoHS COMPLIANT.



LED(B/L) CIRCUIT

Pin	Name
1	NC
2	VCI
3	IOVCC
4	GND
5	RESET
6	NC
7	GND
8	MIPI_0N
9	MIPI_0P
10	GND
11	MIPI_1N
12	MIPI_1P
13	GND
14	MIPI_CKN
15	MIPI_CKP
16	GND
17	MIPI_2N
18	MIPI_2P
19	GND
20	MIPI_3N
21	MIPI_3P
22	GND
23	NC
24	NC
25	GND
26	NC
27	NC
28	NC
29	NC
30	GND
31	LED-
32	LED-
33	NC
34	NC
35	NC
36	NC
37	NC
38	NC
39	LED+
40	LED+

3. Input Terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	NC	NO Connection	--
2	VCI	Supply Voltage (3.3V).	P
3	IOVCC	I/O power supply voltage.	P
4	GND	Ground.	P
5	RESET	- The external reset input. Initializes the chip with a low input. Be sure to execute a p ower-on reset after supplying power.	I
6	NC	NO Connection	--
7	GND	Ground.	P
8	MIPI_0N	- MIPI DSI differential data pair. (Data lane 0) Leave it open or fix to GND level when not in use.	I/O
9	MIPI_0P		
10	GND	Ground.	P
11	MIPI_1N	- MIPI DSI differential data pair. (Data lane 1) Leave it open or fix to GND level when not in use.	I/O
12	MIPI_1P		
13	GND	Ground.	P
14	MIPI_CLKN	- MIPI DSI differential clock pair Leave it open or fix to GND level when not in use.	I
15	MIPI_CLKP		
16	GND	Ground.	P
17	MIPI_2N	- MIPI DSI differential data pair. (Data lane 2) Leave it open or fix to GND level when not in use.	I/O
18	MIPI_2P		
19	GND	Ground.	P
20	MIPI_3N	- MIPI DSI differential data pair. (Data lane 3) Leave it open or fix to GND level when not in use. -When use 3-lane , Connect to GND	I/O
21	MIPI_3P		
22	GND	Ground.	P
23	NC	NO Connection	--
24	NC	NO Connection	--
25	GND	Ground.	P
26	NC	NO Connection	--

27	NC	NO Connection	--
28	NC	NO Connection	--
29	NC	NO Connection	--
30	GND	Ground.	P
31	LED-	Cathode pin of backlight.	P
32	LED-		
33	NC	NO Connection	--
34	NC	NO Connection	--
35	NC	NO Connection	--
36	NC	NO Connection	--
37	NC	NO Connection	--
38	NC	NO Connection	--
39	LED+	Anode pin of backlight.	P
40	LED+		

4. LCD Optical Characteristics

4.1 Optical Specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal Viewing Angle	700	900	--		(1)(2)
Response Time	Rising	$T_{R+}T_F$		--	30	40	msec	
	Falling							(1)(3)
Color Gamut		S(%)	--	60	62.2	--	%	
Color Filter Chromacicity	White	W_X	--	-0.04	0.2758	+0.04		(1)(4) CF glass
		W_Y	--		0.3035			
	Red	R_X	--		0.6241			
		R_Y	--		0.3386			
	Green	G_X	--		0.2997			
		G_Y	--		0.5642			
	Blue	B_X	--		0.1467			
		B_Y	--		0.0634			
Viewing Angle	Hor.	ΘL	CR>10	75	85	--		(1)(4)
		ΘR		75	85	--		
	Ver.	ΘU		75	85	--		
		ΘD		75	85	--		
Option View Direction		ALL						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding: dark room

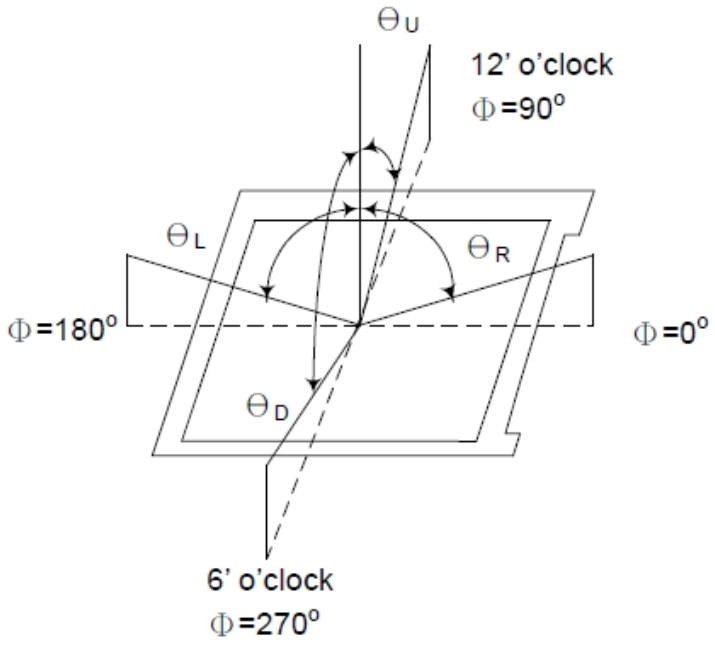
Ambient temperature: 25°C±2°C

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

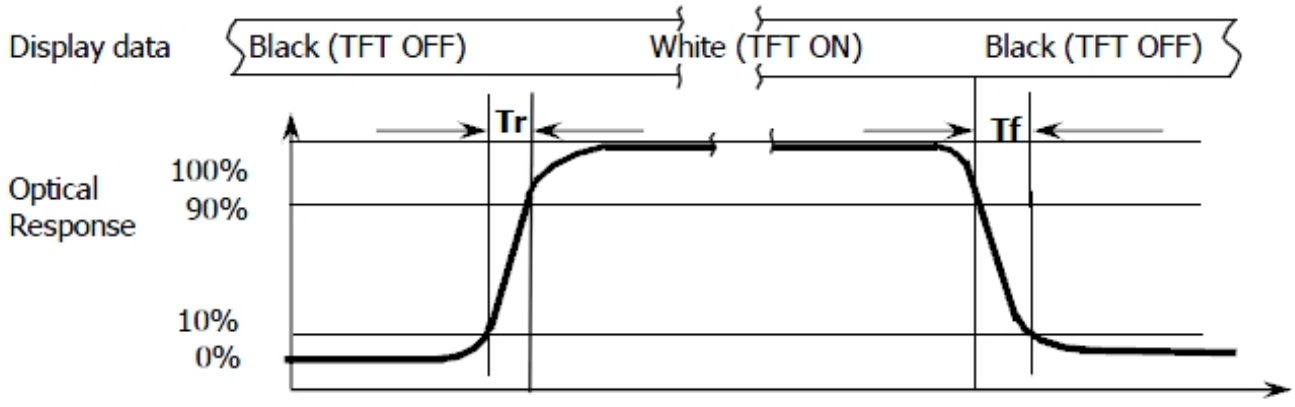
Note (1): Definition of Viewing Angle:



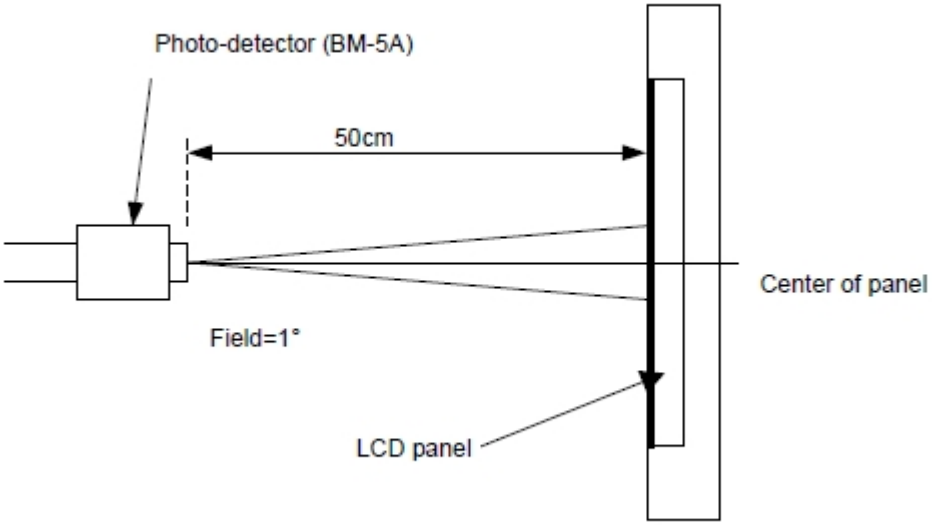
Note (2): Definition of Contrast Ratio (CR): measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VCI	-0.3	4.6	V	Note1
Digital Interface Supply Voltage	IOVCC	-0.3	3.3	V	--
Operating Temperature	T_{OP}	-20	+70	°C	--
Storage Temperature	T_{ST}	-30	+80	°C	--

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged.
Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.5	2.8	3.3	V	--
Digital Interface Supply Voltage	IOVCC	1.65	1.8	3.3		
Normal Mode Current Consumption	IDD	--	35	80	mA	--
Level Input Voltage	V_{IH}	0.7 IOVCC	--	IOVCC	V	--
	V_{IL}	-0.3	--	0.3 IOVCC	V	--
Level Output Voltage	V_{OH}	0.8* IOVCC	--	IOVCC	V	--
	V_{OL}	GND	--	0.2 IOVCC	V	--

5.3 LED Backlight Characteristics

The Backlight System is edge-lighting type with 24 chips White LED

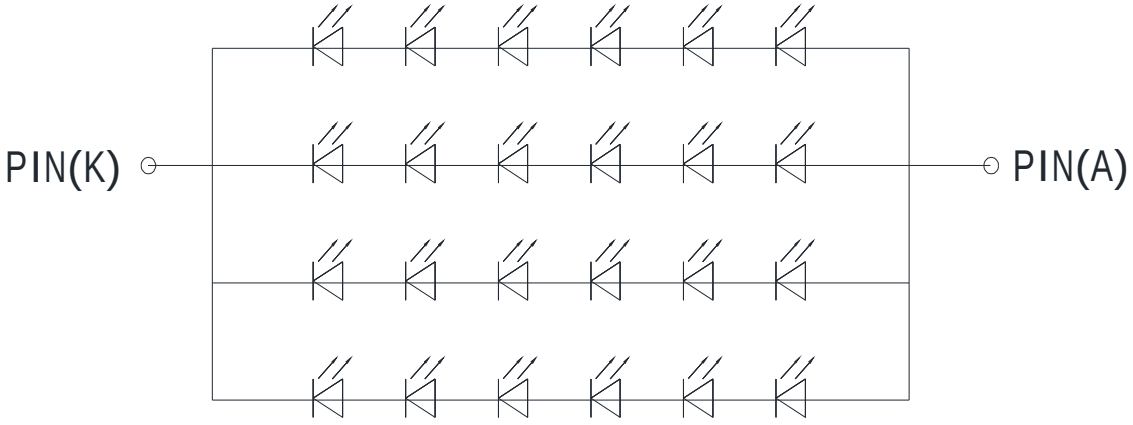
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	--	160	--	mA	--
Forward Voltage	V_F	--	18.2	--	V	--
LCM Luminance	L_V	950	1100	--	cd/m2	Note3
LED Lifetime	Hr	50000			Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25°C±3°C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=160mA.

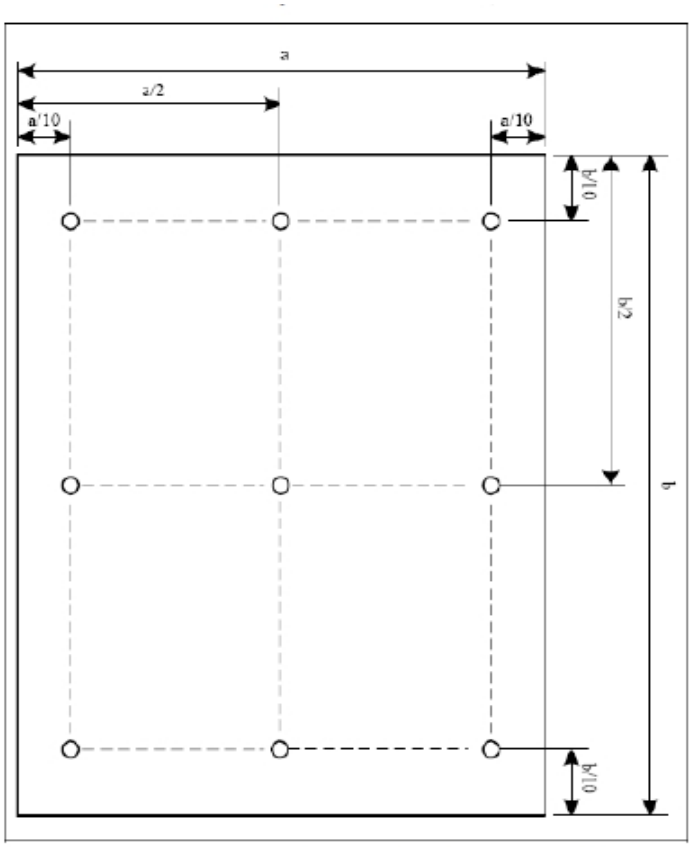
The LED lifetime could be decreased if operating IL is larger than 160mA.

The constant current driving method is suggested.



LED(B/L) CIRCUIT

NOTE 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

6. MIPI Interface AC Characteristics

6.1 High Speed Mode-Clock Timings

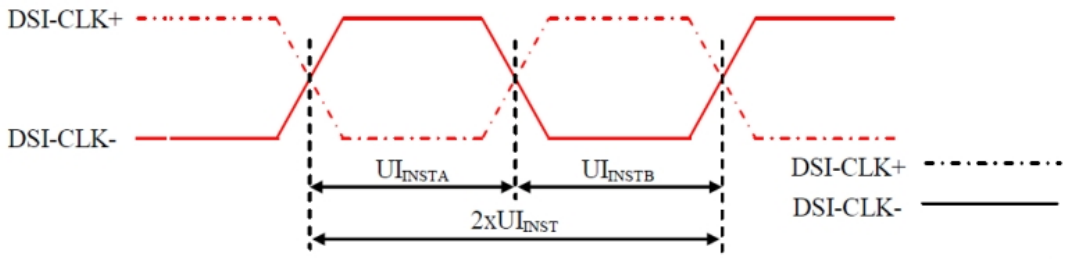


Figure 114 DSI Clock Channel Timing

Table 45 DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
DSI-CLK+/-	UI_{INSTA}, UI_{INSTB}	UI instantaneous Half	2	12.5	ns

Note: $UI = UI_{INSTA} = UI_{INSTB}$

6.2 High Speed Mode-Clock/Data Timings

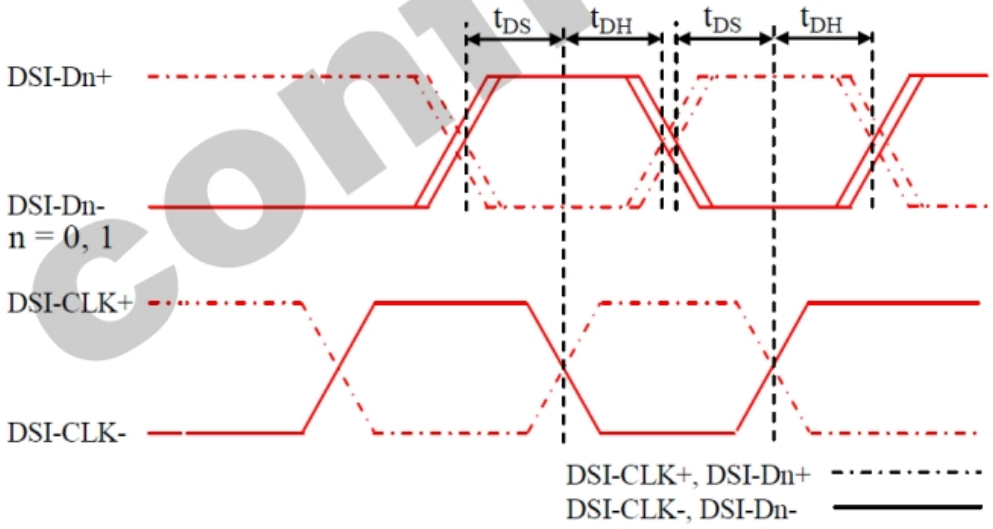


Figure 115 DSI Data to Clock Channel Timings

Table 46 DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DSI-Dn+/- , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

6.3 High Speed Mode-Rising and Falling Timings

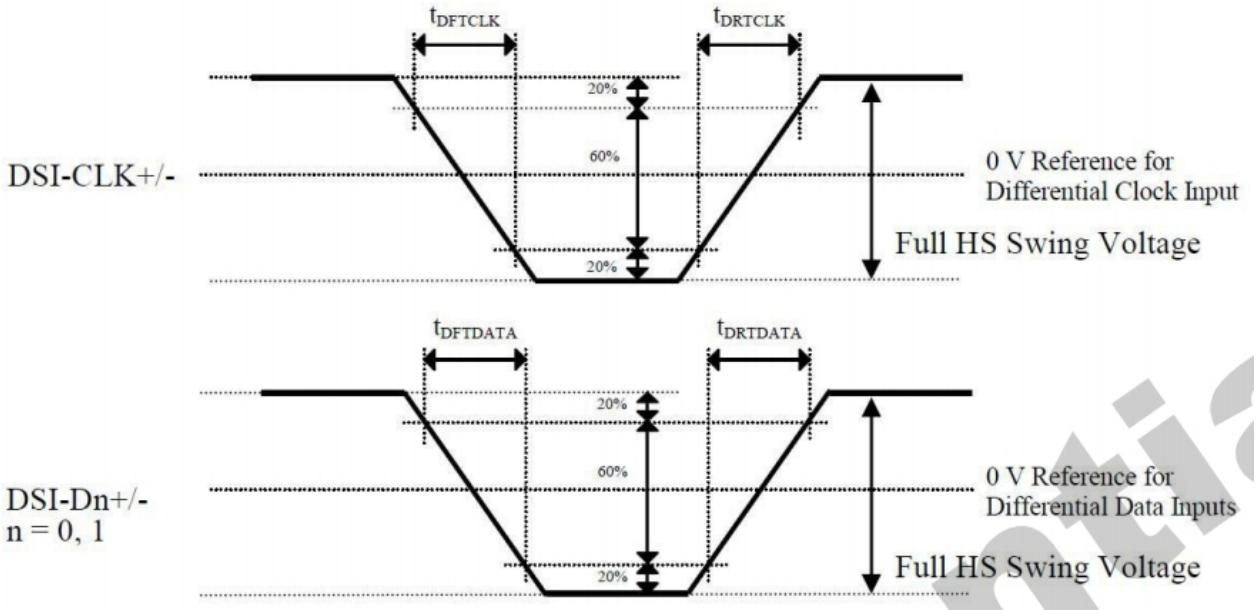


Figure 116 Rise and Fall Timings on Clock and Data Channels

Table 47 Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification			
			Min	Typ	Max	Unit
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLK+/-	-	-	150 (Note)	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note)	ps
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLK+/-	-	-	150 (Note)	ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note)	ps

Note:The display module has to meet timing requirements, what are defined for the transmitter (MPU) on MIPI D-Phy standard

6.4 Low Speed Mode-Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MPU to the Display Module (GC9703C) sequence below.

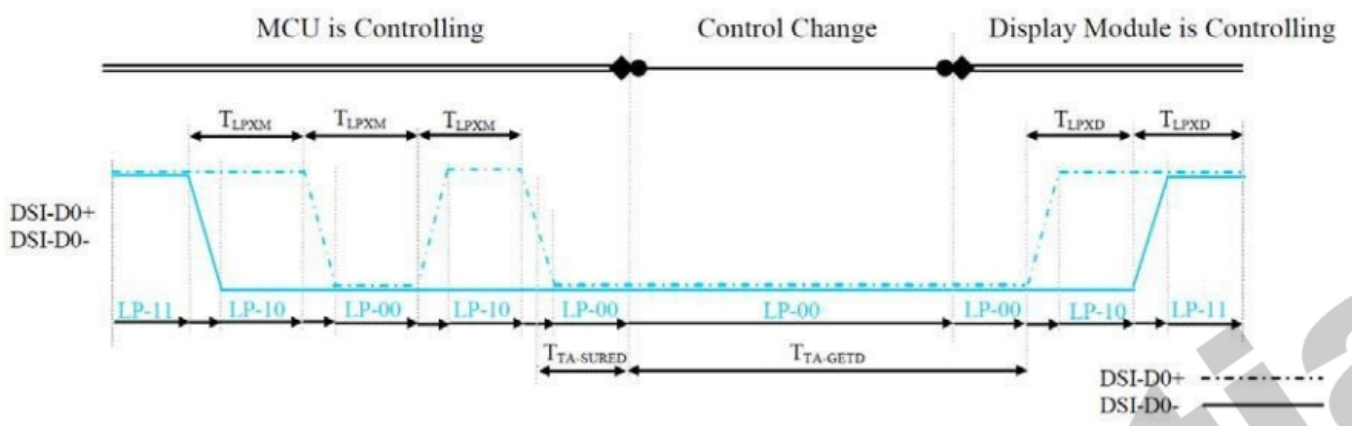


Figure 117 BTA from the MPU to the Display Module

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA)from the Display Module (GC9703C) to the MPU sequence below.

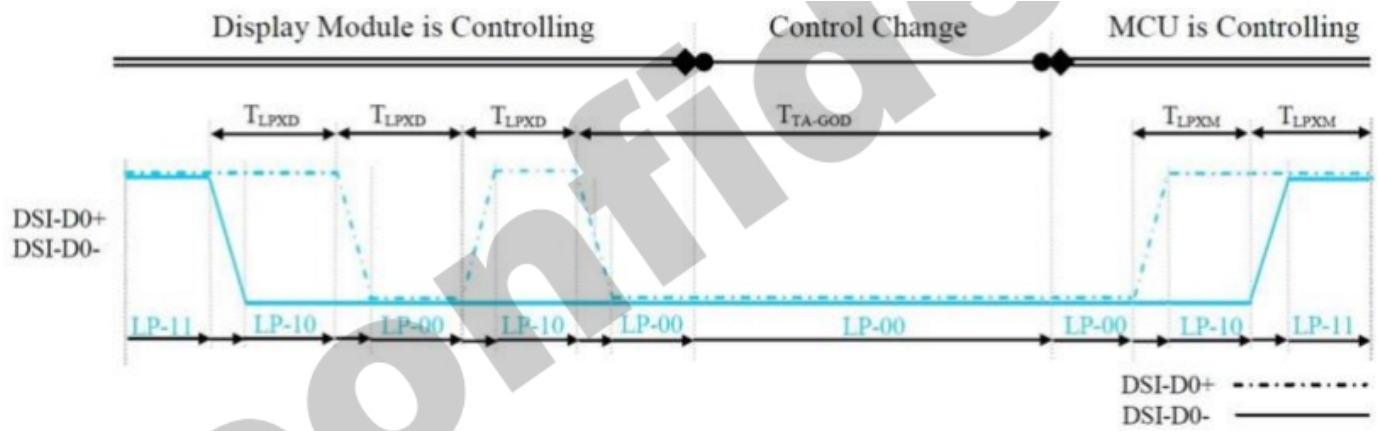


Figure 118 BTA from the Display Module to the MPU

Table 48 Low Power State Period Timings-A

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01,LP-10 or LP-11 periods MPU □ Display Module(GC9703C)	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01,LP-10 or LP-11 periods Display Module(GC9703C) □ MPU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module' (GC9703C) starts driving	T_{LPXD}	$2XT_{LPXD}$	ns

Table 49 Low Power State Period Timings-B

Signal	Symbol	Description	Time	Unit
DS-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (GC9703C)	$5XT_{LPXD}$	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4XT_{LPXD}$	ns

6.5 Data Lanes from Low Power Mode to High Speed Mode

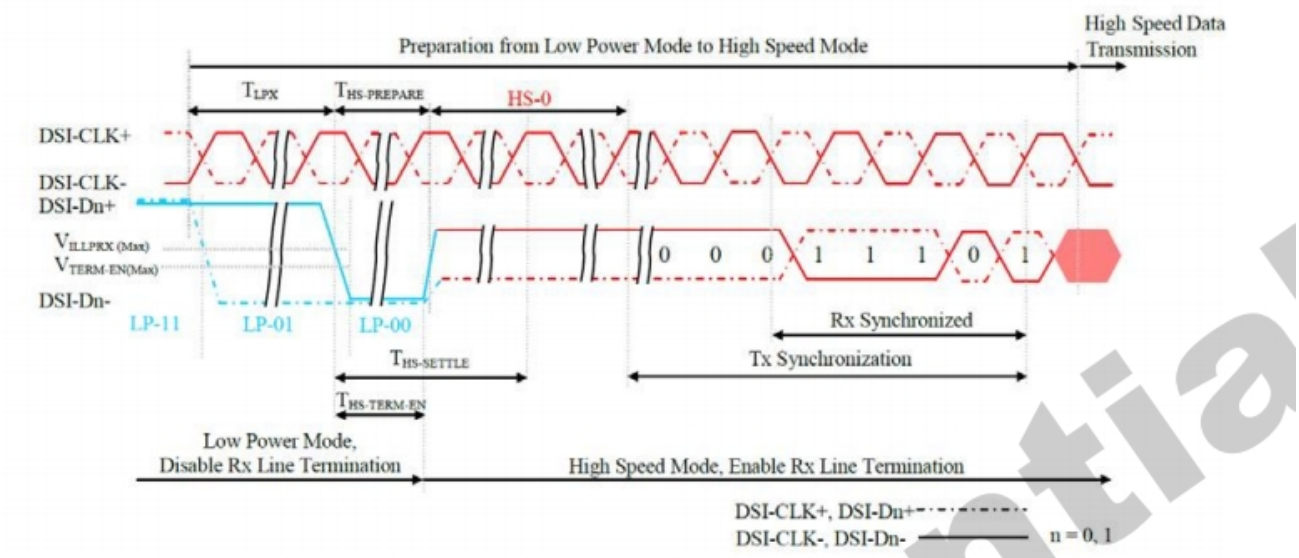


Figure 119 Data Lanes – Low Power Mode to High Speed Mode Timings

Table 50 Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

6.6 Data Lanes from High Speed Mode to Low Power Mode

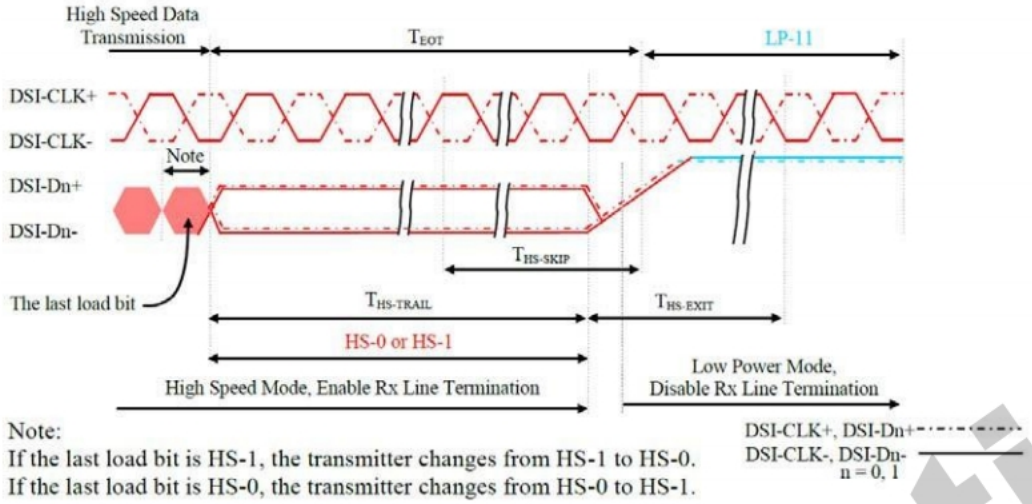


Figure 120 Data Lanes – High Speed Mode to Low Power Mode Timings

Table 51 Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (GC9703C) to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

6.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

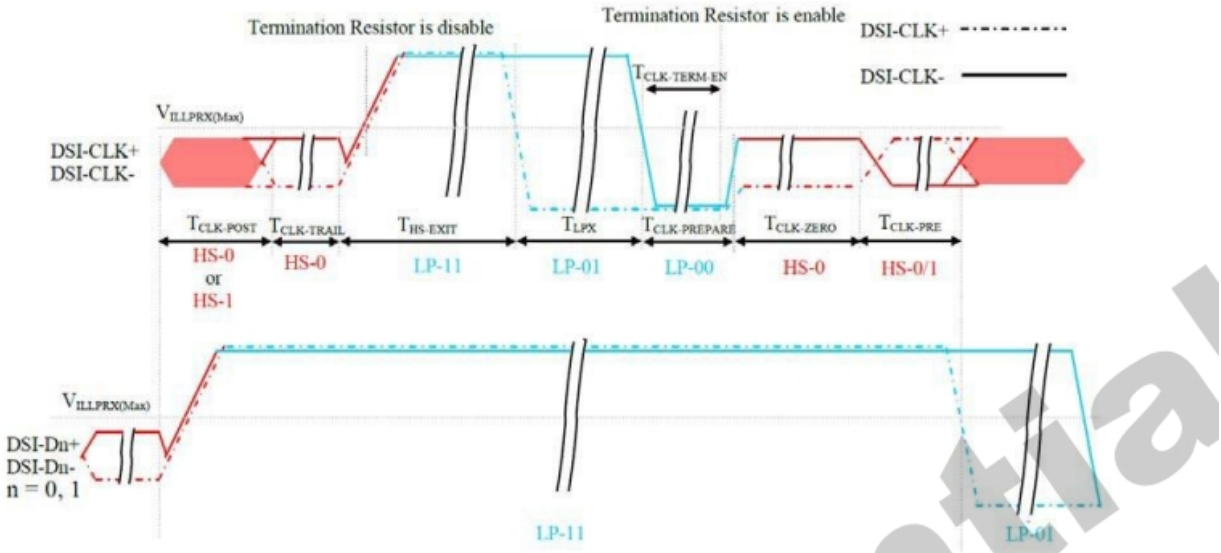


Figure 121 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Table 52 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MPU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
SI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

6.8 Reset Input Timing

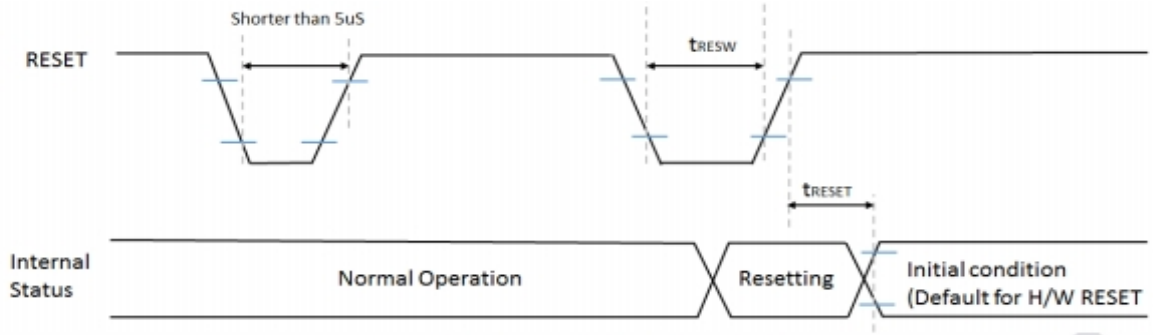


Figure 4-13 Reset Input Timing

Table 4-2 Reset Input Timing

Signal	Symbol	Parameter	Description	Specification			Unit	Notes
				MIN	TYP	MAX		
RESET	tRESW	Reset "L" pulse width		10			uS	1
	tRESET	Reset complete time	When reset applied during Sleep in mode			5	mS	2
			When reset applied during Sleep Out mode			120	mS	5

***Note* 1:** Condition : Ta =25℃.

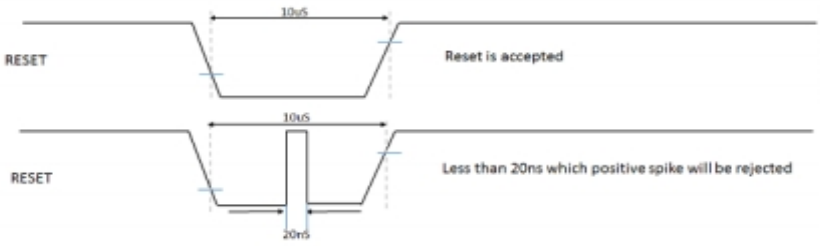
***Note* 2:** Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table below.

RESET Pulse	Action
Less than 5us	Reset Rejected
More than 10uS	Reset
Between 5us and 10uS	Reset Start

***Note* 2:** During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for H/W RESET.

Note3: During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W RESET complete time (tRESET) within 5ms after a rising edge of RESET.

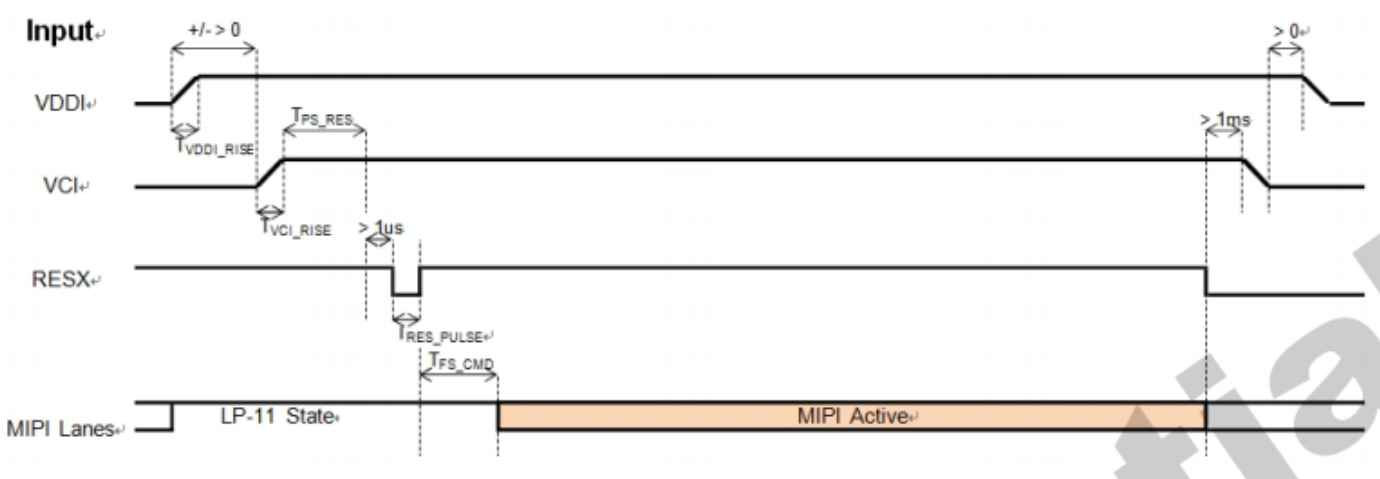
***Note 4*:** Spike Rejection also applies during a valid reset pulse as shown below:



***Note 5*:** It is necessary to wait 5ms after releasing RESET when sending commands, and Sleep Out command can not be sent within 120ms.

6.9 Power ON/OFF Sequence

Power Mode



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	VCI Rise time	10	-	-	us
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	50	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

Power on/off sequence with 2 Power Mode

7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

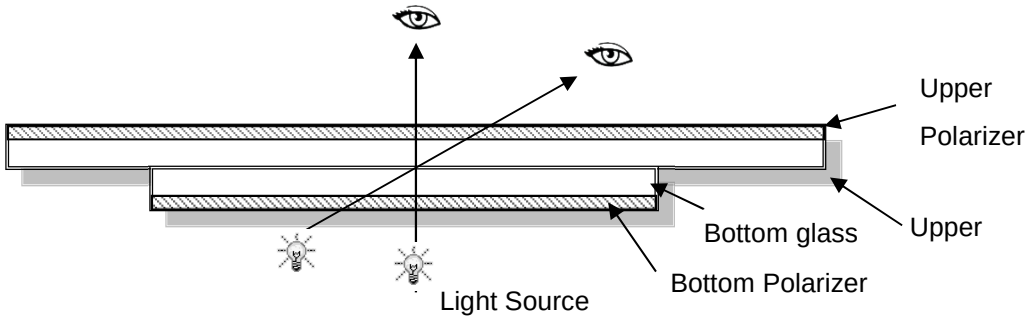
Temperature: 25°C ± 5°C

Humidity: 65% ± 10%RH

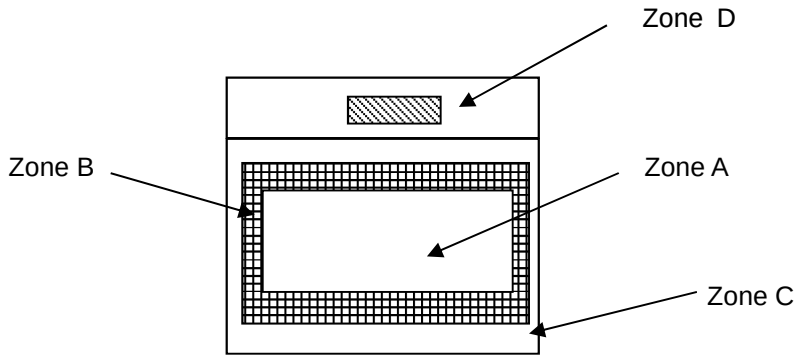
Viewing Angle: Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance: 30-50cm



7.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

Note: As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

7.1.3 Sampling Plan

According to GB/T 2828-2003; Normal Inspection, Class II

AQL:

Major Defect	Minor Defect
0.65	1.5

LCD: Liquid Crystal Display, LCM: Liquid Crystal Module

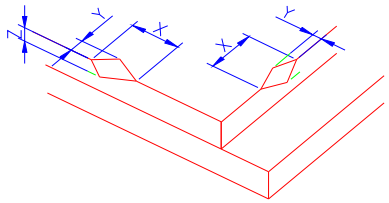
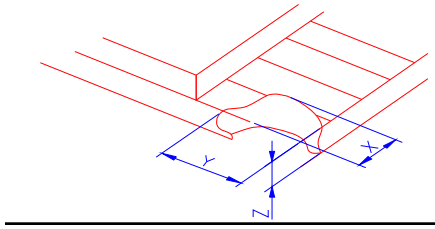
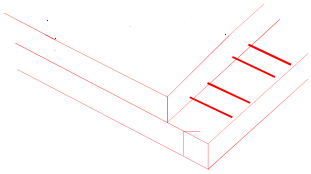
No	Items to be inspected	Criteria	Classification of Defects
1	Functional Defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc…	Major
2	Missing	Missing components and etc…	
3	Outline Dimension	Overall outline dimension beyond the drawing is not allowed,deformation and etc…	
4	Color Tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line Defect	Light dot,Dim spot,(Note1) Polarizer Air Bubble, Polarizer accidented spot and etc…	
6	Soldering Appearance	Good soldering , Peeling off is not allowed and etc…	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

Note1:

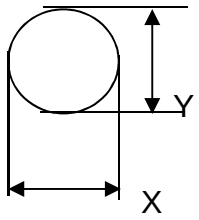
a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

7.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

2.0 Spot defect



Φ=(X+Y)/2

① light dot（ black/white spot , pinhole, stain，etc.）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧10mm)		
0.25<Φ≤0.4	2(distance≧10mm)		
Φ>0.4	0		

② Dim spot（light leakage、dent、dark spot，etc）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧10mm)		
0.25<Φ≤0.4	2(distance≧10mm)		
Φ>0.4	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.5	2(distance≧10mm)		
Φ>0.5	0		

④Polarizer Bubble

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.4	2(distance≧10mm)		
0.4<Φ≤0.5	1		
Φ>0.5	0		

3.0 LCD Pixel defect

Pixel bad points

Item	Zone A	Acceptable Qty
Bright dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Dark dot	Random	N≤3
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm
Total bright and dark dot		N≤4

Note:

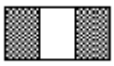
A) Bright dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

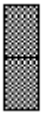
C) 2 dot adjacent = 1 pair = 2 dots

Picture:

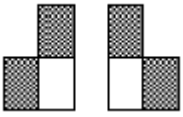
2 dot adjacent



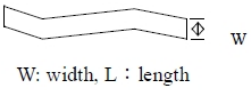
2 dot adjacent



2 dot adjacent (vertical)



2 dot adjacent (slant)

<table>
<tr>
<td>4.0</td>
<td>Line defect (LCD /Polarizer backlight black/white line, scratch, stain)
 

N：Count</td>
<td>
<table>
<tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.05</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L≤5.0</td><td colspan="2">N≤3</td></tr>
<tr><td>0.06<W≤0.08</td><td>L≤4.0</td><td colspan="2">N≤2</td></tr>
<tr><td>W>0.08</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td>
</tr>
<tr>
<td>5.0</td>
<td>Electronic Components SMT.</td>
<td>Not allow missing parts，solderless connection，cold solder joint，mismatch，The positive and negative polarity opposite</td>
</tr>
<tr>
<td>6.0</td>
<td>Display color& Brightness.</td>
<td>1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td>
</tr>
<tr>
<td>7.0</td>
<td>LCD Mura/Waving/ Hot spot</td>
<td>Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.</td>
</tr>
</table>

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

8. Reliability Test Result

Remark:

Item	Condition	Inspection after test
High Temperature Operating	+70°C, 96h	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1. Air bubble in the LCD; 2. Non-display; 3. Missing segments/line; 4. Glass crack; 5. Current IDD is twice higher than initial value.
Low Temperature Operating	-20°C, 96h	
High Temperature Storage	+80°C, 96h	
Low Temperature Storage	-30°C, 96h	
High Temperature & High Humidity Operating	+60°C, 90% RH, 96h	
Thermal Shock (Non-operation)	-20°C,30 min ↔ +70°C, 30 min, Change time: 5min 20CYC	
ESD Test	C=150pF, R=330, 5points/panel Air:±8kV, 5times; Contact:±6kV, 5 times (Environment: 15°C ~ 35°C, 30%~60%).	
Vibration (Non-operation)	Frequency Range: 10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total)	
Box Drop Test	1 Corner 3 Edges 6 faces, 80㎝(MEDIUM	

1. The test samples should be applied to only one test item.
2. Sample size for each test item is 5~10pcs.
3. For Damp Proof Test, Pure water (Resistance > 10MΩ) should be used.
4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
5. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6. The color fading mura of polarizing filter should not care.

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the “Power ON” condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0°C to 35°C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.