

Display Elektronik GmbH

DATA
SHEET

TFT MODULE

DEM 4001280A VMH-PW-N
(C-TOUCH)
7,84“ TFT + C-TP

Product Specification

Version: 1

16.04.2025

Revision History

[illegible]

Contents

* Description.....	4
* CTP Features	4
1. Block Diagram	5
Signal.....	5
2. Outline Dimension.....	6
3. Input Terminal Pin Assignment	7
3.1 TFT PIN Definition	7
3.2 CTP PIN Definition.....	8
4. LCD Optical Characteristics	9
4.1 Optical Specification	9
5. TFT Electrical Characteristics	12
5.1 Absolute Maximum Rating (Ta=25 VSS=0V).....	12
5.2 DC Electrical Characteristics	12
5.3 LED Backlight Characteristics.....	13
6. RGB Interface Characteristics.....	15
6.1 RGB Interface Selection	15
6.2 RGB Interface Timing characteristics	17
7. CTP Specification.....	18
7.1 Electrical Characteristics	18
7.1.1 Absolute Maximum Rating	18
7.1.2 DC Electrical Characteristics (Ta=25°C)	18
7.2 AC Electrical Characteristics	19
8. LCD Module Out-Going Quality Level	24
8.1 VISUAL & FUNCTION INSPECTION STANDARD.....	24
8.1.1 Inspection Conditions	24
8.1.2 Definition	24
8.1.3 Sampling Plan.....	25
8.1.4 Criteria (Visual)	26
9. Reliability Test Result	32
10. Cautions and Handling Precautions.....	33
10.1 Handling and Operating the Module.....	33
10.2 Storage and Transportation.....	33

DEM 4001280A VMH-PW-N(C-TOUCH) Product Specification

*** Description**

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit, capacitance touch panel, Backlight unit. The resolution of a 7.84" TFT-LCD contains 400x1280 pixels, and can display up to 16.7 Million colors.

*** Features**

General Information Items	Specification	Unit	Note
	Main Panel		
Display Area (AA)	59.40 x 190.08 (7.84 Inch)	mm	-
Driver Element	TFT Active Matrix	-	-
Display Colors	16.7 Million	colors	-
Number of Pixels	400 x RGB x 1280	dots	-
TFT Pixel Arrangement	RGB Vertical Stripe	-	-
Pixel Pitch	0.0495 x 0.1485	mm	-
Viewing Angle	ALL	o'clock	-
TFT Controller IC	GC9704C (Galaxycore)	-	-
LCM Interface	16/18/24-Bit-RGB	-	-
Display Mode	IPS / Transmissive / Normally Black	-	-
Operating Temperature	-20°C to +70°C	°C	-
Storage Temperature	-30°C to +80°C	°C	-
Module Bonding Technology	Use Optical bonding between LCM and CTP	-	-

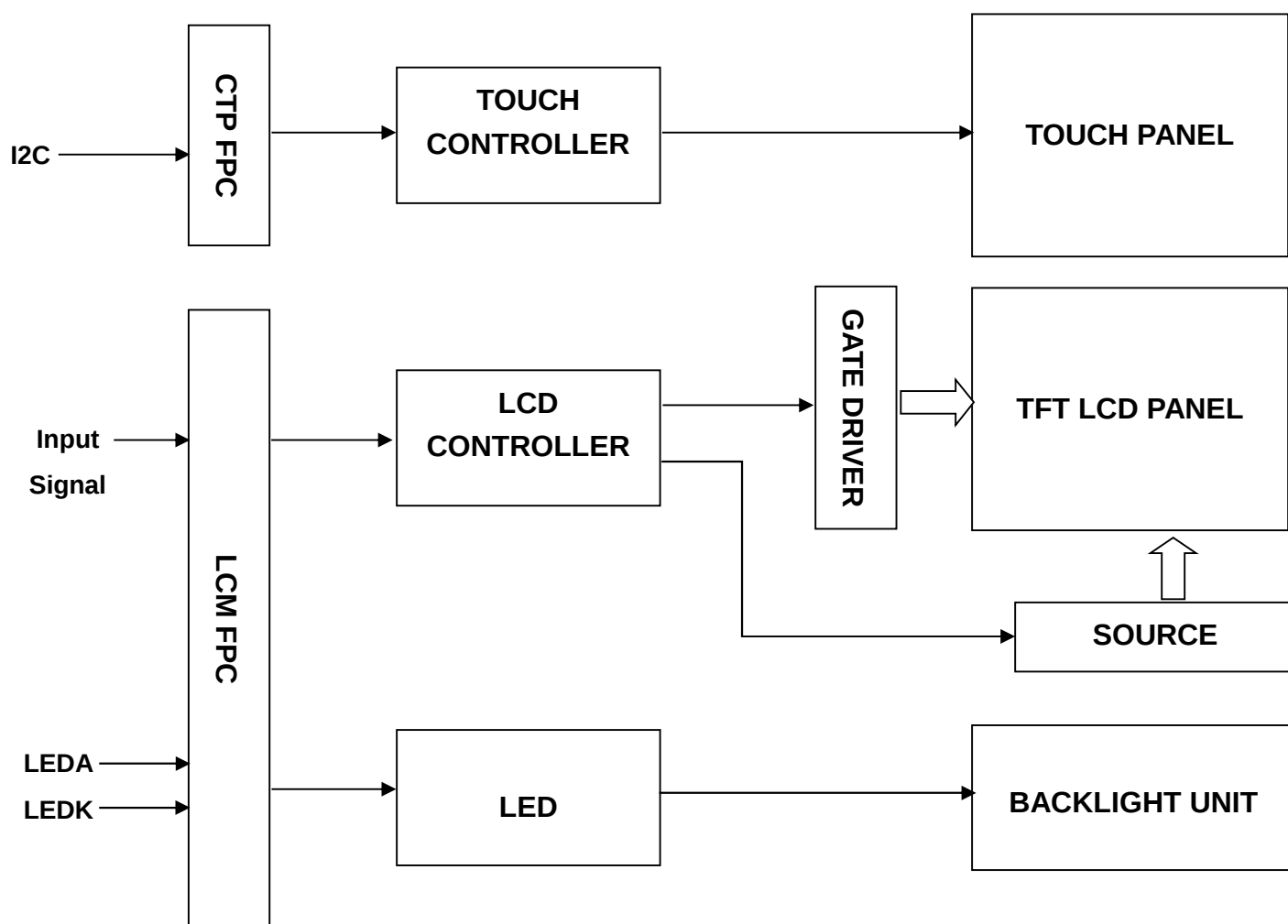
*** CTP Features**

General Information Items	Specification	Unit	Note
	Main Panel		
Resolution	400 x 1280	-	-
Structure	G+F+F	-	-
Controller IC	GT9271 (Goodix)	-	-
Interface	I2C	-	-
Slave Address	0x5D(7bit) or 0x14(7bit)	-	-
Touch Mode	Ten points and Gestures	-	-
Logic level	3.3	V	-
Surface	-	-	-

* Mechanical Information

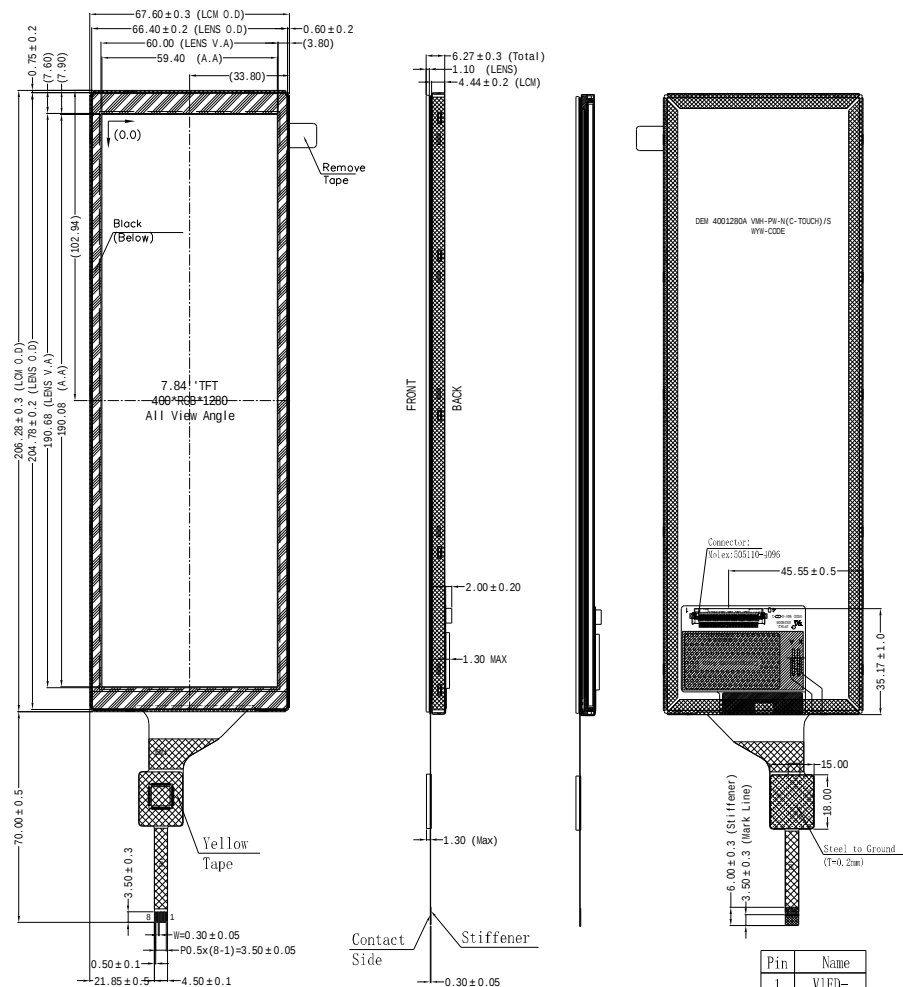
Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	-	67.60	-	mm	-
	Vertical(V)	-	206.28	-	mm	-
	Depth(D)	-	6.27	-	mm	-
Weight		-	TBD	-	g	-

1. Block Diagram



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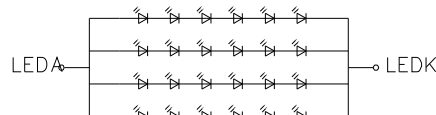
2. Outline Dimension



NOTE:

- 1.DISPLAY TYPE:7.84",TFT-LCD,16.7M COLORS
- 2.DISPLAY MODE:Normally Black,IPS
- 3.VIEWING DIRECTION:FREE
- 4.LCM Driver IC: GC9704C(COG)
- 5.LCM Interface: RGB
- 6.Touch Mode: CTP
Touch Driver IC:GT9271
Touch Interface:IIC
- 7.VCI: 3.3V ,IOVCC: 1.65-3.3V
- 8.OPERATING TEMP: -20 °C TO 70 °C
STORAGE TEMP: -30 °C TO 80 °C
- 9.BACK LIGHT: LED WHITE, 24 LED,160mA,16.8-20.4V
- 10.RoHS COMPLIANT.

LED(B/L) CIRCUIT



Pin	Name
1	VLED-
2	VLED+
3	GND
4	VDD
5	R0
6	R1
7	R2
8	R3
9	R4
10	R5
11	R6
12	R7
13	G0
14	G1
15	G2
16	G3
17	G4
18	G5
19	G6
20	G7
21	B0
22	B1
23	B2
24	B3
25	B4
26	B5
27	B6
28	B7
29	GND
30	PCLK
31	DISP
32	HSYNC
33	VSYNC
34	DE
35	NC
36	GND
37	XR(NC)
38	YD(NC)
39	XL(NC)
40	YU(NC)

Pin	Logic
1	GND
2	NC
3	VDD
4	SCL
5	SDA
6	INT
7	RST
8	GND

3. Input Terminal Pin Assignment**3.1 TFT PIN Definition**

NO.	SYMBOL	DISCRIPTION	I/O
1	VLED-	Cathode pin of backlight	P
2	VLED+	Anode pin of backlight	P
3	GND	Ground.	P
4	VDD	Supply Voltage (3.3Volt)	P
5	R0	Red data input.	I/O
6	R1	Red data input.	I/O
7	R2	Red data input.	I/O
8	R3	Red data input.	I/O
9	R4	Red data input.	I/O
10	R5	Red data input.	I/O
11	R6	Red data input.	I/O
12	R7	Red data input.	I/O
13	G0	Green data input.	I/O
14	G1	Green data input.	I/O
15	G2	Green data input.	I/O
16	G3	Green data input.	I/O
17	G4	Green data input.	I/O
18	G5	Green data input.	I/O
19	G6	Green data input.	I/O
20	G7	Green data input.	I/O
21	B0	Blue data input.	I/O
22	B1	Blue data input.	I/O
23	B2	Blue data input.	I/O
24	B3	Blue data input.	I/O
25	B4	Blue data input.	I/O
26	B5	Blue data input.	I/O

DEM 4001280A VMH-PW-N(C-TOUCH) Product Specification

27	B6	Blue data input.	I/O
28	B7	Blue data input.	I/O
29	GND	Ground.	P
30	PCLK	Dot clock signal for RGB interface operation.	I
31	DISP	Standby setting for testing, it should be connected to VDD in normal operation mode. If connected to GND, the IC is in standby mode.	I
32	HSYNC	Line synchronizing signal for RGB interface operation.	I
33	VSYNC	Frame synchronizing signal for RGB interface operation.	I
34	DE	Data enable signal for RGB interface operation.	I
35	NC	NC	
36	GND	Ground.	P
37	XR(NC)	NC	
38	YD(NC)	NC	
39	XL(NC)	NC	
40	YU(NC)	NC	

3.2 CTP PIN Definition

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground	P
2	NC	No Connection	-
3	VDD	Supply voltage	P
4	SCL	I2C clock input	I
5	SDA	I2C data input and output	I
6	INT	External interrupt to the host	I
7	RST	External Reset, Low is active	I
8	GND	Ground	P

4. LCD Optical Characteristics

4.1 Optical Specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	$\Theta=0$ Normal Viewing Angle	700	1000	--		(1)(2)
Response Time	Rising	T_{R+T_F}		--	30	40	msec	
	Falling							(1)(3)
Color Gamut		S(%)	--	56	61.35	-	%	
Color Filter Chromaticity	White	W_X	--	-0.04	0.278	+0.04	--	(1)(4)
		W_Y	--		0.307			CA-310
	Red	R_X	--		0.623			
		R_Y	--		0.338			
	Green	G_X	--		0.302			
		G_Y	--		0.561			
	Blue	B_X	--		0.147			
		B_Y	--		0.064			
Viewing Angle	Hor.	Θ_L	CR>10	70	80	--	--	(1)(4)
		Θ_R		70	80	--		
	Ver.	Θ_U		70	80	--		
		Θ_D		70	80	--		
Option View Direction		ALL						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding: dark room

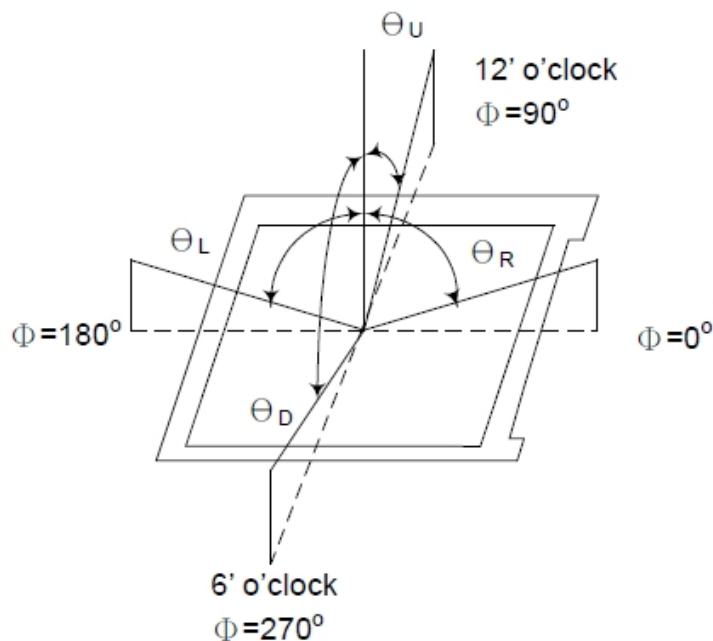
Ambient temperature: 25°C±2°C

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

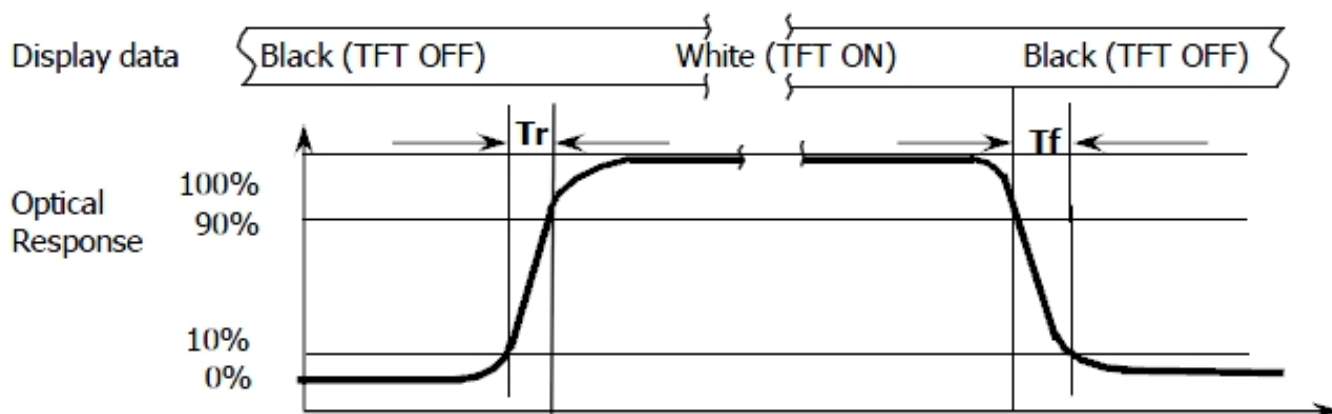
Note (1): Definition of Viewing Angle:



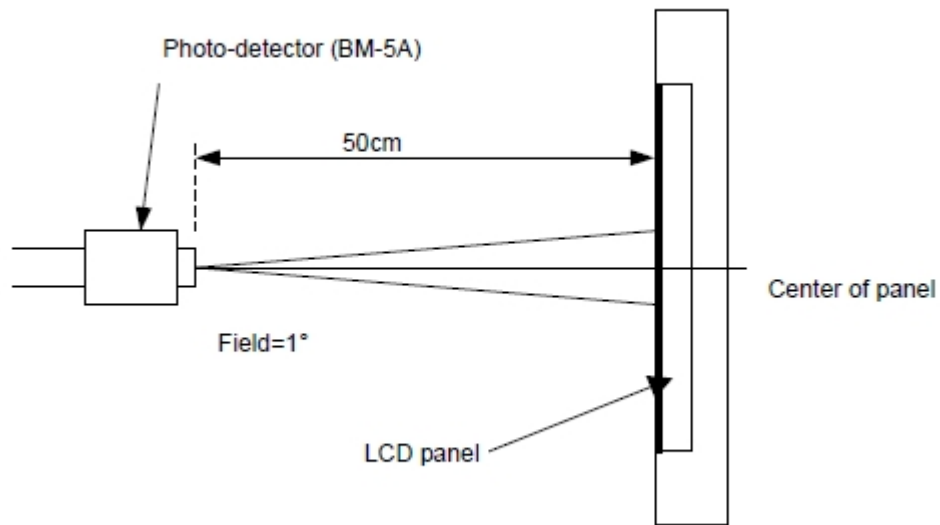
Note (2): Definition of Contrast Ratio(CR): measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



5. TFT Electrical Characteristics**5.1 Absolute Maximum Rating (Ta=25 VSS=0V)**

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VDD	-0.3	4.6	V	Note1
Operating Temperature	T _{OP}	-20	+70	°C	--
Storage Temperature	T _{ST}	-30	+80	°C	--

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged.

Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.5	3.3	3.6	V	--
Normal Mode Current Consumption	IDD	--	50	100	mA	--
Level Input Voltage	V _{IH}	0.7 VDD	--	VDD	V	--
	V _{IL}	-0.3	--	0.3 VDD	V	--
Level Output Voltage	V _{OH}	0.8* VDD	--	VDD	V	--
	V _{OL}	GND	--	0.2 VDD	V	--

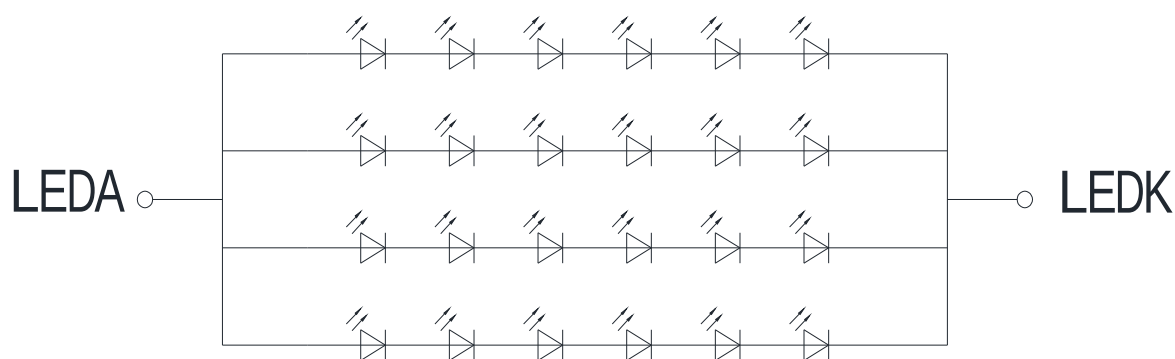
5.3 LED Backlight Characteristics

The Backlight system is edge-lighting type with 24 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I _F	--	160	--	mA	--
Forward Voltage	V _F	16.8	18.3	20.4	V	--
LCM Luminance (I _F =160mA)	L _V	800	900	--	cd/m ²	Note3
LED Lifetime	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

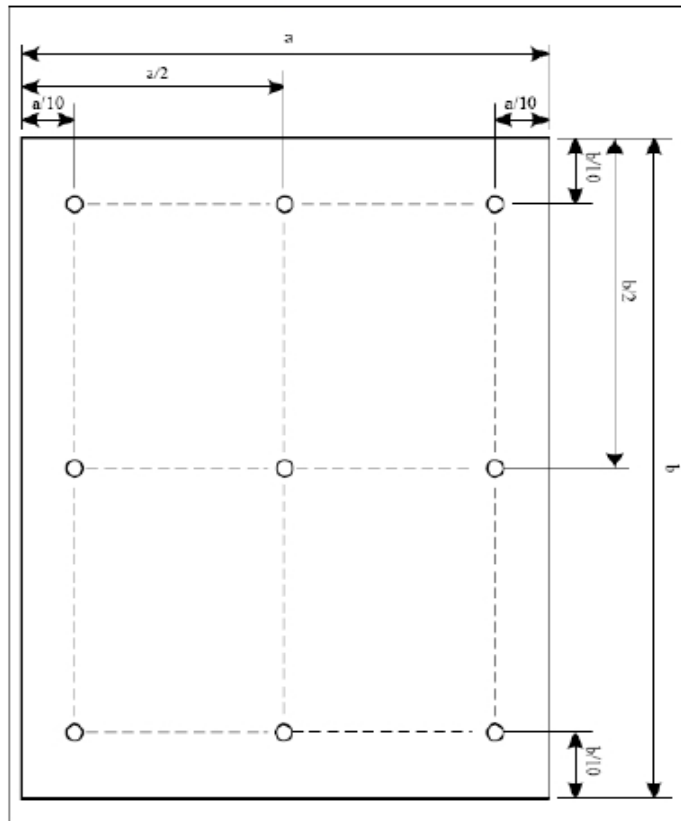
Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25°C±3°C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=160mA. The LED lifetime could be decreased if operating IL is larger than 160mA. The constant current driving method is suggested.



LED(B/L) CIRCUIT

NOTE 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

6. RGB Interface Characteristics

6.1 RGB Interface Selection

The DPI interface is operated with VS, HS, DE PCLK, DB [23:0] lines. It supports several pixel formats that can be selected by vipf [2:0] bits in "Pixel Format Set (R3Ah)". The selection of a given interface is defined by vipf [2:0] as show in the Table 7 and Figure 8 below.

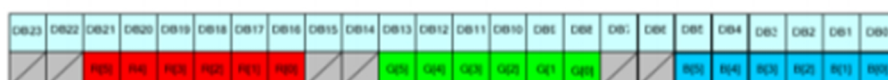
Table 7 DPI (RGB) Interface Selection

vipf [2:0]			DPI (RGB) Interface	Used Pins
1	0	1	16-bit RGB interface	VS, HS, DE, PCLK,DB [20:16] , DB [13:8],DB [4:0]
1	1	0	18-bit RGB interface	VS, HS, DE, PCLK, DB [21:16] , DB [13:8], DB [5:0]
1	1	1	24-bit RGB interface	VS, HS, DE, PCLK, DB [23:0]
Others			Setting prohibited	

16-bit DPI interface connection:set pixel format DPI[2:0]=3'h5



18-bit DPI interface connection:set pixel format DPI[2:0]=3'h6



24-bit DPI interface connection:set pixel format DPI[2:0]=3'h7



Figure 8 DPI (RGB) Interface 16/18/24-bit pixel format selection

The Pixel clock (PCLK) is running all the time without stopping, it is used for entering VS, HS, DE and DB [23:0] states when there is a rising edge of the PCLK. The PCLK can not be used as the internal clock for other functions of the display module.

Vertical synchronization (Vsync) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the PCLK signal.

Horizontal synchronization (Hsync) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the PCLK signal.

DE (Data Enable) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the PCLK signal.

DB [23:0] are used to tell what is the information of the image that is transferred on the display (When DE= '0' (low) and there is a rising edge of PCLK). DB [23:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the PCLK signal.

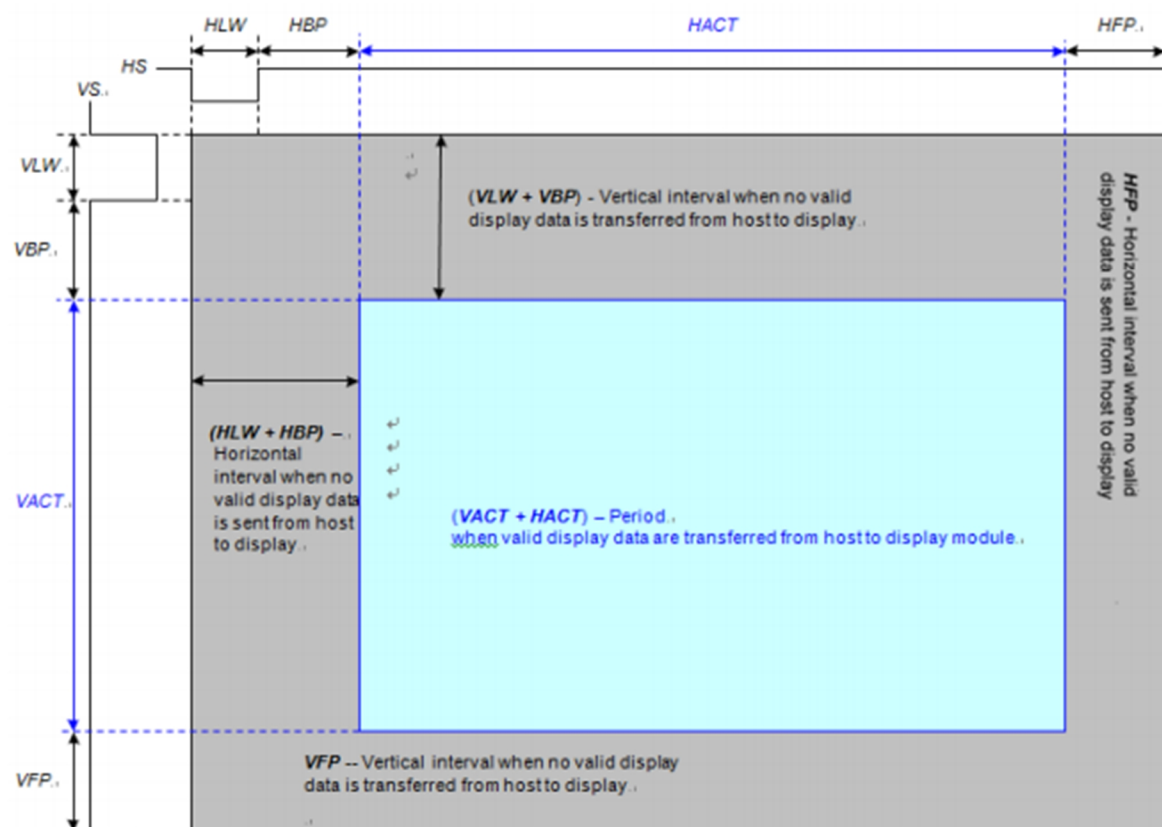
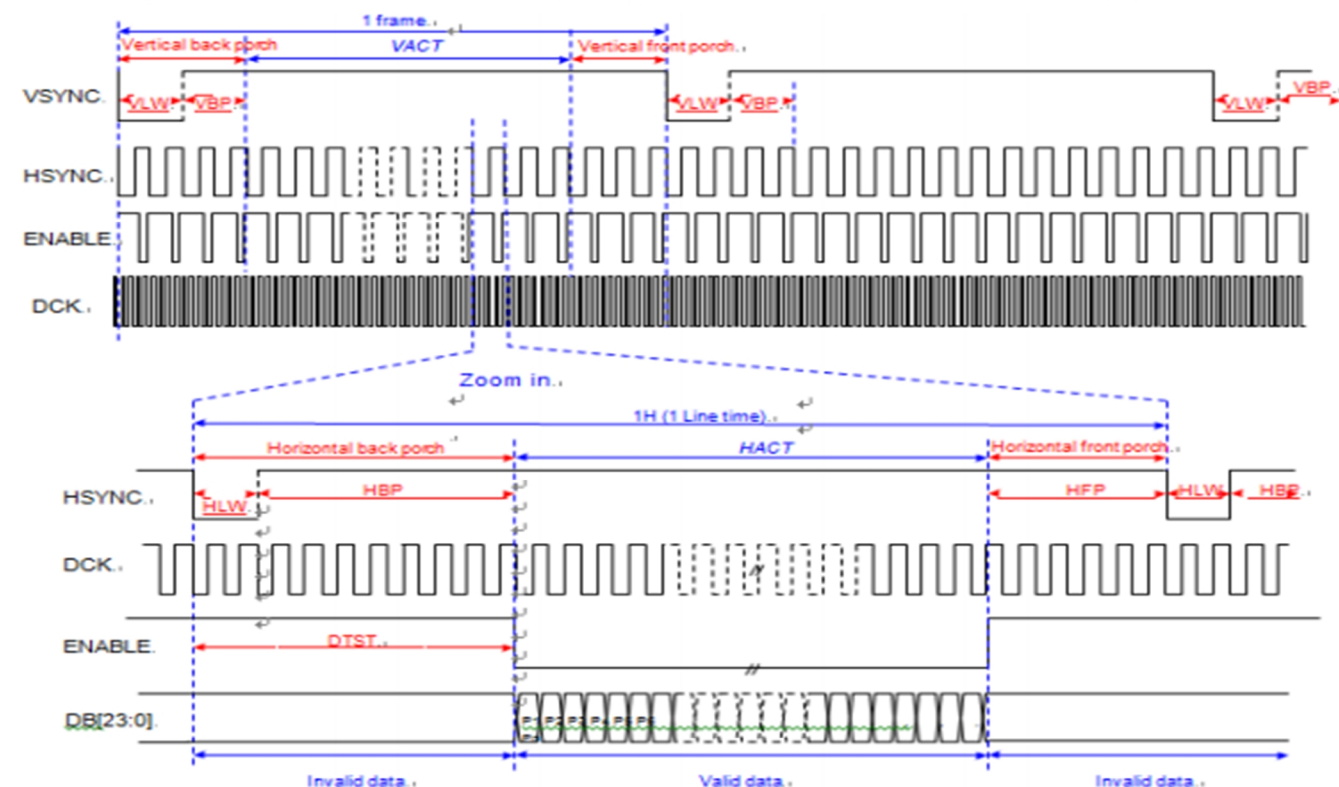


Figure 9 General DPI timing diagram

6.2 RGB Interface Timing characteristics

The timing chart of 24-/18-/16-bit DPI (RGB) interface mode is illustrated in Figure 10.



VLW : VSYNC Low pulse Width
 HLW : HSYNC Low pulse Width
 DTST : Data Transfer Startup Time
 Pn : pixel 1, pixel 2..., pixel n

Note1. $HLW+HBP+HFP \geq 1.2\mu s$.

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	FCLK	--	(40)	--	MHz
Horizontal Synchronization	hpw	--	10	--	PCLK
Horizontal Back Porch	hbp	--	30	--	PCLK
Horizontal Front Porch	hfp	--	56	--	PCLK
Horizontal Address	hdisp	--	400	--	PCLK
Vertical Synchronization	VS	--	10	--	Line
Vertical Back Porch	vbp	--	34	--	Line
Vertical Front Porch	vfp	--	20	--	Line
Vertical Address	vdisp	--	1280	--	Line
Frame rate	FR		60		Hz

Note:

1. Typical value are related to the setting frame rate is 60Hz..s

7. CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	2.66	3.47	--	1

NOTES:

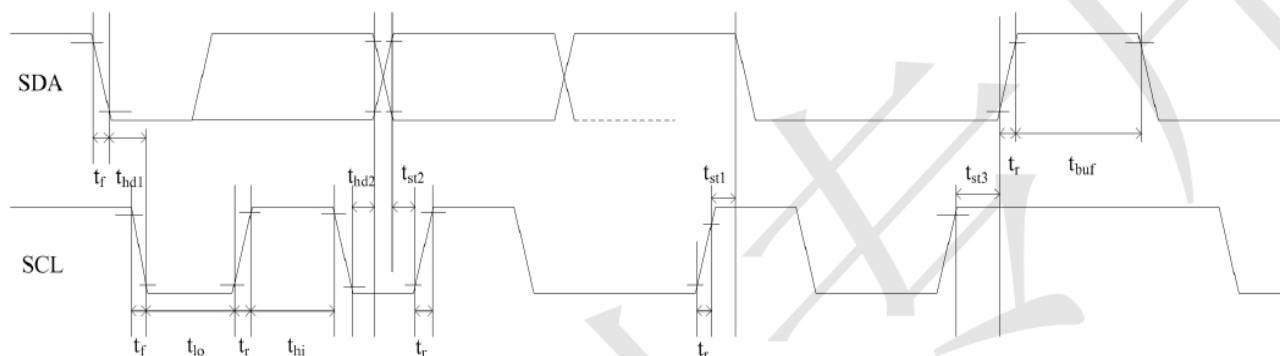
If used beyond the absolute maximum ratings, GT9271 may be permanently damaged. It is strongly recom-manded that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

7.1.2 DC Electrical Characteristics (Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.8	-	3.3	V	
Normal Operation Mode Current Consumption	I _{opr}	-	13		mA	
Green Mode Current Consumption	I _{mon}	-	4.5	-	mA	
Sleep Mode Current Consumption	I _{slp}	70	-	120	uA	
Level Input Voltage	V _{IH}	0.75V _{DD}	-	V _{DD} +0.3	V	
	V _{IL}	-0.3	-	0.25V _{DD}	V	
Level Output Voltage	V _{OH}	0.85V _{DD}	-	-	V	
	V _{OL}	-	-	0.15V _{DD}	V	

7.2 AC Electrical Characteristics

GT9271 provides a standard I2C interface for SCL and SDA to communicate with the host. GT9271 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

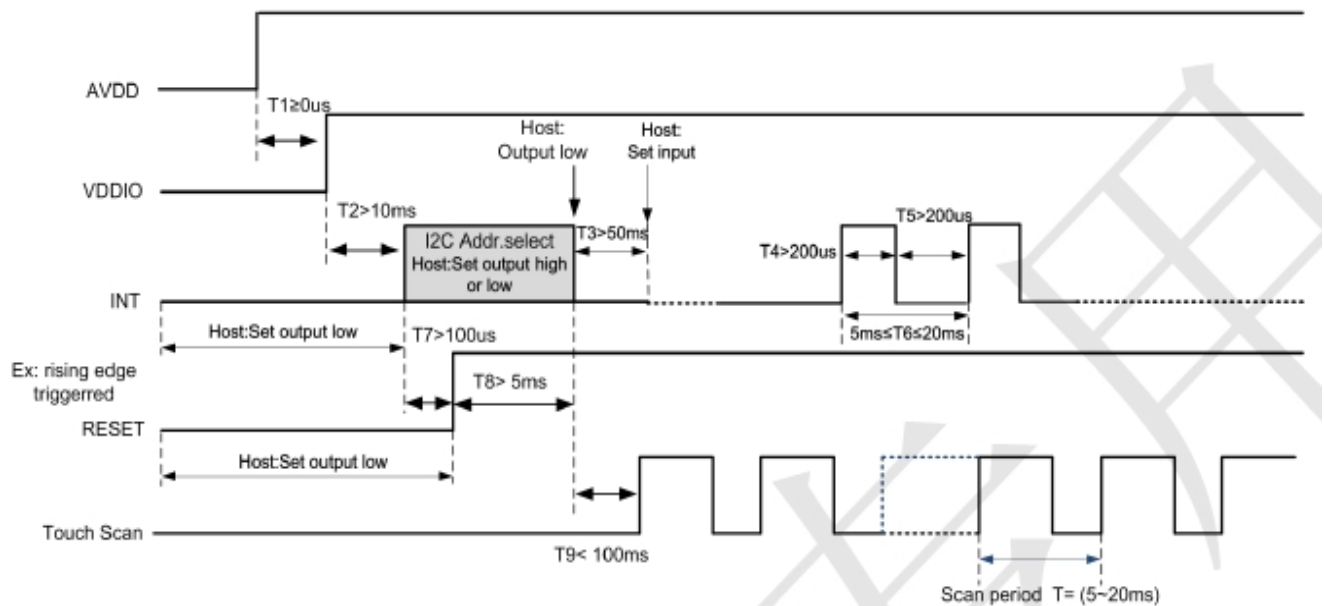
Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

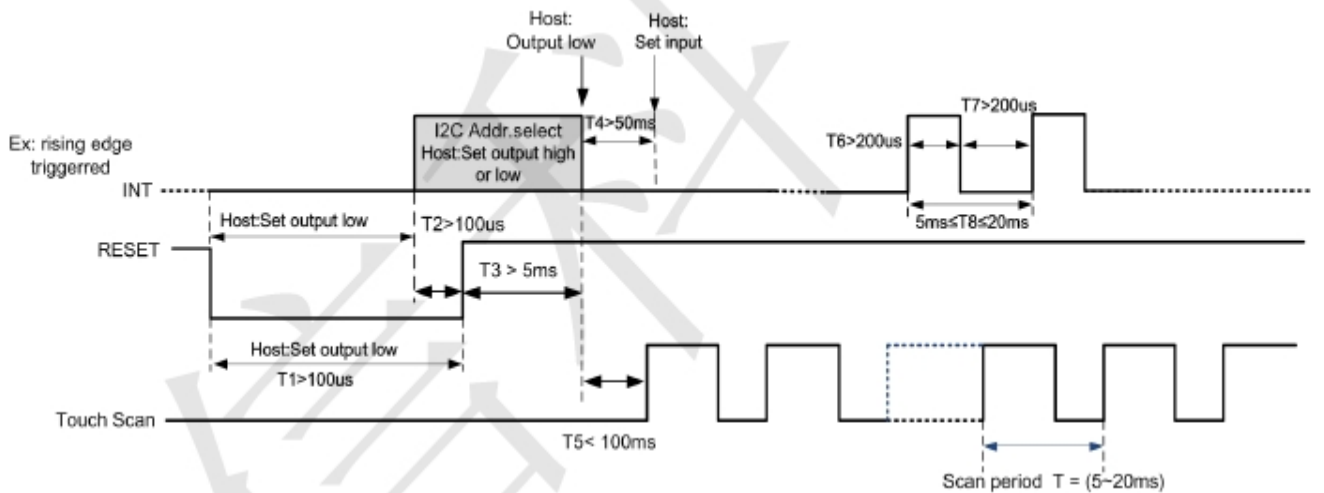
GT9271 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-

on initialization phase. See the diagram below for configuration methods and timings:

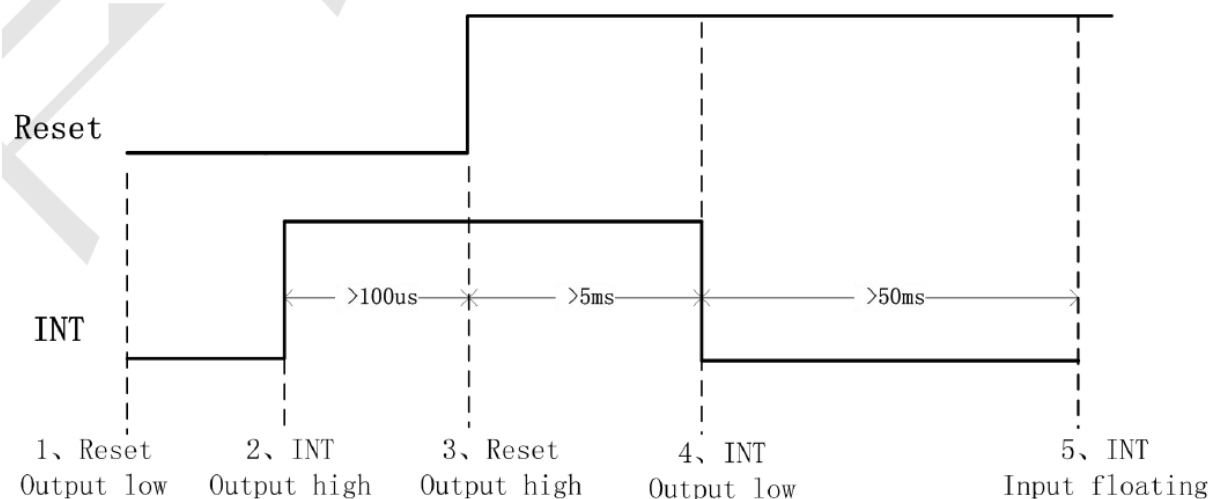
Power-On Timing:



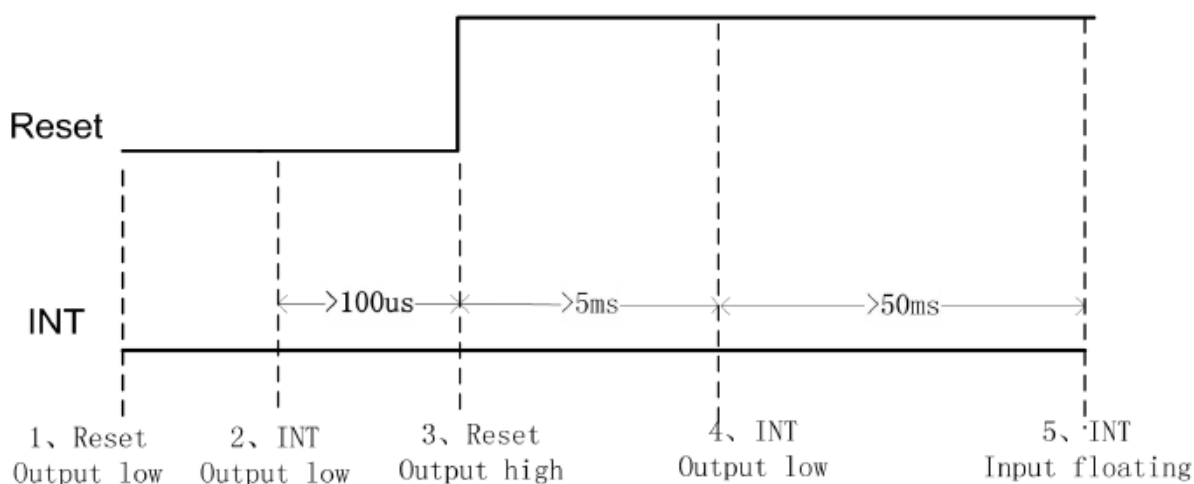
Timing for host resetting GT9271:



Timing for setting slave address to 0x28/0x29:



Timing for setting slave address to 0xBA/0xBB:



a) Data Transmission

(For example: slave address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from high to low when SCL line is high. Data flow or address is transmitted after the Start condition.

All slave devices connected to I²C bus should detect the 8-bit address issued after Start condition and send the correct ACK. After receiving matching address, GT9271 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0xBA or 0xBB, GT9271 will stay in an idle state.

DEM 4001280A VMH-PW-N(C-TOUCH) *Product Specification*

For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is high.

When communication is completed, the host will issue the Stop condition which implies the transition of SDA line from low to high when SCL line is high.

b) Writing Data to GT9271

(For example: slave address is 0xBA/0xBB)



Timing for Write Operation

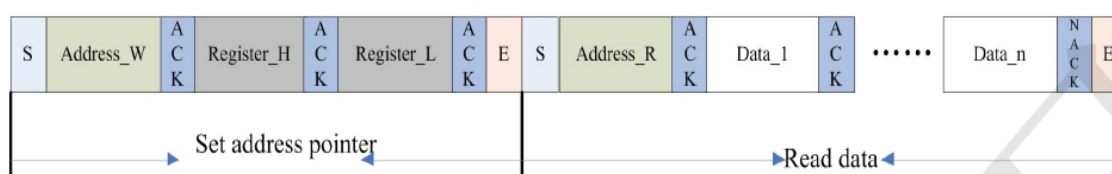
The diagram above displays the timing sequence of the host writing data onto GT9271. First, the host issues a Start condition. Then, the host sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation. Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

c) Reading Data from GT9271

(For example: slave address is 0xBA/0xBB)



Timing for Read Operation

The diagram above is the timing sequence of the host reading data from GT9271. First, the host issues a Start condition and sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0XBB (Read Operation). After receiving ACK, the host starts to read data.

GT9271 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

8. LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

8.1.1 Inspection Conditions

Inspection performed under the following conditions is recommended.

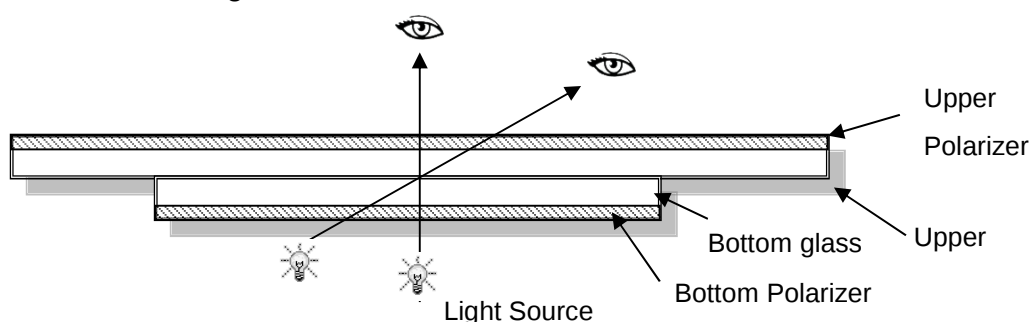
Temperature: $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$

Humidity: $65\% \pm 10\% \text{RH}$

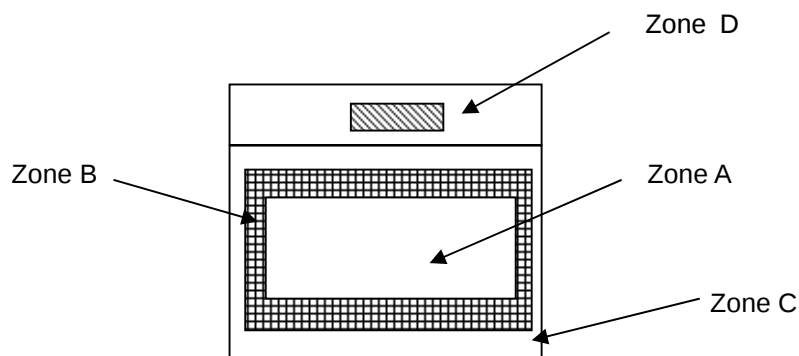
Viewing Angle: Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance: 30-50cm



8.1.2 Definition



Zone A: Effective Viewing Area (Character or Digit can be seen)

Zone B: Viewing Area except Zone A

Zone C: Outside (Zone A+Zone B) which can not be seen after assembly by customer

Zone D: IC Bonding Area

Note: As a general rule ,visual defects in Zone C can be ignored

when it doesn't effect product function or appearance after assembly by customer

8.1.3 Sampling Plan

According to GB/T 2828-2012; Normal Inspection, Class

AQL:

Major Defect	Minor Defect
0.65	1.5

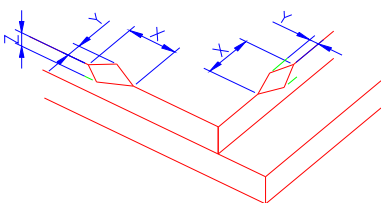
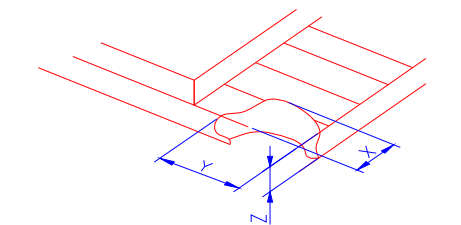
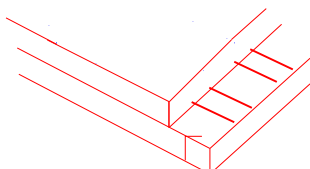
LCD: Liquid Crystal Display, LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc...	Major
2	Missing	Missing components and etc...	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed, deformation and etc...	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot, Dim spot, (Note1) Polarizer Air Bubble, Polarizer accidented spot and etc...	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc...	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying
under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying
under pure red, green, blue picture.

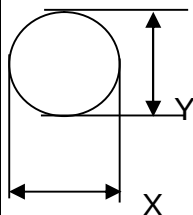
8.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of ITO, T: Height of LCD	(1) The edge of LCD broken	 <table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2)LCD corner broken	 <table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) LCD crack	 Crack Not allowed							

DEM 4001280A VMH-PW-N(C-TOUCH) Product Specification

2.0

Spot defect



$$\Phi = (X + Y) / 2$$

① light dot (black/white spot , pinhole, stain, etc.)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.15$	Ignore	Ignore	
$0.15 < \Phi \leq 0.25$	3(distance $\geq 10\text{mm}$)		
$0.25 < \Phi \leq 0.4$	2(distance $\geq 10\text{mm}$)		
$\Phi > 0.4$	0		

② Dim spot (light leakage、dent、dark spot, etc)

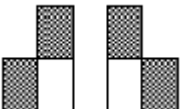
Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.15$	Ignore	Ignore	
$0.15 < \Phi \leq 0.25$	3(distance $\geq 10\text{mm}$)		
$0.25 < \Phi \leq 0.4$	2(distance $\geq 10\text{mm}$)		
$\Phi > 0.4$	0		

③ Polarizer accidented spot

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore	Ignore	
$0.2 < \Phi \leq 0.5$	2(distance $\geq 10\text{mm}$)		
$\Phi > 0.5$	0		

④Polarizer Bubble

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore	Ignore	
$0.2 < \Phi \leq 0.4$	2(distance $\geq 10\text{mm}$)		
$0.4 < \Phi \leq 0.5$	1		
$\Phi > 0.5$	0		

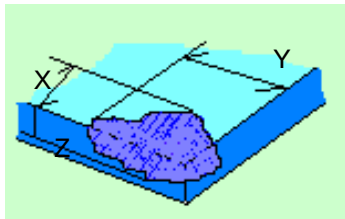
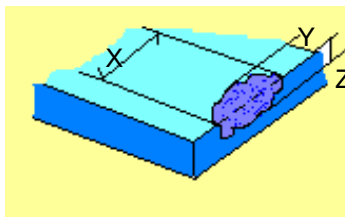
3.0	LCD Pixel defect	Pixel bad points <table border="1"> <thead> <tr> <th>Item</th><th>Zone A</th><th>Acceptable Qty</th></tr> </thead> <tbody> <tr> <td rowspan="3">Bright dot</td><td>Random</td><td>$N \leq 2$</td></tr> <tr> <td>2 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td>3 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td rowspan="3">Dark dot</td><td>Random</td><td>$N \leq 3$</td></tr> <tr> <td>2 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td>3 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td>Distance</td><td> 1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot. </td><td>5mm</td></tr> <tr> <td colspan="2">Total bright and dark dot</td><td>$N \leq 4$</td></tr> </tbody> </table> Note: A) Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern. B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture. C) 2 dot adjacent = 1 pair = 2 dots Picture:  2 dot adjacent  2 dot adjacent (vertical)  2 dot adjacent  2 dot adjacent (slant)	Item	Zone A	Acceptable Qty	Bright dot	Random	$N \leq 2$	2 dots adjacent	$N \leq 0$	3 dots adjacent	$N \leq 0$	Dark dot	Random	$N \leq 3$	2 dots adjacent	$N \leq 0$	3 dots adjacent	$N \leq 0$	Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm	Total bright and dark dot		$N \leq 4$
Item	Zone A	Acceptable Qty																							
Bright dot	Random	$N \leq 2$																							
	2 dots adjacent	$N \leq 0$																							
	3 dots adjacent	$N \leq 0$																							
Dark dot	Random	$N \leq 3$																							
	2 dots adjacent	$N \leq 0$																							
	3 dots adjacent	$N \leq 0$																							
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm																							
Total bright and dark dot		$N \leq 4$																							

DEM 4001280A VMH-PW-N(C-TOUCH) Product Specification

4.0	Line defect (LCD /Polarizer backlight black/white line, scratch, stain)  W: width, L : length N : Count	Width(mm)	Length(m m)	Acceptable Qty		
				A	B	C
		$\Phi \leq 0.05$	Ignore	Ignore		Ignore
		$0.05 < W \leq 0.06$	$L \leq 5.0$	$N \leq 3$		
		$0.06 < W \leq 0.08$	$L \leq 4.0$	$N \leq 2$		
$W > 0.08$	Define as spot defect					
5.0	Electronic Components SMT.	Not allow missing parts, solderless connection, cold solder joint, mismatch, The positive and negative polarity opposite				
6.0	Display color& Brightness.	1. Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples. 2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.				
7.0	LCD Mura/Waving/ Hot spot	Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.				

8.0	CTP Related	CTP Cover sensor accidented black/white spot	Size Φ (mm)	Acceptable Qty			
				A	B	C	
			$\Phi \leq 0.15$	Ignore		Ignore	
			$0.15 < \Phi \leq 0.25$	4 (distance $\geq 10\text{mm}$)			
			$0.25 < \Phi \leq 0.35$	3 (distance $\geq 10\text{mm}$)			
			$\Phi > 0.35$	0			
		CTP Cover scratch	Width(mm)	Ignore(mm)	Acceptable Qty		
					A	B	C
			$\Phi \leq 0.05$	Ignore	Ignore		
			$0.05 < W \leq 0.06$	$L \leq 4.0$	$N \leq 3$		
			$0.06 < W \leq 0.08$	$L \leq 3.0$	$N \leq 2$		
$0.08 < W$	Define as spot defect						

DEM 4001280A VMH-PW-N(C-TOUCH) Product Specification

		CTP Cover Pinhole/ Lack of ink <table><tr><th>Zone</th><th>Acceptable Qty</th></tr><tr><td>Size (mm)</td><td>C</td></tr><tr><td>$\Phi \leq 0.2$</td><td>Ignore</td></tr><tr><td>$0.2 < \Phi \leq 0.3$</td><td>4(distance $\geq 10\text{mm}$)</td></tr><tr><td>$0.3 < \Phi \leq 0.4$</td><td>2(distance $\geq 10\text{mm}$)</td></tr><tr><td>$\Phi > 0.4$</td><td>0</td></tr></table>	Zone	Acceptable Qty	Size (mm)	C	$\Phi \leq 0.2$	Ignore	$0.2 < \Phi \leq 0.3$	4(distance $\geq 10\text{mm}$)	$0.3 < \Phi \leq 0.4$	2(distance $\geq 10\text{mm}$)	$\Phi > 0.4$	0					
Zone	Acceptable Qty																		
Size (mm)	C																		
$\Phi \leq 0.2$	Ignore																		
$0.2 < \Phi \leq 0.3$	4(distance $\geq 10\text{mm}$)																		
$0.3 < \Phi \leq 0.4$	2(distance $\geq 10\text{mm}$)																		
$\Phi > 0.4$	0																		
	CTP Bonding bubble/ accidented spot <table><tr><th>Size $\Phi(\text{mm})$</th><th colspan="2">Acceptable Qty</th></tr><tr><td></td><td>A</td><td>B</td></tr><tr><td>$\Phi \leq 0.1$</td><td colspan="2">Ignore</td></tr><tr><td>$0.1 < \Phi \leq 0.2$</td><td colspan="2">3(distance $\geq 10\text{mm}$)</td></tr><tr><td>$0.2 < \Phi \leq 0.3$</td><td colspan="2">2(distance $\geq 10\text{mm}$)</td></tr><tr><td>$\Phi > 0.3$</td><td colspan="2">0</td></tr></table>	Size $\Phi(\text{mm})$	Acceptable Qty			A	B	$\Phi \leq 0.1$	Ignore		$0.1 < \Phi \leq 0.2$	3(distance $\geq 10\text{mm}$)		$0.2 < \Phi \leq 0.3$	2(distance $\geq 10\text{mm}$)		$\Phi > 0.3$	0	
Size $\Phi(\text{mm})$	Acceptable Qty																		
	A	B																	
$\Phi \leq 0.1$	Ignore																		
$0.1 < \Phi \leq 0.2$	3(distance $\geq 10\text{mm}$)																		
$0.2 < \Phi \leq 0.3$	2(distance $\geq 10\text{mm}$)																		
$\Phi > 0.3$	0																		
	Assembly deflection	beyond the edge of backlight $\leq 0.2\text{mm}$																	
	CTP cover broken X : length Y : width Z : height <table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>$X \leq 0.5\text{mm}$</td><td>$Y \leq 0.5\text{mm}$</td><td>$Z < \text{cover thickness}$</td></tr></table> * Circuitry broken is not allowed.	X	Y	Z	$X \leq 0.5\text{mm}$	$Y \leq 0.5\text{mm}$	$Z < \text{cover thickness}$												
X	Y	Z																	
$X \leq 0.5\text{mm}$	$Y \leq 0.5\text{mm}$	$Z < \text{cover thickness}$																	
	CTP cover broken X : length Y : width Z : height <table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>$X \leq 0.3\text{mm}$</td><td>$Y \leq 0.3\text{mm}$</td><td>$Z < \text{cover thickness}$</td></tr></table> * Circuitry broken is not allowed.	X	Y	Z	$X \leq 0.3\text{mm}$	$Y \leq 0.3\text{mm}$	$Z < \text{cover thickness}$												
X	Y	Z																	
$X \leq 0.3\text{mm}$	$Y \leq 0.3\text{mm}$	$Z < \text{cover thickness}$																	

DEM 4001280A VMH-PW-N(C-TOUCH) Product Specification

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	CTP no function	Not allowed

9. Reliability Test Result

Remark:

Item	Condition	Inspection after test
High Temperature Operating	70°C,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1. Air bubble in the LCD; 2. Non-display; 3. Missing segments/line; 4. Glass crack; 5. Current IDD is twice higher than initial value.
Low Temperature Operating	-20°C, 96HR	
High Temperature Storage	80°C, 96HR	
Low Temperature Storage	-30°C, 96HR	
High Temperature & High Humidity Operating	+70°C, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-20°C,30 min ↔ +60°C,30 min, Change time:5min 20CYC.	
ESD Test	C=150pF, R=330,5points/panel Air:±4KV, 5times; Contact:±2KV, 5 times; (Environment: 15°C~35°C, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total)	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM	

1. The test samples should be applied to only one test item.
2. Sample size for each test item is 5~10pcs.
3. For Damp Proof Test, Pure water (Resistance > 10MΩ) should be used.
4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
5. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6. The color fading mura of polarizing filter should not care.

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

- (4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

- (8) Protect the module from static; it may cause damage to the CMOS ICs.

- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

- (10) Do not disassemble the module.

- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

- (12) Pins of I/F connector shall not be touched directly with bare hands.

- (13) Do not connect, disconnect the module in the "Power ON" condition.

- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence
& 6.2 Power Off Sequence

10.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0°C to 35°C
and relative humidity of less than 70%

- (2) Do not store the TFT-LCD module in direct sunlight.

- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.