Display Elektronik GmbH

DATA SHEET

TFT MODULE

DEM 376960B VMH-PW-N

2,86" TFT

Product Specification   Version: 0

04.01.2025

Revision History

Date	Rev. No.	Page	Summary
04.01.2025	0	ALL	FIRST ISSUE

Contents

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses am orphous silicon TFT as a switching device. This model is composed of a transmissive type TFT-LCD Panel, driver circuit, backlight unit. The resolution of a 2.86" TFT-LCD

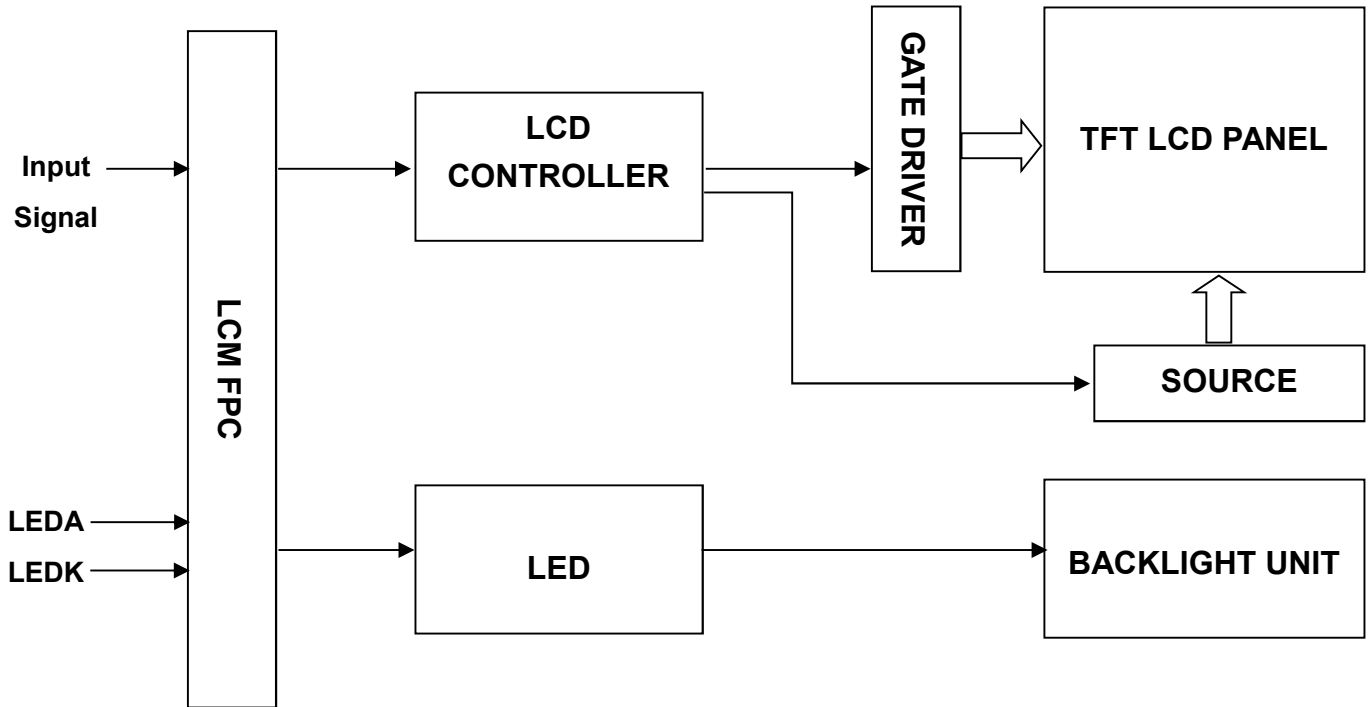contains 376xRGBx960 pixels, and can display up to 16.7 Million colors.

* Features

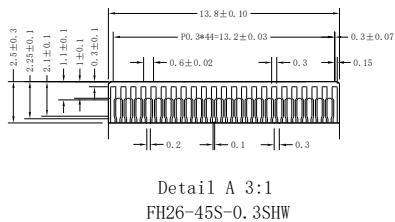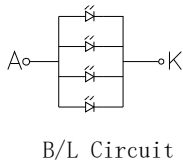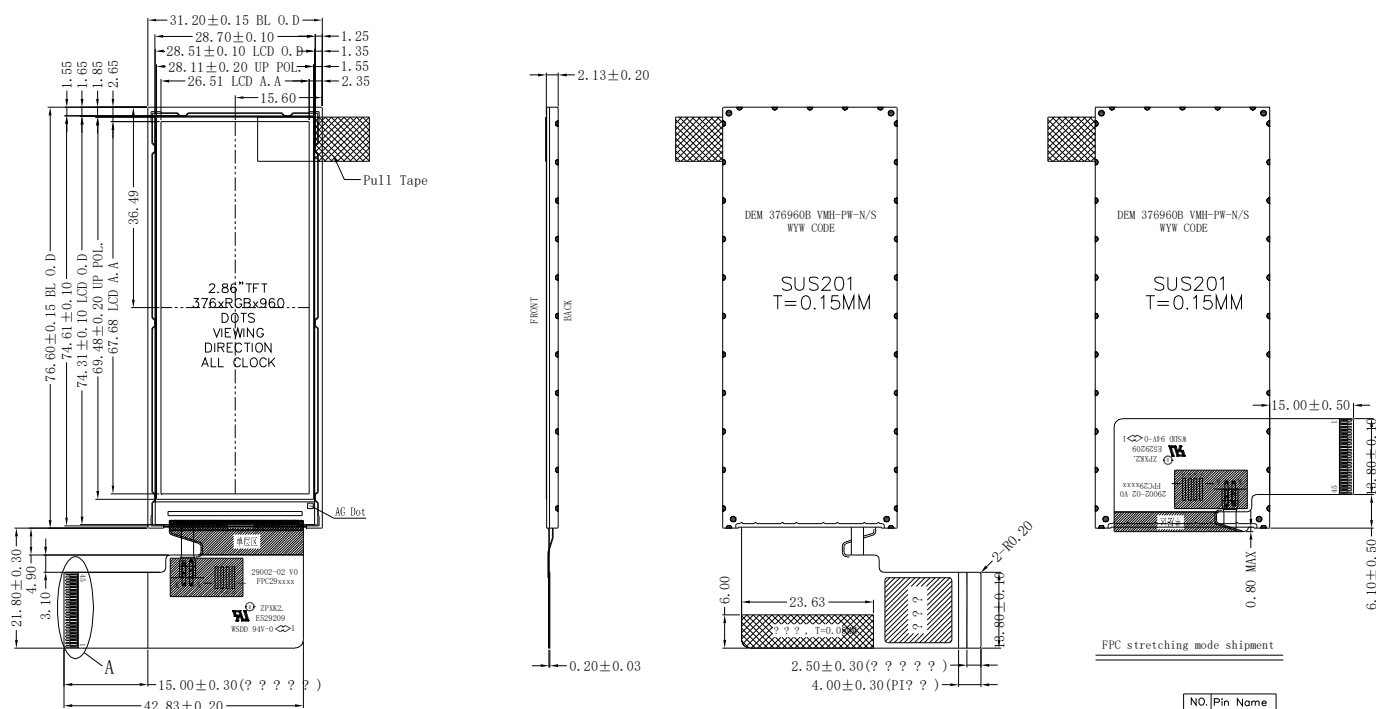| General Information Items	Specification	Unit	Note
	Main Panel		
Display Area(AA)	26.51 x 67.68 (2.86 Inch)	mm	-
Driver Element	TFT Active Matrix	-	-
Display Colors	16.7 Million	colors	-
Number of Pixels	376 x RGB x 960	dots	-
Pixel Arrangement	RGB Vertical Stripe	-	-
Pixel Pitch	0.0235 x 0.0705	mm	-
Viewing Angle	ALL	o'clock	-
Controller IC	ST7701S (Sitronix)	-	-
LCM Interface	SPI, 24/18-BIT-RGB	-	-
Display Mode	IPS, Transmissive / Normally Black	-	-
Operating Temperature	-20°C ~ +70°C	°C	-
Storage Temperature	-30°C ~ +80°C	°C	-

* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	-	31.20	-	mm	-
	Vertical(V)	-	76.60	-	mm	-
	Depth(D)	-	2.13	-	mm	-
Weight		-	10	-	g	-

1. Block Diagram

```
                    ┌──────────────┐            ┌──────┐   ┌──────────────┐
                    │     LCD      │          ┌→│ GATE │═══│TFT LCD PANEL │
  Input  ──→ ┌───┐ →│  CONTROLLER  │──────────┘ │DRIVER│   │              │
  Signal     │ L │  └──────────────┘            └──────┘   │              │
             │ C │          │                              │              │
             │ M │          └──────────────┐               └──────────────┘
             │   │                          │                      ↑
             │ F │                          └──→┌──────────────┐   ║
             │ P │                              │   SOURCE     │═══╝
             │ C │                              └──────────────┘
  LEDA ──→   │   │  →┌──────────────┐            ┌──────────────┐
  LEDK ──→   └───┘   │     LED      │──────────→ │BACKLIGHT UNIT│
                     └──────────────┘            └──────────────┘
```

2. Outline Dimension

Pull Tape

2.86"TFT
376xRGBx960
DOTS
VIEWING
DIRECTION
ALL CLOCK

AG Dot

A

B/L Circuit

Detail A 3:1
FH26-45S-0.3SHW

DEM 376960B VMH-PW-N/S
WYW CODE

SUS201
T=0.15MM

FPC stretching mode shipment

NOTE:
1. DISPLAY TYPE:2.86″,TFT-LCD,16.7M COLORS
2. DISPLAY MODE:NORMALLY BLACK/IPS
3. VIEWING DIRECTION:ALL
4. LCM DRIVER IC:ST7701S (COG)
　 LCM Interface:3SPI+16/18/24 RGB
5. VDD/VCI:3.3V(TYP.),IOVCC:1.65-3.3V
6. OPERATING TEMP: -20°C TO 70°C
　 STORAGE TEMP: -30°C TO 80°C
7. BACK LIGHT:LED WHITE, 4 LED,80mA,2.8~3.3V
8. RoHS COMPLIANT.

NO.	Pin Name
1	GND
2	VCI
3	IOVCC
4	SDO
5	SDI
6	SCL
7	CS
8	RESET
9	DB23(R7)
10	DB22(R6)
11	DB21(R5)
12	DB20(R4)
13	DB19(R3)
14	DB18(R2)
15	DB17(R1)
16	DB16(R0)
17	DB15(G7)
18	DB14(G6)
19	DB13(G5)
20	DB12(G4)
21	DB11(G3)
22	DB10(G2)
23	DB9(G1)
24	DB8(G0)
25	DB7(B7)
26	DB6(B6)
27	DB5(B5)
28	DB4(B4)
29	DB3(B3)
30	DB2(B2)
31	DB1(B1)
32	DB0(B0)
33	DE
34	PCLK
35	HSYNC
36	VSYNC
37	GND
38	XR/NC
39	YD/NC
40	XL/NC
41	YU/NC
42	NC
43	LEDA
44	NC
45	LEDK

3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VCI	Supply voltage (3.3V).	P
3	IOVCC	Supply Voltage (Logic) (1.8~3.3V).	P
4	SDO	Serial data output pin used for the SPI Interface. Leave the pin open when not in use.	O
5	SDI	SDI: Serial data input/output bidirectional pin for SPI Interface.	I/O
6	SCL	SDI: Serial data input/output bidirectional pin for SPI Interface.	I
7	CS	- A chip select signal Low: the chip is selected and accessible High: the chip is not selected and not accessible	I
8	RESET	- The external reset input - Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.	I
9-32	DB23-DB0	24-bit parallel data bus for RGB Interface. Fix to IOVCC or GND level when not in use.	I/O
33	DE	Data enable signal for RGB interface operation Low: access enabled High: access inhibited Fix to IOVCC or GND level when not in use.	I
34	PCLK	Dot clock signal for RGB interface operation	I
35	HSYNC	Line synchronizing signal for RGB interface operation	I
36	VSYNC	Frame synchronizing signal for RGB interface operation	I
37	GND	Ground.	P
38	XR/NC	Touch panel Right Glass Terminal. Leave the pin open when not in use.	A/D
39	YD/NC	Touch panel Bottom Film Terminal. Leave the pin open when not in use.	A/D
40	XL/NC	Touch panel LIFT Glass Terminal. Leave the pin open when not in use.	A/D
41	YU/NC	Touch panel Top Film Terminal. Leave the pin open when not in use.	A/D

42	NC	No connection.	-
43	LEDA	Anode pin of backlight.	P
44	NC	No connection.	-
45	LEDK	Cathode pin of backlight.	P

4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR		1000	1500	--		*(1)(2)
Response Time	Rising	T_R		--	30	35	msec	*(1)(3)
	Falling	T_F		--				
Color Gamut		S(%)		--	50.61	--	%	*
Color Filter Chromacicity	White	W_X	Θ=0 Normal Viewing Angle	-0.04	0.3252	+0.04	-	*(1)（4） CA-310 Test
		W_Y			0.3562			
	Red	R_X			0.5915			
		R_Y			0.3625			
	Green	G_X			0.3406			
		G_Y			0.5739			
	Blue	B_X			0.1504			
		B_Y			0.0959			
Viewing Angle	Hor.	$Θ_L$	CR>10	75	85	--	-	*(1)（4）
		$Θ_R$		75	85	--		
	Ver.	$Θ_U$		75	85	--		
		$Θ_D$		75	85	--		
Option View Direction			ALL					

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding: dark room

Ambient temperature: 25°C±2°C

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity

and BM-5A for other optical characteristics.

Note (1): Definition of Viewing Angle :

12' o'clock
$\Phi = 90°$

$\Phi = 180°$

$\Phi = 0°$

6' o'clock
$\Phi = 270°$
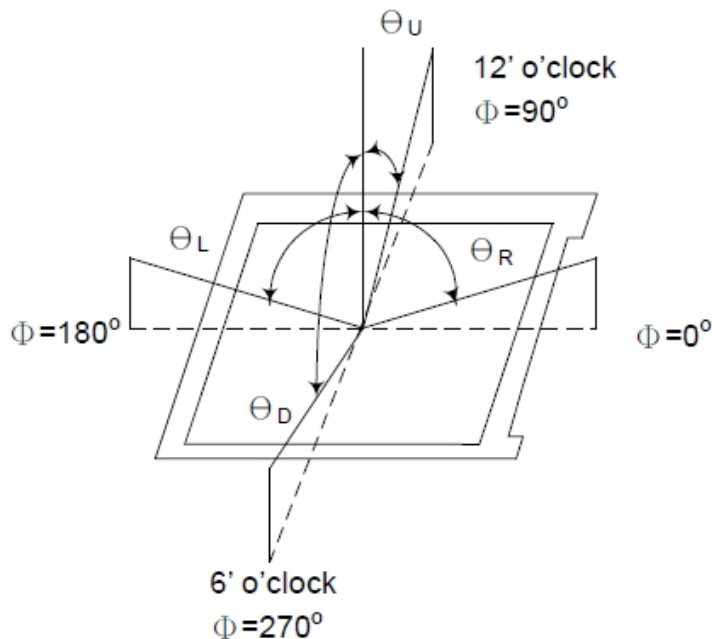
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time

Display data   Black (TFT OFF)   White (TFT ON)   Black (TFT OFF)

Optical Response

100%
90%

10%
0%

Tr   Tf
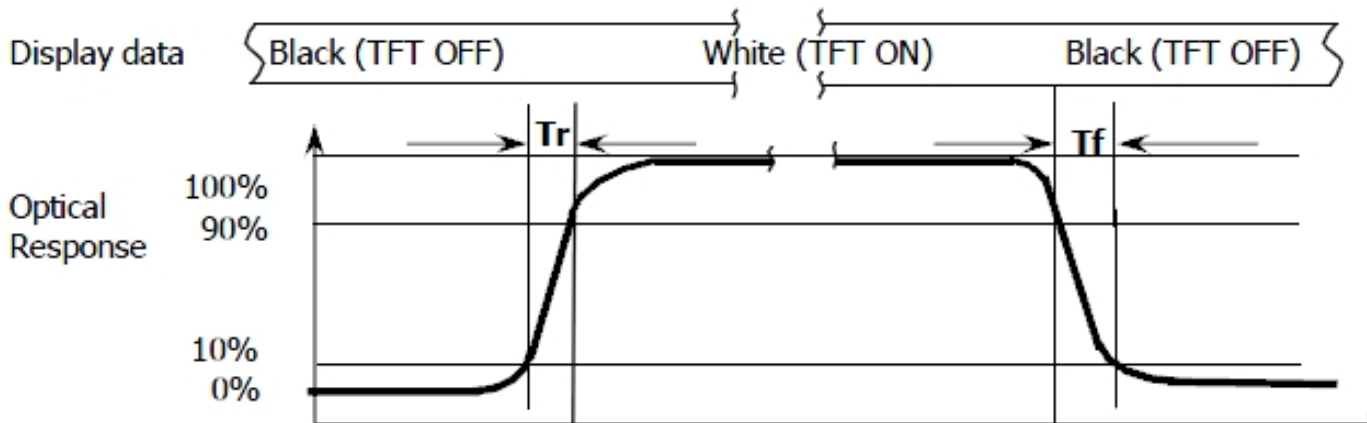
Note (4): Definition of optical measurement setup

Photo-detector (BM-5A)

50cm

Field=1°

Center of panel

LCD panel
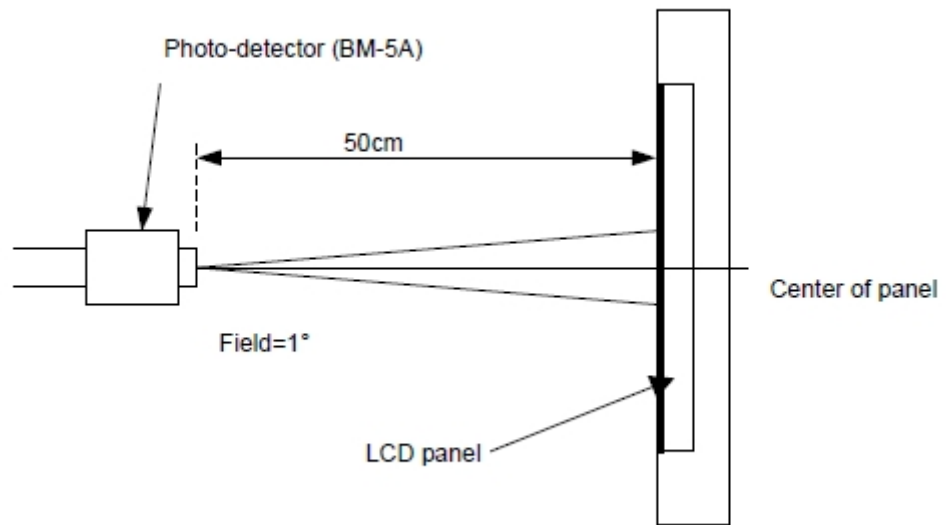
5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VCI	-0.3	4.6	V
Digital Interface Supply Voltage	IOVCC	-0.3	4.6	V
Operating Temperature	T_{OP}	-20	+70	°C
Storage Temperature	T_{ST}	-30	+80	°C

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.5	2.8	3.6	V	--
Digital interface supple Voltage	IOVCC	1.65	1.8	3.3	V	--
Normal mode Current consumption	IDD	--	30	--	mA	--
Level input voltage	V_{IH}	0.7 IOVCC	--	IOVCC	V	--
	V_{IL}	-0.3	--	0.3 IOVCC	V	--
Level output voltage	V_{OH}	0.8* IOVCC	--	IOVCC	V	--
	V_{OL}	GND	--	0.2 IOVCC	V	--

5.3 LED Backlight Characteristics

The Backlight system is edge-lighting type with 4 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	--	80	--	mA	--
Forward Voltage	V_F	--	3.2	--	V	--
LCM Luminance	L_V	500	550	--	cd/m2	Note3
LED Lifetime	Hr	50000			Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

Note (1) LED Lifetime can be defined as the time in which it continues to operate under the condition: Ta=25°C±3°C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=80mA. The LED lifetime could be decreased if operating IL is larger than 80mA.

The constant current driving method is suggested.

A ○——————○ K
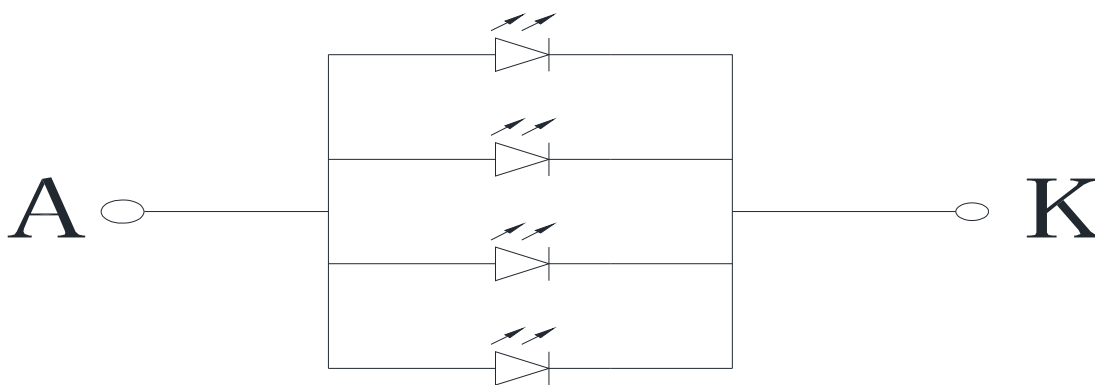
B/L Circuit

NOTE 3: Luminance Uniformity of these 9 points is defined as below:
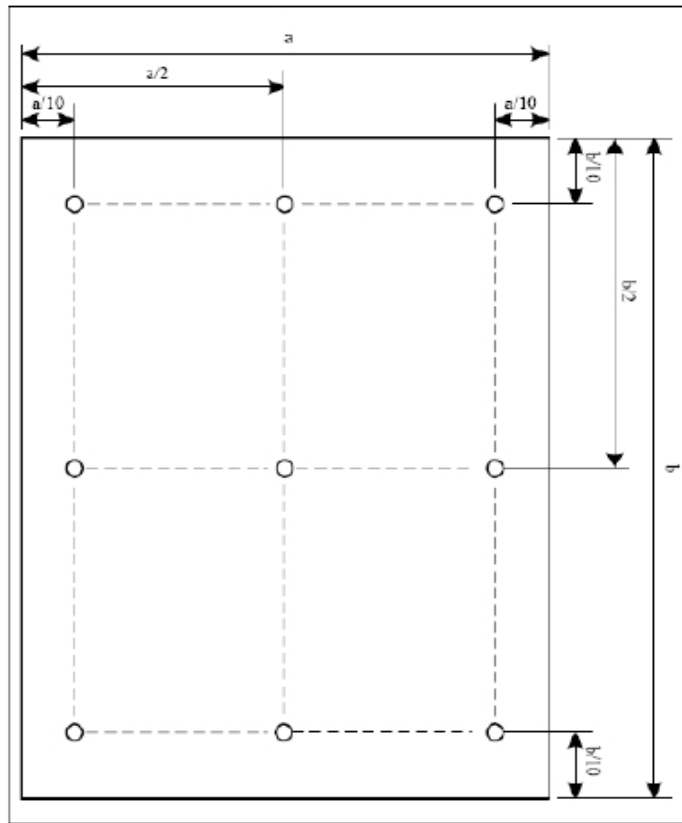
$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

6. AC Characteristics

6.1 Serial Interface Characteristics (3-Line Serial):

IOVCC=1.8V,VCI=2.8V,Ta=25°C
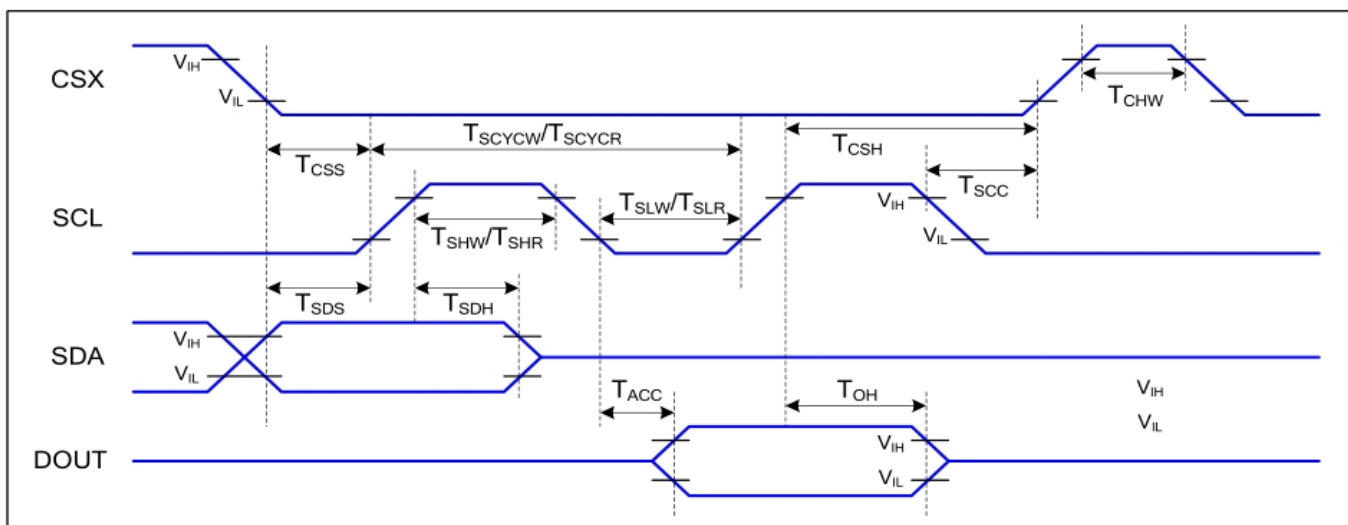
3-Line Serial Interface Timing Characteristics

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	60		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA	T_{SDS}	Data setup time	10		ns	
(DIN)	T_{SDH}	Data hold time	10		ns	

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are

specified as 30% and 70% of IOVCC for Input signals.

6.2 RGB Interface Characteristics:
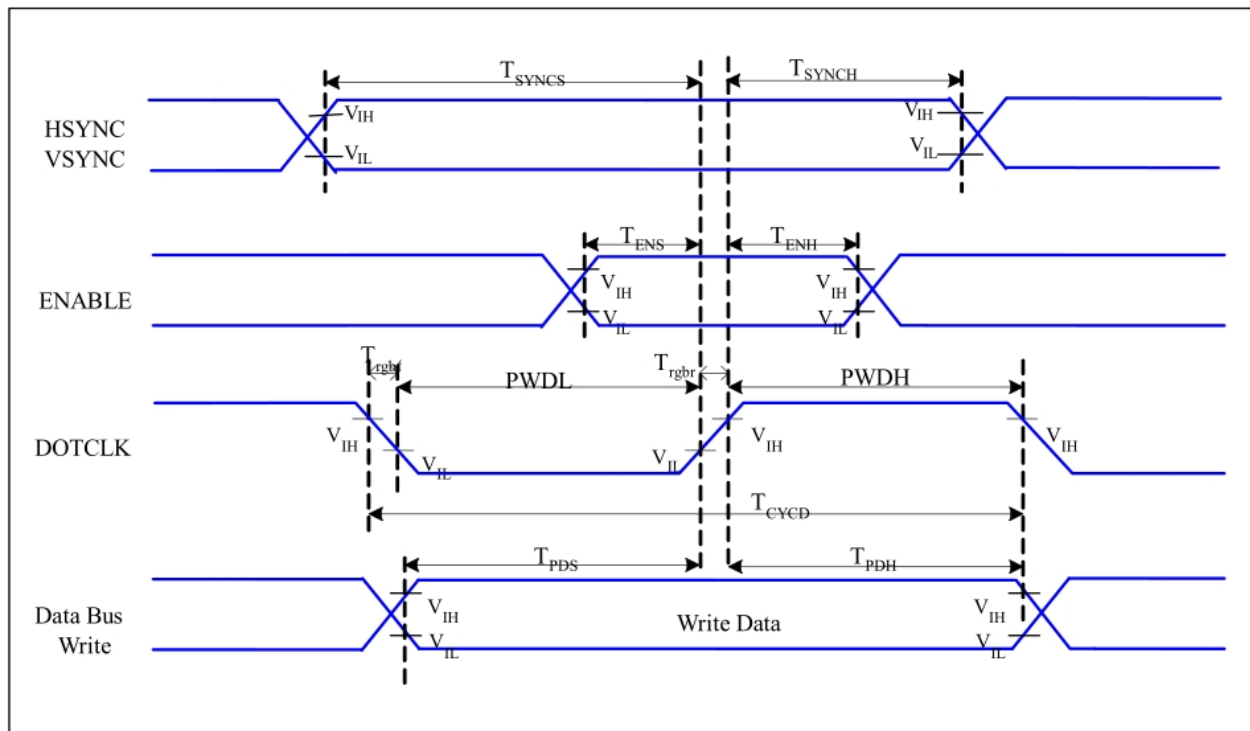
RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	5	-	ns	
	T_{ENH}	Enable Hold Time	5	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	33	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	5	-	ns	
	T_{PDH}	PD Data Hold Time	5	-	ns	

6.3 Reset Input Timing：
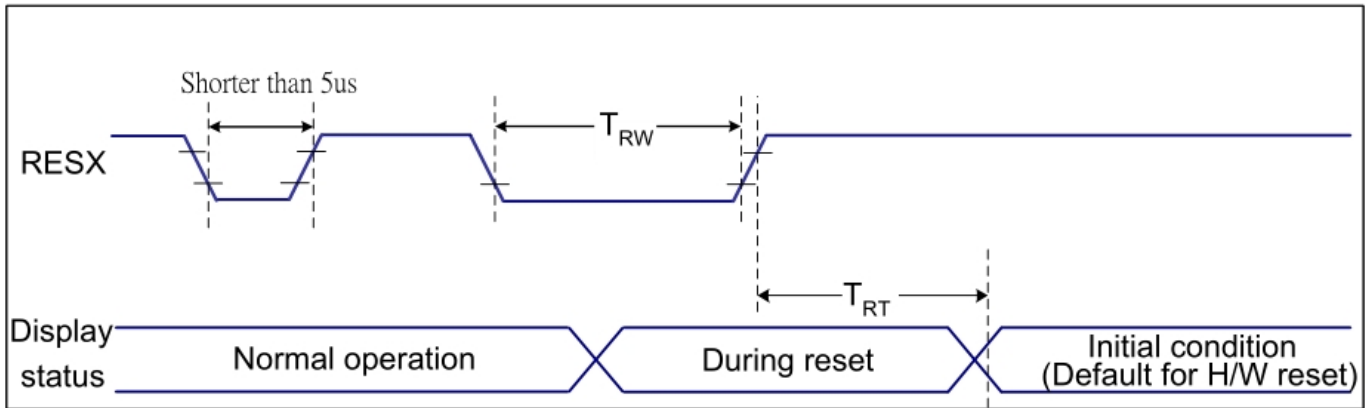
Reset Timing

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Reset Timing

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:
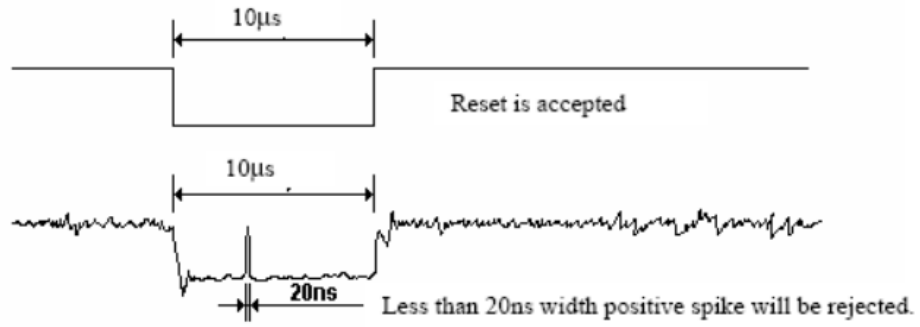
5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

6.4 RGB Interface

The ST7701 support RGB interface Mode 1 and Mode 2. The interface signals as shown in ST7701S datasheet table 6.3.1.The Mode 1 and Mode 2 function is select by setting in the Command 2, please reference application note.In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D[23:0]), when DE is high state.

The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer PCLK, VS and HS signal to ST7701.In RGB Mode 2, back porch of Vsync is defined by VBP[5:0] of RGBPRCTR command. And back porch of Hsync is defined by HBP[5:0] of RGBPRCTR command. Front porch of Vsync is defined by VFP[5:0] of RGBPRCTR command. And front porch of Hsync is defined by HFP[5:0] of RGBPRCTR command.

RGB I/F Mode	PCLK	DE	VS	HS	DB[23:0]	Register for Blanking Porch setting
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

Symbol	Name	Description
PCLK	Pixel clock	Pixel clock for capturing pixels at display interface
HS	Horizontal sync	Horizontal synchronization timing signal
VS	Vertical sync	Vertical synchronization timing signal
DE	Data enable	Data enable signal (assertion indicates valid pixels)
DB[23:0]	Pixel data	Pixel data in 16-bit,18-bit and 24-bit format

The Interface Signals of RGB Interface

6.4.1 RGB Color Format

ST7701 supports two kinds of RGB interface, DE mode (mode 1) and HV mode (mode 2), and 16bit/18bit and 24 bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, D[17:0] pins can be used;when HV mode is selected and the VSYNC, HSYNC, DOTCLK, D[17:0] pins can be used. When using RGB interface, only serial interface can be selected.

Pad name	24 bits configuration VIPF[3:0]=0111	18 bits configuration VIPF[3:0]=0110		16 bits configuration VIPF[3:0]=0101
		MDT=0	MDT=1	
DB[23]	R7	Not used	Not used	Not used
DB[22]	R6	Not used	Not used	Not used
DB[21]	R5	R5	Not used	Not used
DB[20]	R4	R4	Not used	R4
DB[19]	R3	R3	Not used	R3
DB[18]	R2	R2	Not used	R2
DB[17]	R1	R1	R5	R1
DB[16]	R0	R0	R4	R0
DB[15]	G7	Not used	R3	Not used
DB[14]	G6	Not used	R2	Not used
DB[13]	G5	G5	R1	G5
DB[12]	G4	G4	R0	G4
DB[11]	G3	G3	G5	G3
DB[10]	G2	G2	G4	G2
DB[09]	G1	G1	G3	G1
DB[08]	G0	G0	G2	G0
DB[07]	B7	Not used	G1	Not used
DB[06]	B6	Not used	G0	Not used
DB[05]	B5	B5	B5	Not used
DB[04]	B4	B4	B4	B4
DB[03]	B3	B3	B3	B3
DB[02]	B2	B2	B2	B2
DB[01]	B1	B1	B1	B1
DB[00]	B0	B0	B0	B0

The interface color mapping of RGB interface

6.4.2 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.
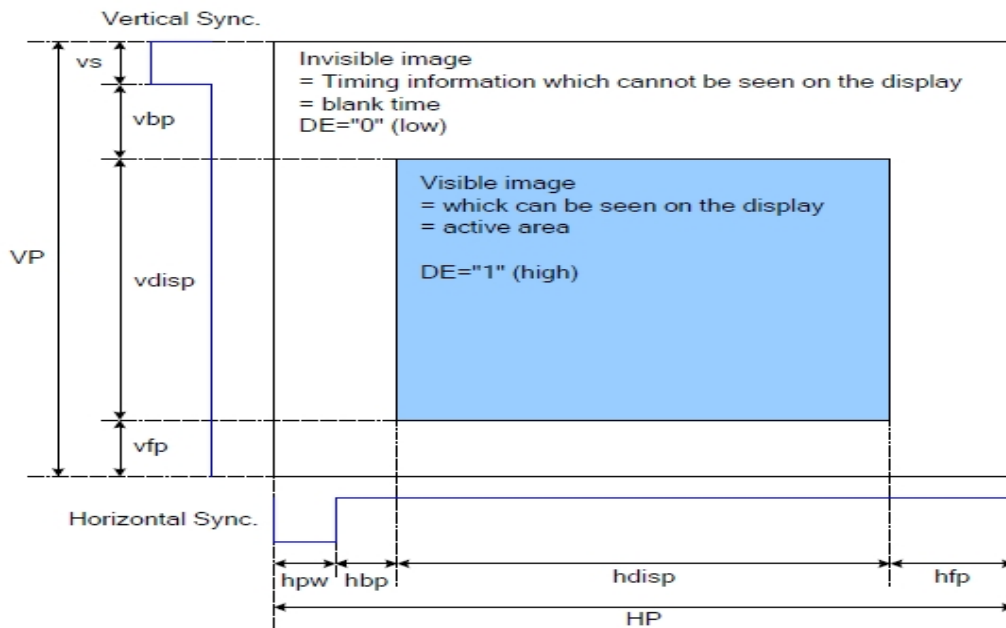
DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	FCLK	--	(30)	--	MHz
Horizontal display area	HDISP	--	376	--	Clock
Horizontal Sync. Width	hpw	1	10	--	Clock
Horizontal Sync. Back Porch	hbp	1	30	-	Clock
Horizontal Sync. Front Porch	hfp	1	56	--	Clock
Vertical display area	VDISP	--	960	--	Line
Vertical Sync. Width	vs	1	10	--	Line
Vertical Sync. Back Porch	vbp	1	30	--	Line
Vertical Sync. Front Porch	vfp	1	60	--	Line
Frame-Rate		--	60	--	Hz

Note: Typical value are related to the setting frame rate is 60Hz..

6.4.3 RGB Interface Mode Selection

ST7701 supports two kinds of RGB interface, DE mode and HV mode. The table shown below uses command C3h to select RGB interface mode.

DE/Sync	RGB Mode
0	DE mode
1	HV mode

6.4.4 RGB Interface Timing

The timing chart of RGB interface DE mode is shown as follows.
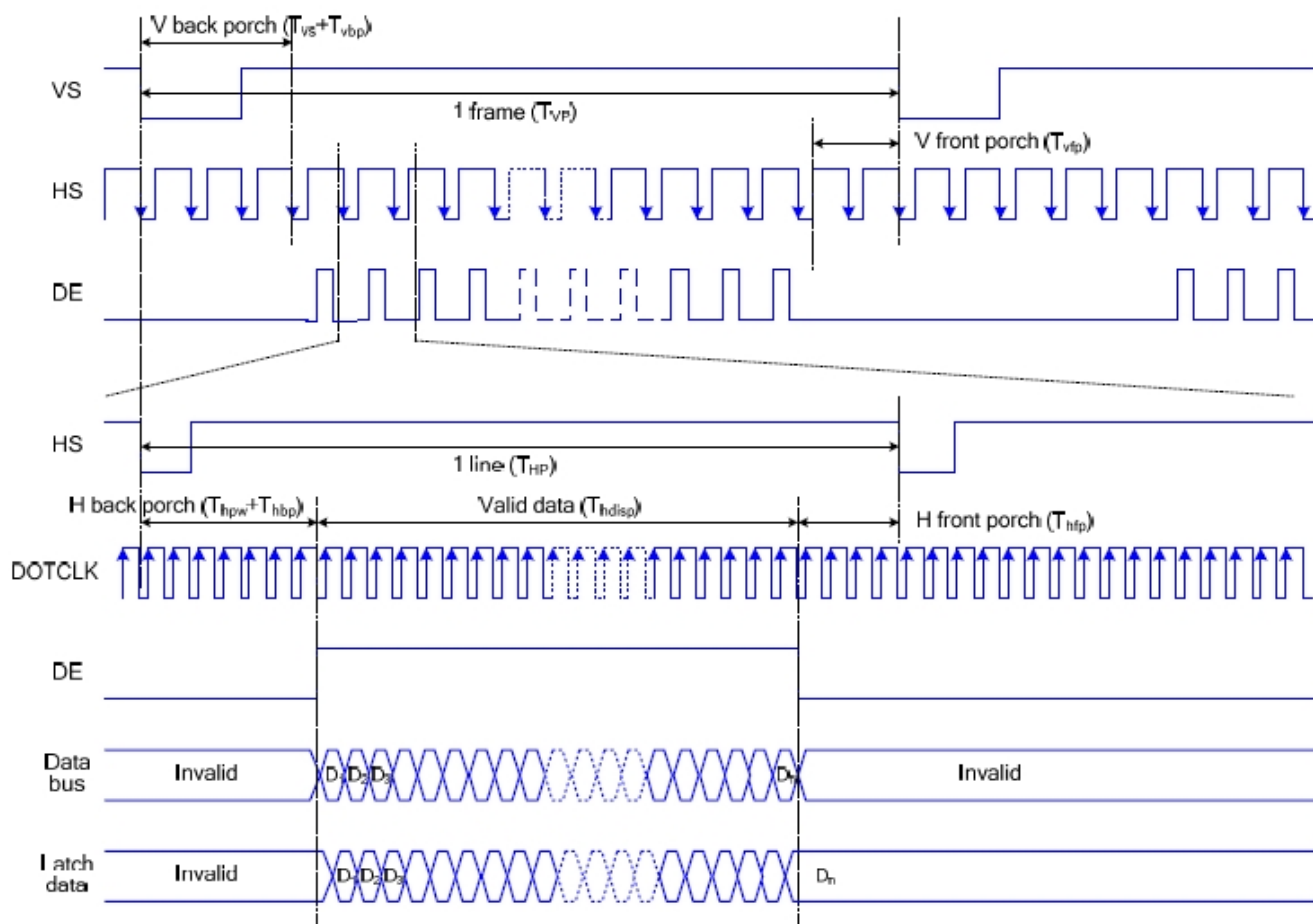
Note: The setting of front porch and back porch in host must match that in IC as this mode.

Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.
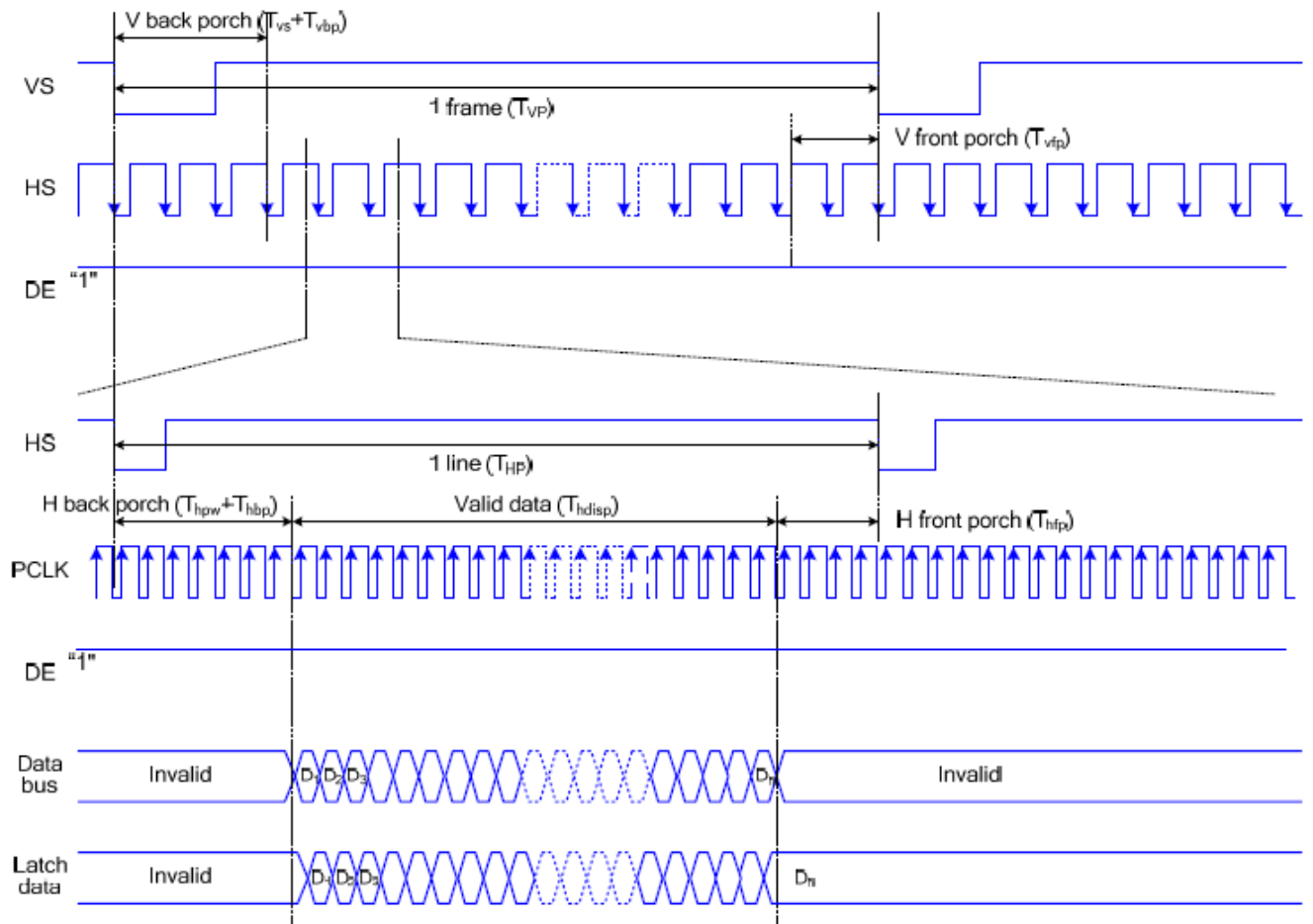
Timing Chart of RGB Interface HV Mode

7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

Temperature: 25°C±5°C

Humidity: 65%±10%RH

Viewing Angle: Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance: 30-50cm
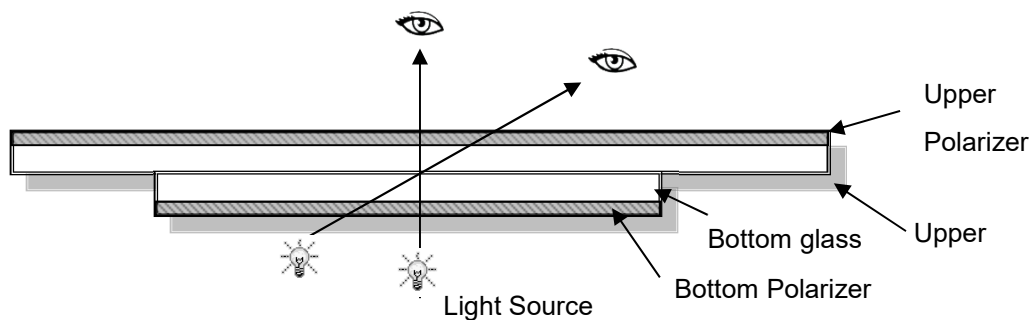
7.1.2 Definition
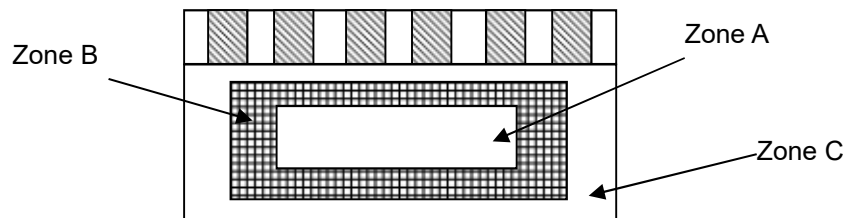
Zone A : Effective Viewing   Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note: As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

7.1.3 Sampling Plan

According to GB/T 2828-2012, normal inspection, ClassⅡ

AQL:

Major Defect	Minor Defect
0.65	1.5
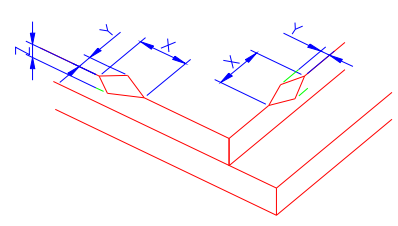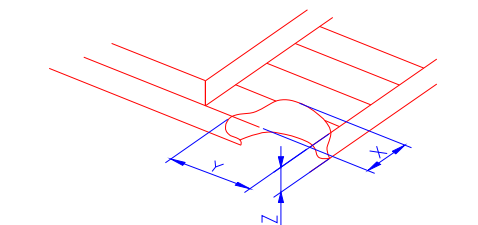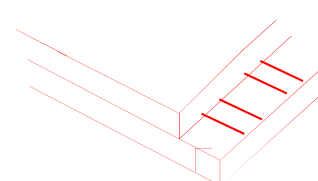
LCD: Liquid Crystal Display, LCM: Liquid Crystal Module,
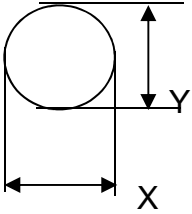
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc…	Major
2	Missing	Missing components and etc…	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed,deformation and etc…	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot,Dim spot,(Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc.	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	
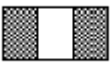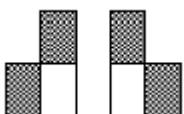
Note1:

a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black
           pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under
         pure red, green, blue picture.

7.1.4 Criteria (Visual)

Number	Items	Criteria(mm)
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of ITO, T: Height of LCD	(1) The edge of LCD broken	 | X	Y	Z
≤3.0mm	<Inner border line of the seal	≤T	
	(2)LCD corner broken	 | X	Y	Z
≤3.0mm	≤L	≤T	
	(3) LCD crack	 Crack Not allowed

Spot defect

2.0

$\Phi=(X+Y)/2$

① light dot（ black/white spot , pinhole, stain，etc.）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧6mm)		
0.25<Φ≤0.4	2(distance≧6mm)		
Φ>0.4	0		

② Dim spot（light leakage、dent、dark spot，etc）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧6mm)		
0.25<Φ≤0.4	2(distance≧6mm)		
Φ>0.4	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.5	2(distance≧6mm)		
Φ>0.5	0		

④Polarizer Bubble

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.4	3(distance≧6mm)		
Φ>0.4	0		

3.0	LCD Pixel defect	Pixel bad points

Item	Zone A		Acceptable Qty
Bright dot	Random		N≤2
	2 dots adjacent		N≤0
	3 dots adjacent		N≤0
Dark dot	Random		N≤2
	2 dots adjacent		N≤0
	3 dots adjacent		N≤0
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.		5mm
Total bright and dark dot			N≤4

Note:

A) Bright dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

C) 2 dot adjacent = 1 pair = 2 dots

Picture:

2 dot adjacent　　　　　　　　2 dot adjacent

2 dot adjacent (vertical)　　　　2 dot adjacent (slant)

4.0	Line defect (LCD /Polarizer backlight black/white line, scratch, stain) W: width, L : length N：Count					

Width(mm)	Length(mm)	Acceptable Qty		
		A	B	C
Φ≤0.03	Ignore	Ignore		
0.03<W≤0.04	L≤3.0	N≤2		Ignore
0.04<W≤0.05	L≤2.0	N≤1		
W>0.05		Define as spot defect		

5.0	Electronic Compone nts SMT.	Not allow missing parts，solderless connection，cold solder joint，mis match，The positive and negative polarity opposite
6.0	Display color& Brigh tness.	1. Color：Measuring the color coordinates, The measurement standar d according to the datasheet or samples. 2. Brightness：Measuring the brightness of White screen, The measu rement standard according to the datasheet or Samples.
7.0	LCD Mura/Waving/ Hot spot	Not visible through 5% ND filter in 50% gray or judge by limit sampl e if necessary.

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

8. Reliability Test Result

Remark:

Item	Condition	Inspection after test
High Temperature Operating	+70°C, 96h	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1. Air bubble in the LCD; 2. Non-display; 3. Missing segments/line; 4. Glass crack; 5. Current IDD is twice higher than initial value.
Low Temperature Operating	-20°C, 96h	
High Temperature Storage	+80°C, 96h	
Low Temperature Storage	-30°C, 96h	
High Temperature & High Humidity Operating	+60°C, 90% RH ,96h	
Thermal Shock (Non-operation)	-30°C, 30 min ↔ +80°C, 30 min, Change time: 5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8kV, 5times; Contact:±6kV, 5 times; (Environment: 15°C~35°C, 30%~60%).	
Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX)	

1. The test samples should be applied to only one test item.

2. Sample size for each test item is 5~10pcs.

3. For Damp Proof Test, Pure water (Resistance > 10MΩ) should be used.

4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

5. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

6. The color fading mura of polarizing filter should not care.

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0°C to 35°C

and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed.

Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.