Display Elektronik GmbH

DATA SHEET

TFT MODULE

DEM 360360A VMH-PW-N

ROUND 1,8“ TFT

Product Specification

Version: 0

17.01.2024

Revision History

Date	Rev. No.	Page	Summary
17.01.2025	0	ALL	FIRST ISSUE

Contents

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amo rphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit, backlight unit. The resolution of a 1.8" TFT-LCD contains 360xRGBx360 Pixels, and can display up to 262k colors.

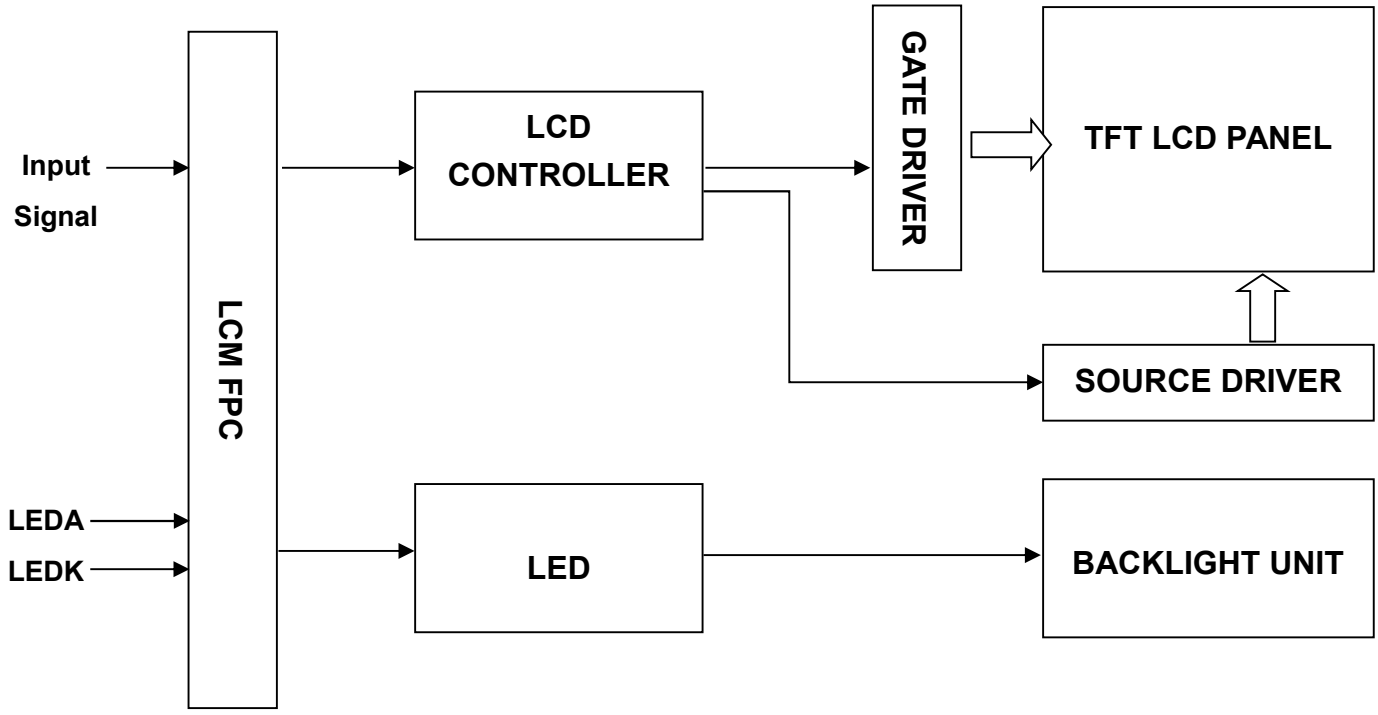
* Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display Area(AA)	45.684 x 45.684 (1.8 Inch)	mm	-
Driver Element	TFT Active Matrix	-	-
Display Colors	262k	colors	-
Number of Pixels	360 x RGB x 360	dots	-
Pixel Arrangement	RGB Vertical Stripe	-	-
Pixel Pitch	0.1269 x 0.1269	mm	-
Viewing Angle	ALL	o'clock	-
Controller IC	ST77916 (Sitronix)	-	-
LCM Interface	8-BIT-MCU, QSPI, 3/4 SPI	-	-
Display Mode	IPS, Transmissive / Normally Black	-	-
Operating Temperature	-20°C ~ +70°C	°C	-
Storage Temperature	-30°C ~ +80°C	°C	-

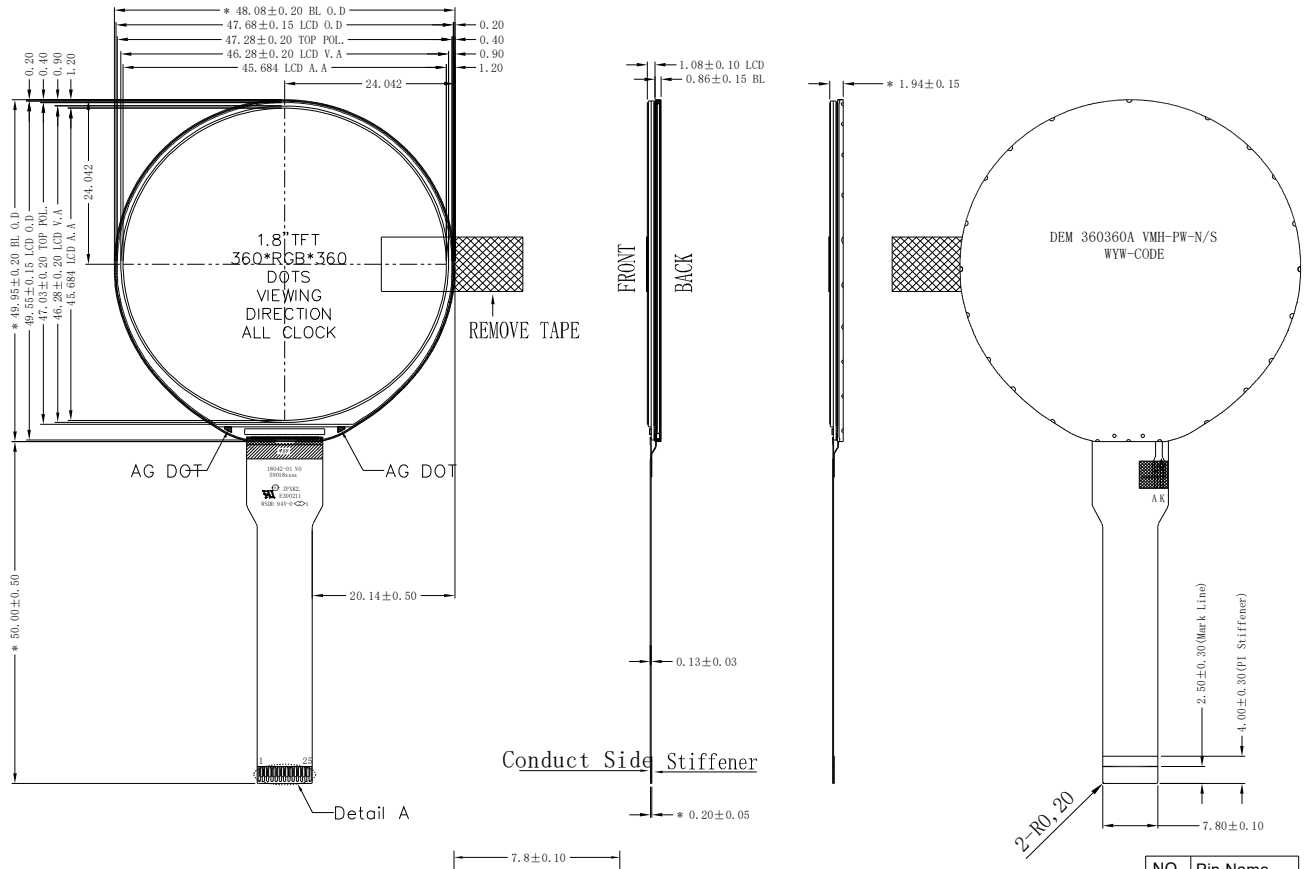
* Mechanical Information

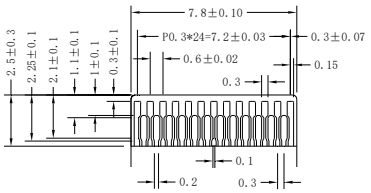
Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	-	48.08	-	mm	-
	Vertical(V)	-	49.95	-	mm	-
	Depth(D)	-	1.94	-	mm	-
Weight		-	7	-	g	-

1. Block Diagram



2. Outline Dimension





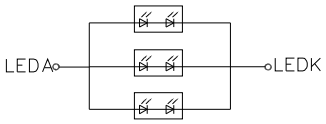
Detail A 3:1
FH26-25S-0.3SHW

NOTES:
1. DISPLAY TYPE: 1.8", TFT-LCD,262K COLORS
2. DISPLAY MODE: NORMALLY BLACK,IPS
3. VIEWING DIRECTION: ALL
4. LCM DRIVER IC: ST77916(COG)
5. LCM Interface: MCU/QSPI/SPI
6. VDD/VCI: 3.3V; LCM IOVCC:1.65~3.3V
7. OPERATING TEMP: -20°C TO 70°C
   STORAGE TEMP: -30°C TO 80°C
8. BACK LIGHT: LED WHITE, 3 DUAL CHIP LED, 60mA, 5.4~6.8V
9. RoHS and REACH COMPLIANT.

The System interface mode select.

IM2	IM1	IM0	Interface type	DB Pin in use
0	1	0	2 data lane serial I/F	D[1:0]P(SDA1? SDA2)
0	1	1	QSPI I/F	Single: DOP(SDA0) Dual: D[1:0]P(SDA0? SDA1) Quad: D[3:0]P(SDA0? SDA1? SDA2? SDA3)
0	0	0	3-line 9bit serial I/F	SDA(DOP) SCL CS
1	1	0	4-line 8bit serial I/F	SDA(DOP) SCL CSXP DCXP
1	1	1	80-8bit parallel I/F	D7P-DOP

NOTE:If not use PIN,fix to the GND ,IOVCC or NC.



BL CIRCUIT DIAGRAM

NO.	Pin Name
1	LEDK
2	NC
3	LEDA
4	NC
5	GND
6	IM0
7	IM1
8	IM2
9	RESET
10	D7P
11	D6P
12	D5P
13	D4P
14	D3P
15	D2P
16	D1P
17	D0P
18	CSXP
19	RDXP(SCL)
20	WRXP
21	DCXP
22	GND
23	IOVCC
24	VDD
25	GND

Note: The opening of top case must less than LCD POL 0.3mm at least,the LCD V.A is the Recommended opening of Lens.

3. Input terminal Pin Assignment

<table>
<tr><th>NO</th><th>SYMBOL</th><th>DISCRIPTION</th><th>I/O</th></tr>
<tr><td>1</td><td>LEDK</td><td>Cathode pin of backlight</td><td>P</td></tr>
<tr><td>2</td><td>NC</td><td>--</td><td>--</td></tr>
<tr><td>3</td><td>LEDA</td><td>Anode pin of backlight</td><td>P</td></tr>
<tr><td>4</td><td>NC</td><td>--</td><td>--</td></tr>
<tr><td>5</td><td>GND</td><td>Ground.</td><td>P</td></tr>
<tr><td>6</td><td>IM0</td><td rowspan="3">The System interface mode select.
<table><tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface type</th><th>DB Pin in use</th></tr><tr><td>0</td><td>1</td><td>0</td><td>2 data lane serial I/F</td><td>D[1:0]P(SDA1、SDA2)</td></tr><tr><td>0</td><td>1</td><td>1</td><td>QSPI I/F</td><td>Single: D0P(SDA0)
Dual: D[1:0]P(SDA0、SDA1)
Quad: D[3:0]P(SDA0、SDA1、SDA2、SDA3)</td></tr><tr><td>0</td><td>0</td><td>0</td><td>3-line 9bit serial I/F</td><td>SDA(D0P) SCL CS</td></tr><tr><td>1</td><td>1</td><td>0</td><td>4-line 8bit serial I/F</td><td>SDA(D0P) SCL CSXP DCXP</td></tr><tr><td>1</td><td>1</td><td>1</td><td>80-8bit parallel I/F</td><td>D7P-D0P</td></tr></table>NOTE:If not use PIN,fix to the GND ,IOVCC or NC.</td><td>I</td></tr>
<tr><td>7</td><td>IM1</td><td>I</td></tr>
<tr><td>8</td><td>IM2</td><td>I</td></tr>
<tr><td>9</td><td>RESET</td><td>This signal will reset the device and must be applied to properly initialize the chip.</td><td>I</td></tr>
<tr><td>10-17</td><td>D[7:0]P</td><td>-D[1:0]P are used as MCU parallel interface data bus.
8-bit parallel I/F: D[7:0]P are used.
-D[7:0]P are used as SPI interface data bus.
8-bit serial I/F: D0P is used. (SDA)
9-bit serial I/F: D0P is used. (SDA)
2 data lane serial I/F: D[1:0]P are used. (SDA1、SDA2)
-D[7:0]P are used as QSPI interface data bus.
Single: D0P is used. (SDA0)
Dual: D[1:0]P are used. (SDA0、SDA1)
Quad: D[3:0]P are used. (SDA0、SDA1、SDA2、SDA3)
-If not used, please fix this pin at IOVCC or GND.</td><td>I/O</td></tr>
<tr><td>18</td><td>CSXP</td><td>Chip select pin.
Low enable.
High disable.</td><td>I</td></tr>
<tr><td>19</td><td>RDXP(SCL)</td><td>-Read enable in MCU parallel interface.
- Clock in SPI interface. (SCL)
-If not used, please fix this pin at IOVCC or GND.</td><td>I</td></tr>
</table>

20	WRXP	Write enable in MCU parallel interface. -If not used, please fix this pin at IOVCC or GND.	I
21	DCXP	-Display data/command selection pin in parallel interface. -Display data/command selection pin in 4-line serial interface. (A0) DCX='1': display data or parameter. DCX='0': command data. -If not used, please fix this pin at IOVCC or GND	I
22	GND	Ground.	P
23	IOVCC	Supply voltage (1.65-3.3V).	P
24	VDD	Supply voltage (3.3V).	P
25	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Optical Specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal Viewing Angle	600	800	--		(1)(2)
Response Time	Rising	$T_{R+}T_F$		--	25	35	msec	
	Falling							(1)(3)
Color Gamut		S(%)		60	64.4	--	%	
Color Filter Chromaticity	White	W_X		-0.02	0.266	+0.02		(1)(4) CA-310
		W_Y			0.286			
	Red	R_X		-0.04	0.636	+0.04		
		R_Y			0.350			
	Green	G_X			0.308			
		G_Y			0.580			
	Blue	B_X			0.145			
		B_Y			0.073			
Viewing Angle	Hor.	ΘL	CR>10	80	85	--		(1)(4)
		ΘR		80	85	--		
	Ver.	ΘU		80	85	--		
		ΘD		80	85	--		
Option View Direction		ALL						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding: dark room

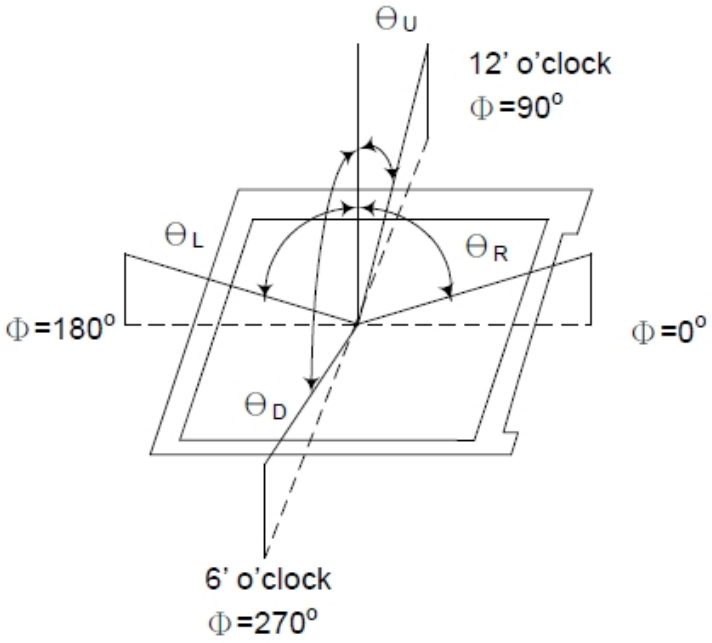
Ambient temperature: 25°C±2°C

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

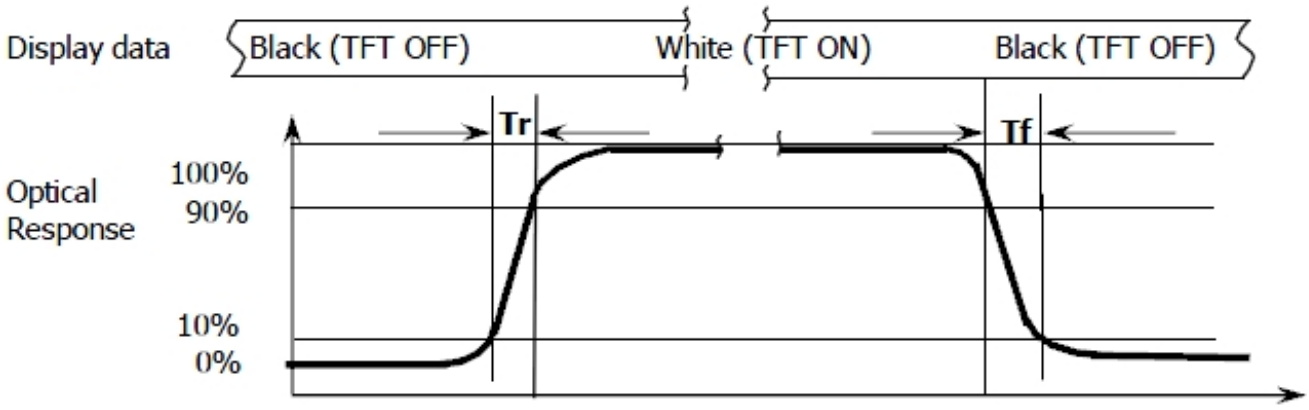
Note (1): Definition of Viewing Angle:



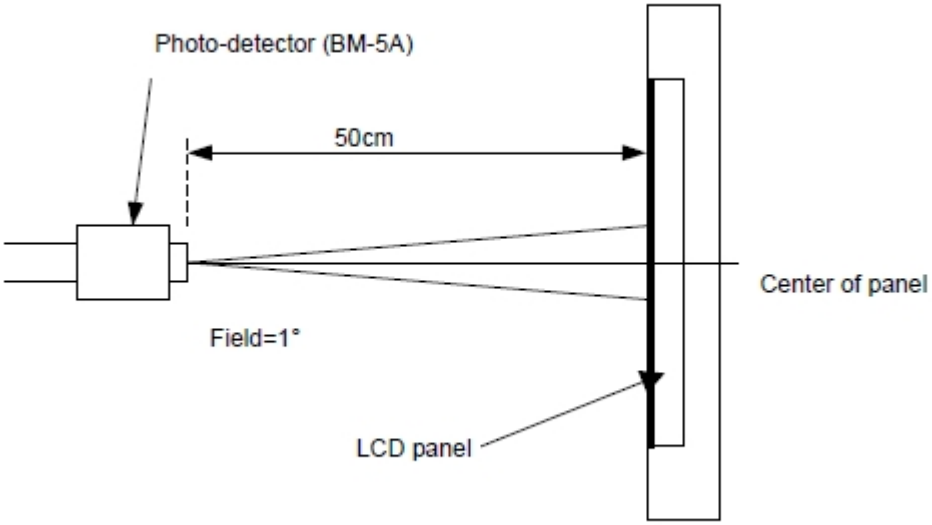
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



5. Electrical Characteristics

5.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	+4.6	V
Digital Interface Supply Voltage	IOVCC	-0.3	+4.6	V
Operating Temperature	T_{OP}	-20	+70	°C
Storage Temperature	T_{ST}	-30	+80	°C

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.65	2.8	3.3	V	-
Digital Interface Supply Voltage	IOVCC	1.65	1.8	3.3	V	-
Normal Mode Current consumption	IDD	--	11	22	mA	-
Level Input Voltage	V_{IH}	0.7*IOVCC	-	IOVCC	V	-
	V_{IL}	GND	-	0.3*IOVCC	V	-
Level Output Voltage	V_{OH}	0.8*IOVCC	-	IOVCC	V	-
	V_{OL}	GND	-	0.2*IOVCC	V	-

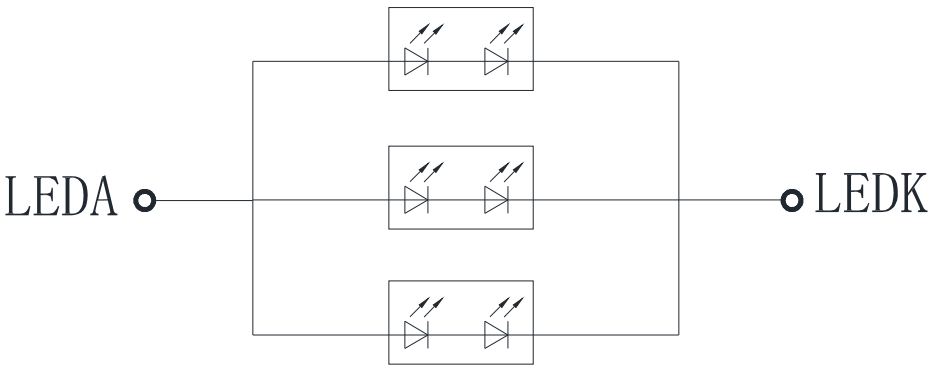
5.3 LED Backlight Characteristics

The backlight system is edge-lighting type with 3 DUAL chips LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	--	60	--	mA	-
Forward Voltage	V_F	5.4	--	6.8	V	-
LCM Luminance	LV	700	800	--	cd/m2	Note3
LED Lifetime	Hr	50000	--	--	Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

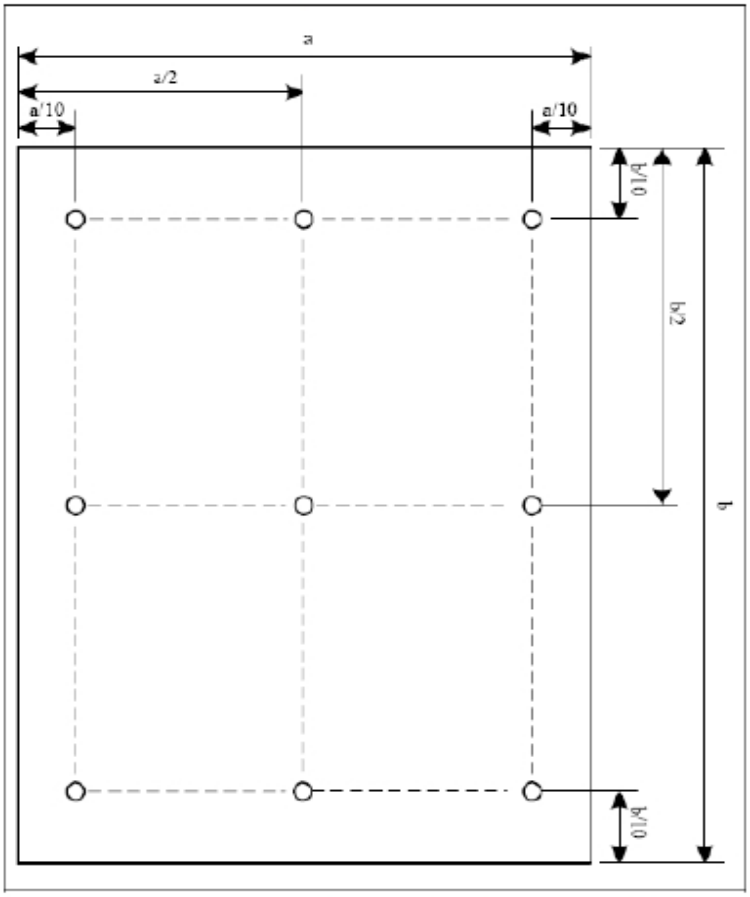
Note1: LED Lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25°C±3°C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=60mA. The LED lifetime could be decreased if operating IL is larger than 60mA.
The constant current driving method is suggested.



BL CIRCUIT DIAGRAM

Note (3) Luminance Uniformity of these 9 points is defined as below:

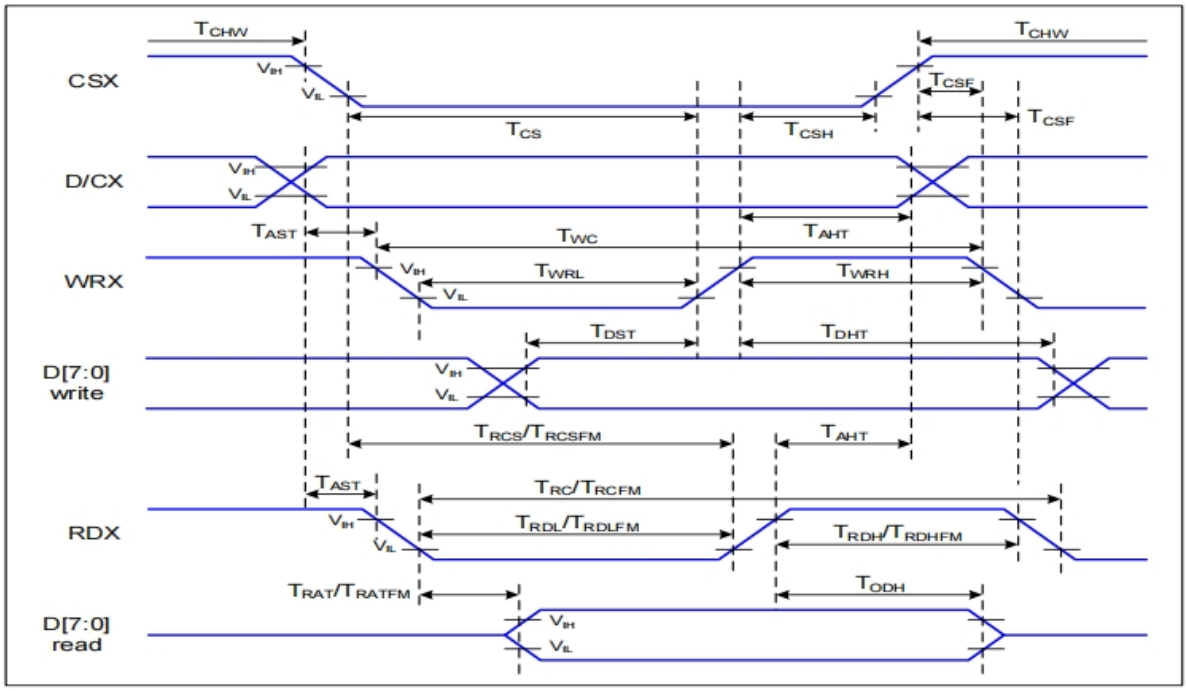


$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

6. AC Characteristic

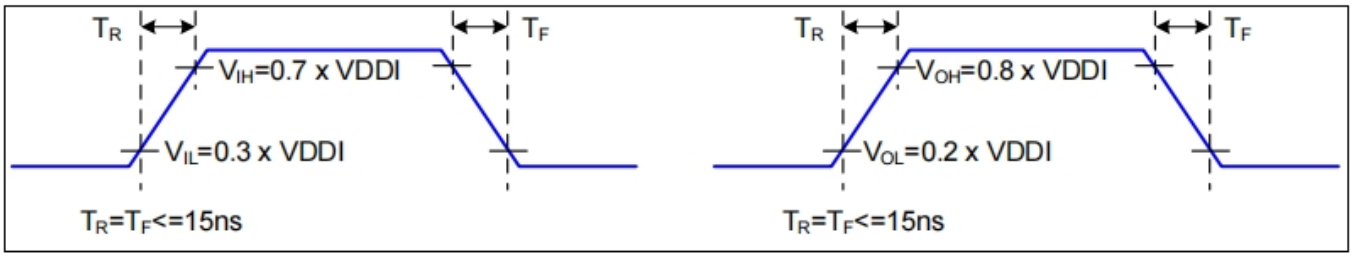
6.1 8080 Series MCU Parallel Interface Characteristics: 8-bit Bus



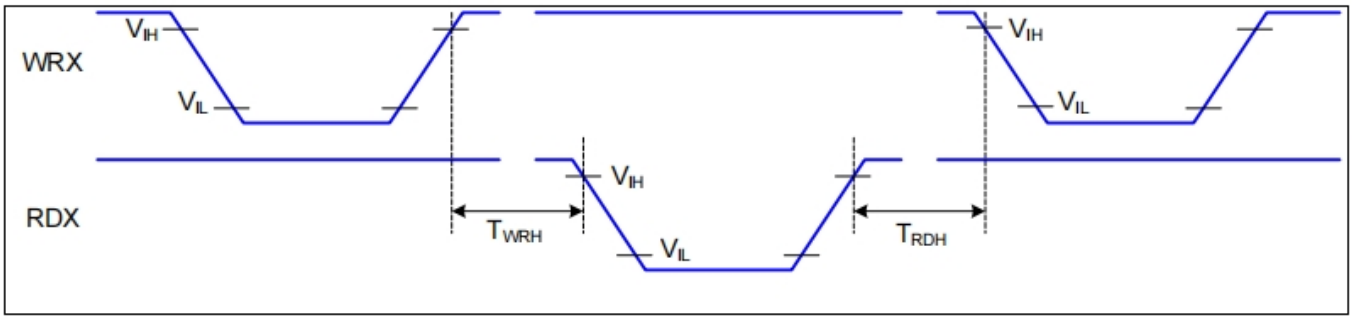
VDDI=1.65 to 3.3V, VDD=2.65 to 3.3V, GND=RGND=0V, Ta=25℃

Signal	Symbol	Parameter		Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time		0		ns	-
	T_{AHT}	Address hold time (Write/Read)		10		ns	
CSX	T_{CHW}	Chip select "H" pulse width		0		ns	-
	T_{CS}	Chip select setup time (Write)		15		ns	
	T_{RCS}	Chip select setup time (Read ID)		45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)		355		ns	
	T_{CSF}	Chip select wait time (Write/Read)		10		ns	
	T_{CSH}	Chip select hold time		10		ns	
WRX	T_{WC}	Write cycle		30		ns	
	T_{WRH}	Control pulse "H" duration		14		ns	
	T_{WRL}	Control pulse "L" duration		14		ns	
RDX (ID)	T_{RC}	Read cycle (ID)		160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)		90		ns	
	T_{RDL}	Control pulse "L" duration (ID)		45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)		450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)		90		ns	

	T_{RDLFM}	Control pulse "L" duration (FM)		355		ns	
D[7:0]	T_{DST}	Data setup time		10		ns	For CL=30pF
	T_{DHT}	Data hold time		10		ns	
	T_{RAT}	Read access time (ID)			40	ns	
	T_{RATFM}	Read access time (FM)			340	ns	
	T_{ODH}	Output disable time		20	80	ns	



Rising and Falling Timing for I/O Signal

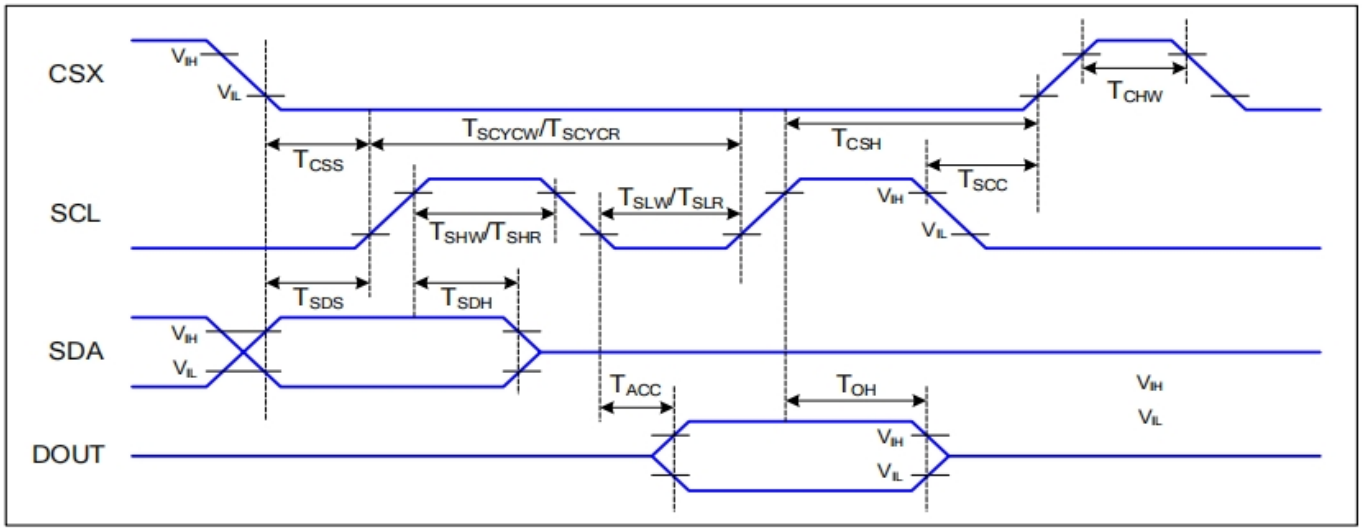


Write-to-Read and Read-to-Write Timing

Note:

The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI/IOVCC for Input signals.

6.2 Serial Interface Characteristics (3-Line Serial):

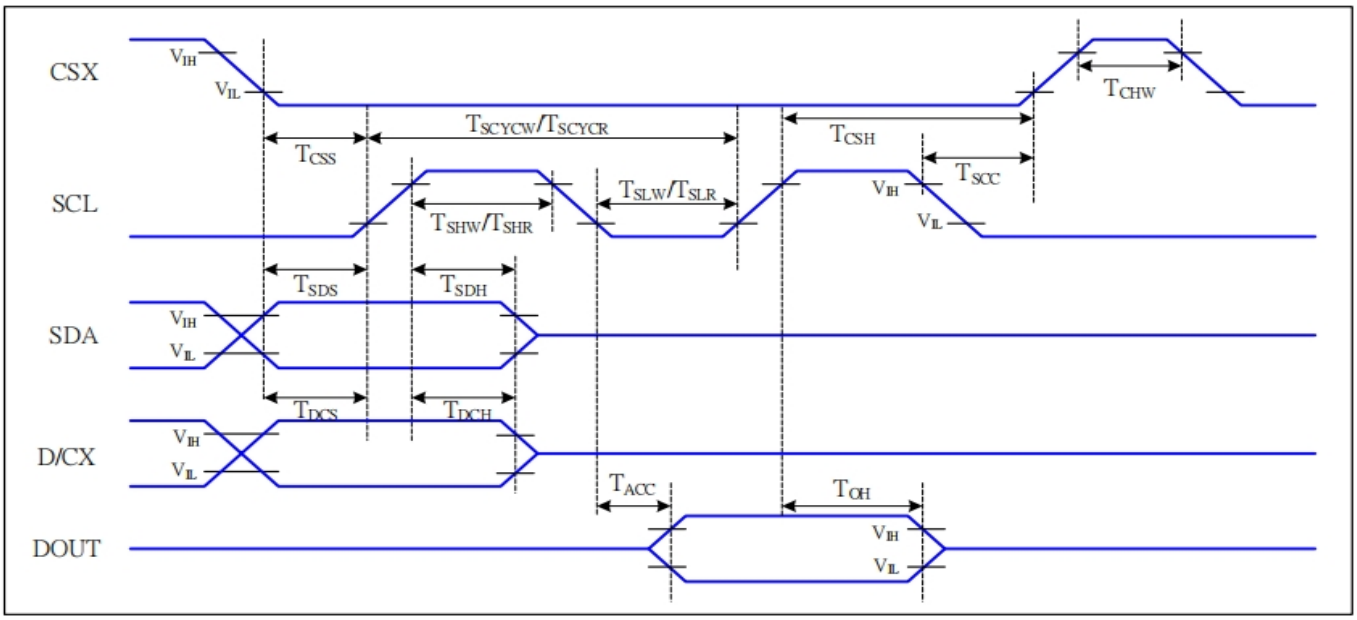


VDDI=1.65 to 3.3V, VDD=2.65 to 3.3V, GND=RGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	
	T_{SHW}	SCL "H" pulse width (Write)	7		ns	
	T_{SLW}	SCL "L" pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI/IOVCC for Input signals.

6.3 Serial Interface Characteristics (4-Line Serial):

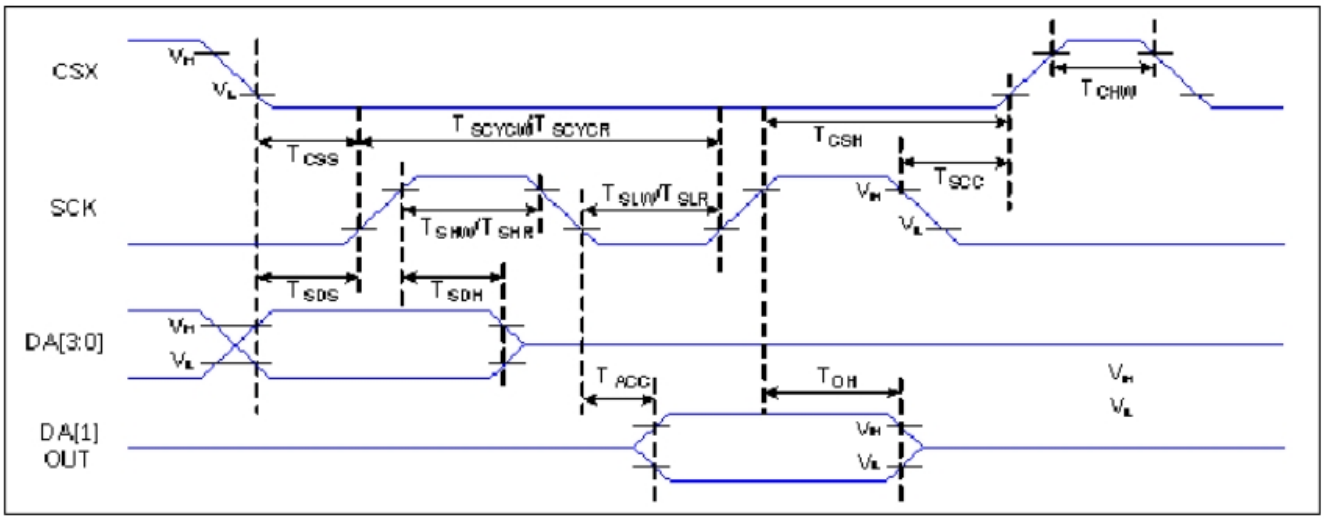


VDDI=1.65 to 3.3V, VDD=2.65 to 3.3V, GND=RGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	7		ns	
	T_{SLW}	SCL "L" pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	7		ns	
	T_{DCH}	D/CX hold time	7		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI/IOVCC for Input signals.

6.4 QSPI Interface Characteristics:

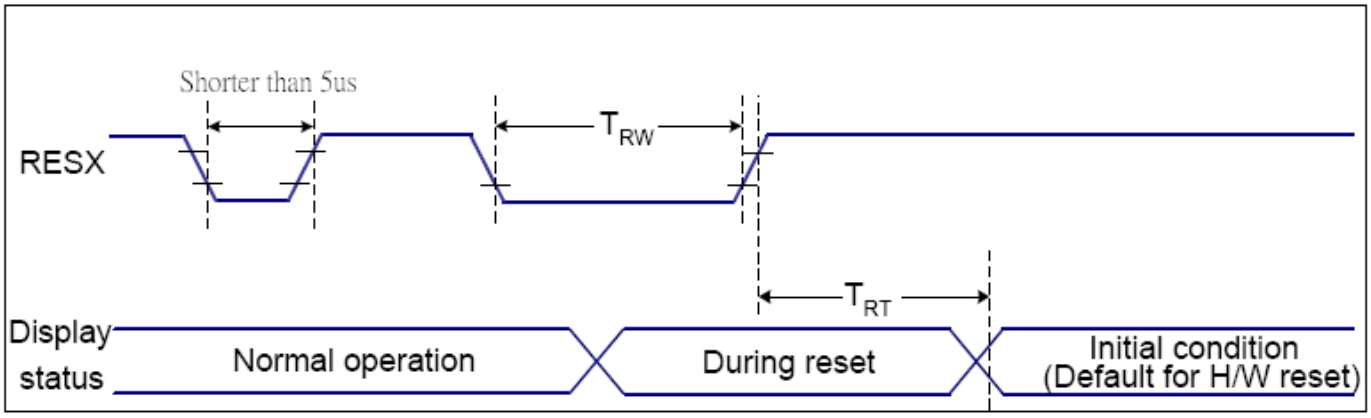


VDDI=1.65 to 3.3V, VDD=2.65 to 3.3V, GND=RGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
			200		ns	*Note1*
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	
	T_{SHW}	SCL "H" pulse width (Write)	7		ns	
	T_{SLW}	SCL "L" pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI/IOVCC for Input signals.

6.5 Reset Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

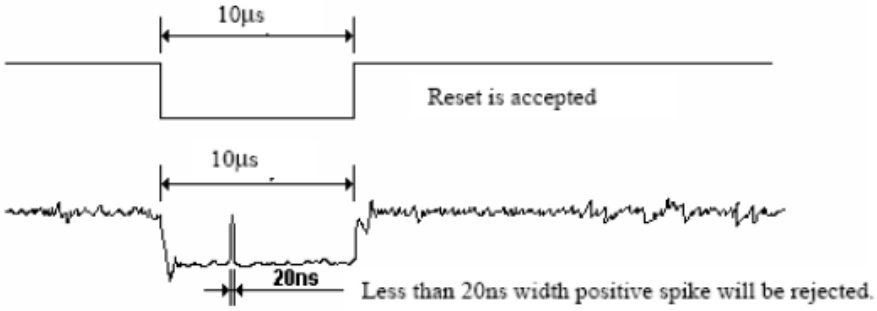
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection Conditions

Inspection performed under the following conditions is recommended.

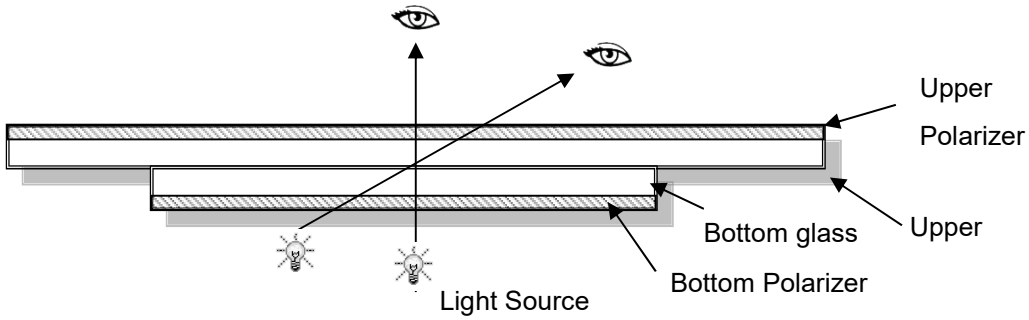
Temperature: 25°C±5°C

Humidity: 65%±10%RH

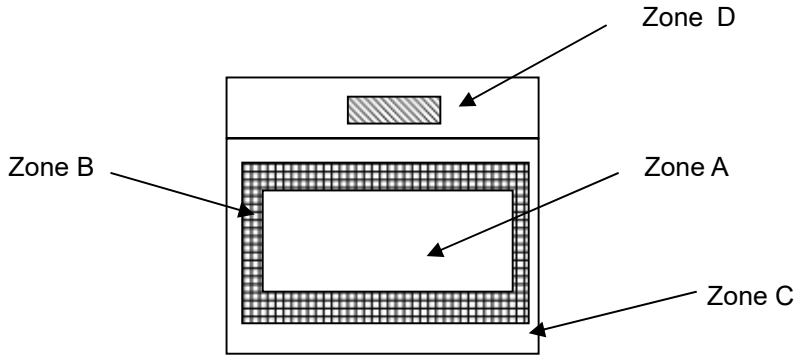
Viewing Angle: Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance: 30-50cm



7.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer

Zone D : IC Bonding Area

Note: As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

7.1.3 Sampling Plan

According to GB/T 2828-2012, normal inspection, Class Ⅱ

AQL:

Major Defect	Minor Defect
0.65	1.5

LCD: Liquid Crystal Display, LCM: Liquid Crystal Module,

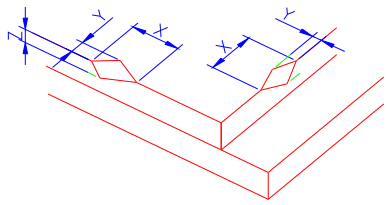
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc…	Major
2	Missing	Missing components and etc…	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed,deformation and etc…	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot,Dim spot,(Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc.	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

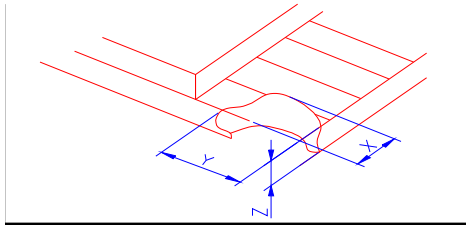
Note1:

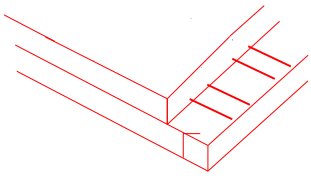
a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

7.1.4 Criteria (Visual)

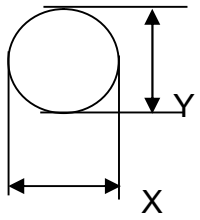
<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 

<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 

<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(3) LCD crack</td><td> 

Crack
Not allowed</td></tr>
</table>

2.0 Spot defect



Φ=(X+Y)/2

① light dot（ black/white spot , pinhole, stain，etc.）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧6mm)		
0.25<Φ≤0.4	2(distance≧6mm)		
Φ>0.4	0		

② Dim spot（light leakage、dent、dark spot，etc）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧6mm)		
0.25<Φ≤0.4	2(distance≧6mm)		
Φ>0.4	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.5	2(distance≧6mm)		
Φ>0.5	0		

④Polarizer Bubble

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.4	3(distance≧6mm)		
Φ>0.4	0		

3.0 LCD Pixel defect

Pixel bad points

Item	Zone A	Acceptable Qty
Bright dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Dark dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm
Total bright and dark dot		N≤4

Note:

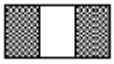
A) Bright dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

C) 2 dot adjacent = 1 pair = 2 dots

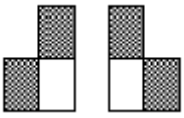
Picture:

2 dot adjacent

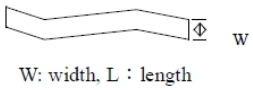


2 dot adjacent

2 dot adjacent (vertical)



2 dot adjacent (slant)

<table>
<tr>
<td>4.0</td>
<td>Line defect (LCD /Polarizer backlight black/white line, scratch, stain)
 

N：Count</td>
<td>
<table>
<tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.03</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.04</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.04<W≤0.05</td><td>L≤2.0</td><td colspan="2">N≤1</td></tr>
<tr><td>W>0.05</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td>
</tr>
<tr>
<td>5.0</td>
<td>Electronic Components SMT.</td>
<td>Not allow missing parts，solderless connection，cold solder joint，mismatch，The positive and negative polarity opposite</td>
</tr>
<tr>
<td>6.0</td>
<td>Display color& Brightness.</td>
<td>1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td>
</tr>
<tr>
<td>7.0</td>
<td>LCD Mura/Waving
/
Hot spot</td>
<td>Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.</td>
</tr>
</table>

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

8. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	+70°C, 96h	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1. Air bubble in the LCD; 2. Non-display; 3. Missing segments/line; 4. Glass crack; 5. Current IDD is twice higher than initial value.
Low Temperature Operating	-20°C, 96h	
High Temperature Storage	+80°C, 96h	
Low Temperature Storage	-30°C, 96h	
High Temperature & High Humidity Operating	+60°C, 90% RH ,96h	
Thermal Shock (Non-operation)	-10°C, 30 min ↔ +60°C, 30 min, Change time: 5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8kV, 5times; Contact:±6kV, 5 times; (Environment: 15°C~35°C, 30%~60%).	
Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX)	

Remark:

1. The test samples should be applied to only one test item.
2. Sample size for each test item is 5~10pcs.
3. For Damp Proof Test, Pure water (Resistance > 10MΩ) should be used.
4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
5. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6. The color fading mura of polarizing filter should not care.

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the “Power ON” condition.

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0°C to 35°C
and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed.
Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.