

27.12.2024

Revision History

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27.12.2024	0	ALL	FIRST ISSUE

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* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amo rphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit,back-light unit. The resolution of a 3.46 " TFT-LCD contains 340xRGBx800 Pixels, and can display up to 65k/262k colors.

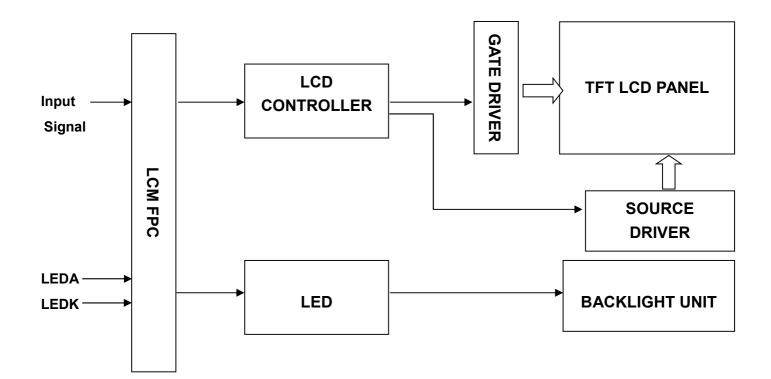
* Features

General Information	Specification	l la it	Nata
Items	Main Panel	Unit	Note
Display Area(AA)	33.97 x *81.00 (3.46 Inch)	mm	-
Driver Element	TFT Active Matrix	-	-
Display Colors	65k / 262k	colors	-
Number of Pixels	340 x RGB x 800	dots	-
Pixel Arrangement	RGB Vertical Stripe	-	-
Viewing Angle	ALL	o'clock	-
Controller IC	ST7701S (Sitronix)	-	-
LCM Interface	3-SPI + 16BIT-RGB	-	-
Display Mode	IPS, Transmissive / Normally Black	-	-
Operating Temperature	-20°C ~ +70°C	°C	-
Storage Temperature	-30°C ~ +80°C	°C	-

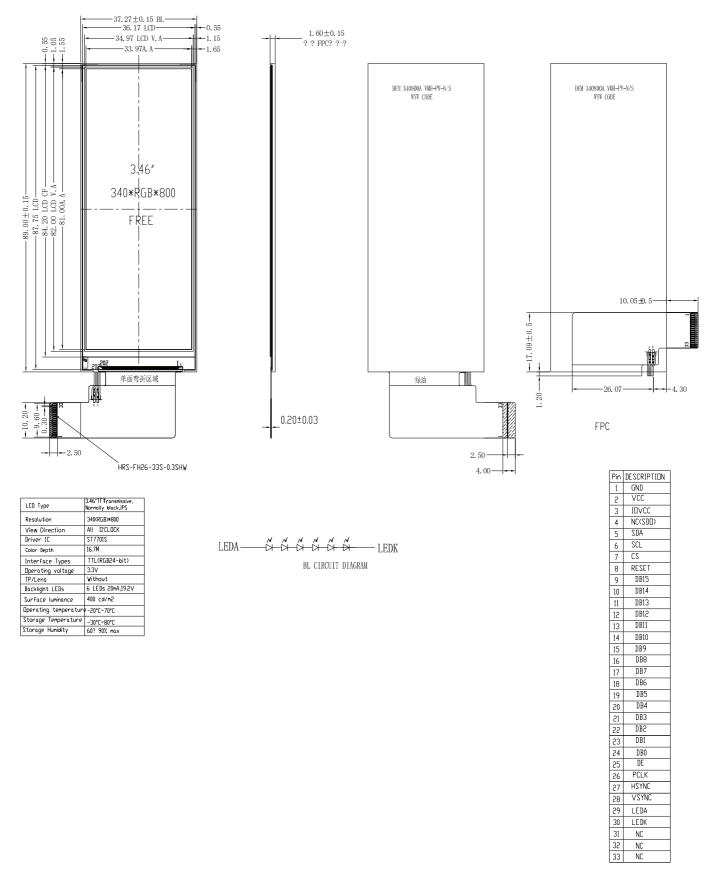
* Mechanical Information

	ltem	Min.	Тур.	Max.	Unit	Note
	Horizontal(H)	-	37.27	-	mm	-
Module Size	Vertical(V)	-	89.0	-	mm	-
SIZE	Depth(D)	-	1.6	-	mm	-
	Weight		10	-	g	-

1. Block Diagram



2. Outline Dimension



3. Input Terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O		
1	GND	Ground.	Р		
2	VCC	Supply voltage (3.3V).	Р		
3	IOVC	Supply Voltage (Logic)(1.8~3.3V).	Р		
4	NC(SDO)	-	-		
5	SDA	Serial data input/output bidirectional pin for SPI Interface.	I/O		
6	SCL	SCL: Serial clock input for SPI interface.	I		
		A chip select signal			
7	CS	Low: the chip is selected and accessible	I		
		High: the chip is not selected and not accessible			
		The external reset input			
8	RESET	Initializes the chip with a low input. Be sure to execute	I		
		a power-on reset after supplying power.			
9-24	DB15-DB0	16-bit parallel data bus for RGB Interface.	I		
		Data enable signal for RGB interface operation			
25	DE	Low: access enabled			
25	DL	High: access inhibited	I		
		Fix to IOVCC or GND level when not in use.			
26	PCLK	Dot clock signal for RGB interface operation			
20	FOLK	Fix to IOVCC or GND level when not in use.	I		
27	HSYNC	Line synchronizing signal for RGB interface operation			
21	Horne	Fix to IOVCC or GND level when not in use.	1		
28	VSYNC	Frame synchronizing signal for RGB interface operation			
20	VOTINO	Fix to IOVCC or GND level when not in use.	1		
29	LEDA	Anode pin of backlight.	Р		
30	LEDK	Cathode pin of backlight.	Р		
31-33	NC	-	-		

4. LCD Optical Characteristics

4.1 Optical Specification

Item		Symbol	Condition	Min.	Тур.	Max.	Unit.	Note
Contrast Ra	tio	CR			600			(1)(2)
Response Time	Rising Falling	T _{R+} T _F			30	50	msec	(1)(3)
Uniformity		S(%)			60		%	C-light
		Wx	Θ=0	0.2184	0.2584	0.2984		(1)(4)
	White	W _Y	Normal	0.2718	0.3118	0.3518		
	Red	Rx	Viewing	0.5864	0.6264	0.6664		
Color Filter		Ry	Angle	0.3058	0.3458	0.3858		
Chromacicity	Green	Gx		0.2857	0.3257	0.3657		
		Gy		0.5066	0.5466	0.5866		
		Bx		0.1083	0.1483	0.1883		
	Blue	B _Y		0.0452	0.0852	0.1252		
		ΘL			80			(1)(4)
	Hor.	ΘR			80			
Viewing Angle		ΘU	CR>10		80			
	Ver.	ΘD			80			
Option View Dir	ection				ALL			(5)

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding: dark room

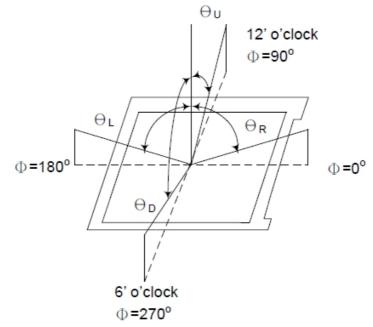
Ambient temperature: 25°C ± 2°C

15min. warm-up time.

Measuring Equipment

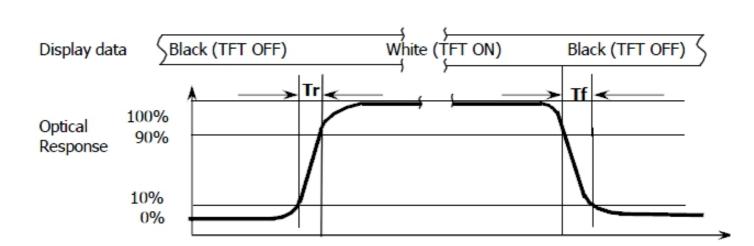
FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

Note (1): Definition of Viewing Angle:



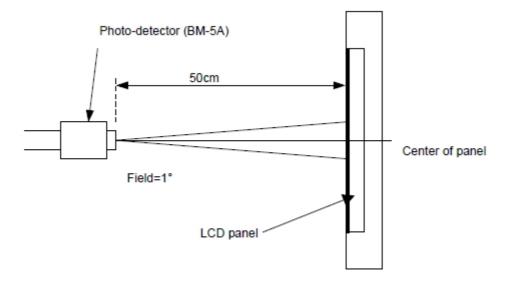
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

CR = Luminance with all pixels white Luminance with all pixels black



Note (3): Response Time

Note (4): Definition of optical measurement setup



5. Electrical Characteristics

5.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VCC	-0.3	4.6	V	Note1
Digital Interface Supply Voltage	IOVCC	-0.3	4.6	V	-
Operating Temperature	T _{OP}	-20	+70	°C	-
Storage Temperature	Тѕт	-30	+80	°C	-

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Тур.	Max.	Unit	Note
Digital Supply Voltage	VCC	2.5	3.3	3.6	V	-
Digital Interface Supply Voltage	IOVCC	1.65	1.8	3.3		-
Normal Mode Current	ICC		28		mA	-
	Vін	0.7* lovcc		lovcc	V	-
Level Input Voltage	VIL	GND		0.3* lovcc	V	-
	Vон	0.8*lovcc		lovcc	V	-
Level Output Voltage	Vol	GND		0.2*lovcc	V	-

5.3 LED Backlight Characteristics

Item	Symbol	Min.	Тур.	Max.	Unit	Note
Forward Current	lf	15	20		mA	-
Forward Voltage	VF		19.2		V	-
LCM Luminance (I⊧ =20mA)	LV	350	400		cd/m2	Note3
LED Lifetime	Hr		50000		Hour	Note1,2
Uniformity	Avg	80			%	Note3

The Backlight system is edge-lighting type with 6 chips LED

Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25°C±3°C, typical IL value indicated in the above table until the brightness becomes less than 50%.

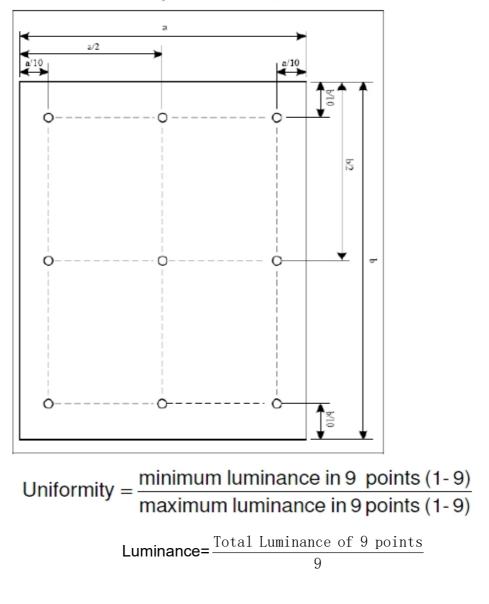
Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 20mA.

The constant current driving method is suggested.

LEDA ______ A A A A A LEDK

BL CIRCUIT DIAGRAM

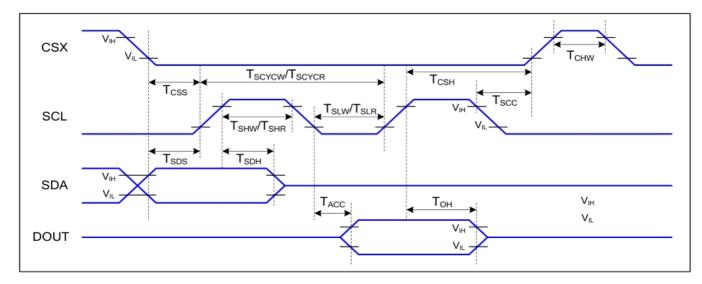
Note (3) Luminance Uniformity of these 9 points is defined as below:



6. AC Characteristics

6.1 Serial Interface Characteristics (3-Line Serial):

IOVCC=1.8V,VCI=2.8V,Ta=25°C



3-Line Serial Interface Timing Characteristics

Signal	Symbol	Parameter	Min	Max	Unit	Description
	T _{css}	Chip select setup time (write)	15		ns	
	Т _{сsн}	Chip select hold time (write)	15		ns	
CSX	T _{CSS}	Chip select setup time (read)	60		ns	
	T _{SCC}	Chip select hold time (read)	60		ns	
	T _{CHW}	Chip select "H" pulse width	40		ns	
	T _{SCYCW}	Serial clock cycle (Write)	66		ns	
	T _{SHW}	SCL "H" pulse width (Write)	15		ns	
SCL	T _{SLW}	SCL "L" pulse width (Write)	15		ns	
SOL	T _{SCYCR}	Serial clock cycle (Read)	150		ns	
	T _{SHR}	SCL "H" pulse width (Read)	60		ns	
	T _{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA	T _{SDS}	Data setup time	10		ns	
(DIN)	T _{SDH}	Data hold time	10		ns	

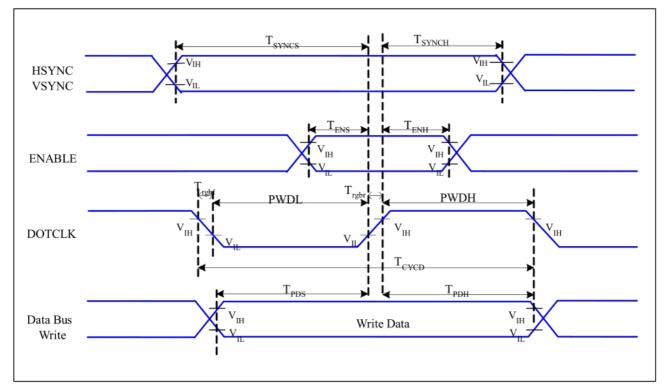
3-Line Serial Interface Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

6.2.RGB Interface Characteristics :

IOVCC=1.8V,VCI=2.8V,Ta=25°C

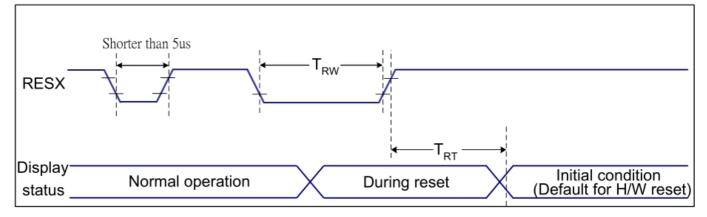


RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T _{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T _{ENS}	Enable Setup Time	5	-	ns	
	T _{ENH}	Enable Hold Time	5	-	ns	
	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
DOTCLK	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
DUTCLK	T _{CYCD}	DOTCLK Cycle Time	33	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DP	T _{PDS}	PD Data Setup Time	5	-	ns	
DB	T _{PDH}	PD Data Hold Time	5	-	ns	

18/16 Bits RGB Interface Timing Characteristics

6.3 Reset Input Timing:



Reset Timing

Related Pins	Symbol	Parameter	MIN	МАХ	Unit
TRW		Reset pulse duration	10	-	us
RESX	тот	Penet especi	-	5 (Note 1, 5)	ms
	TRT	Reset cancel		120(Note 1, 6, 7)	ms

Reset Timing

Notes:

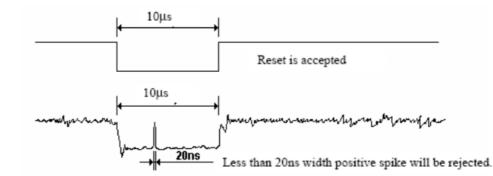
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action	
Shorter than 5us	Reset Rejected	
Longer than 9us	Reset	
Between 5us and 9us	Reset starts	

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for

120msec.

7. RGB Interface

The ST7701 support RGB interface Mode 1 and Mode 2. The interface signals as shown in ST7701S datasheet table 6.3.1.The Mode 1 and Mode 2 function is select by setting in the Command 2, please reference application note. In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D[23:0]), when DE is high state.The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer PCLK, VS and HS signal to ST7701.In RGB Mode 2, back porch of Vsync is defined by VBP[5:0]of RGBPRCTR command. And back porch of Hsync is defined by HBP[5:0] of RGBPRCTR command.

Front porch of Vsync is defined by VFP[5:0] of RGBPRCTR command. And front porch of Hsync is defined by H FP[5:0] of RGBPRCTR command.

RGB I/F Mode	PCLK	DE	VS	HS	DB[23:0]	Register for Blanking Porch setting
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

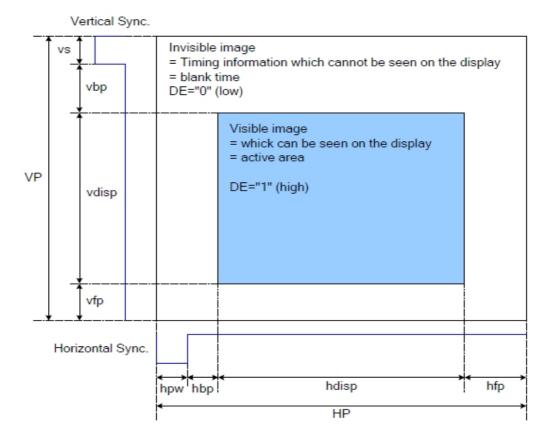
Symbol	Name	Description	
PCLK	Pixel clock	Pixel clock for capturing pixels at display interface	
HS	Horizontal sync	Horizontal synchronization timing signal	
VS	Vertical sync	Vertical synchronization timing signal	
DE	Data enable	Data enable signal (assertion indicates valid pixels)	
DB[23:0]	Pixel data	Pixel data in 16-bit, 18-bit and 24-bit format	

The interface signals of RGB interface

The back porch and front porch are used to set the RGB interface timing.

7.1.1 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function.



DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Тур.	Max.	Unit
DCLK frequency	FCLK	-	(25)	-	MHz
Horizontal Sync. Width	hpw	1	(4)	255	Clock
Horizontal Sync. Back Porch	hbp	1	(20)	255	Clock
Horizontal Sync. Front Porch	hfp	1	(10)		Clock
Vertical Sync. Width	VS	1	(4)	254	Line
Vertical Sync. Back Porch	vbp	1	(10)	254	Line
Vertical Sync. Front Porch	vfp	1	(8)		Line

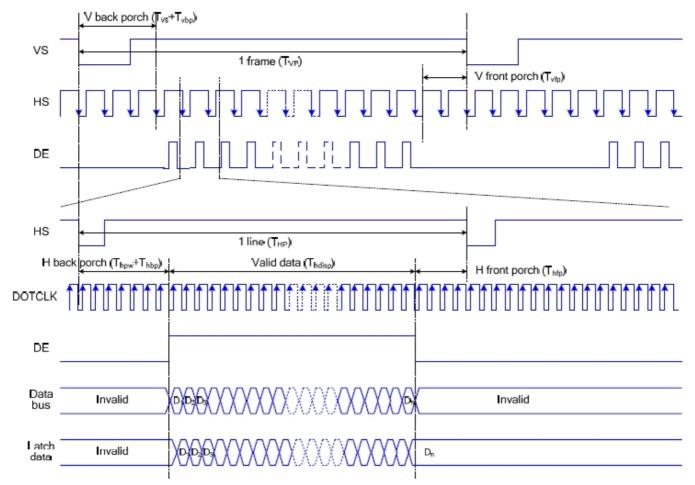
Note: 1. Typical value are related to the setting frame rate is 60Hz.

7.1.2 RGB Interface Mode Selection

ST7701S supports two kinds of RGB interface, DE mode and HV mode. The table shown below uses command C3h to select RGB interface mode.

DE/Sync	RGB Mode	
0	DE mode	
1	HV mode	

7.1.3 RGB Interface Timing

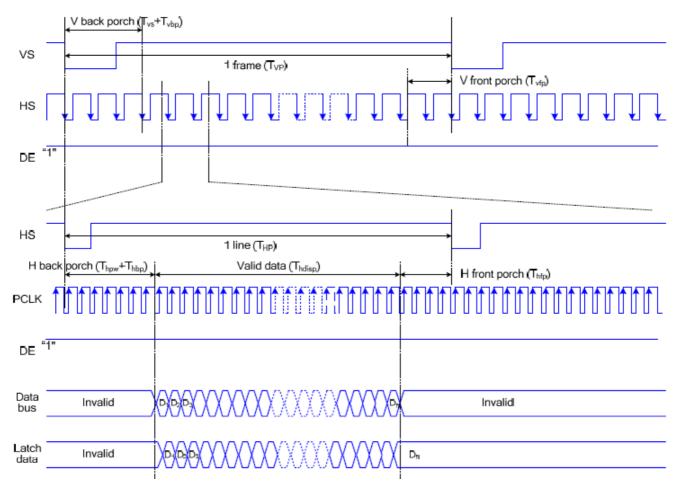


The timing chart of RGB interface DE mode is shown as follows.

Note: The setting of front porch and back porch in host must match that in IC as this mode.

Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.



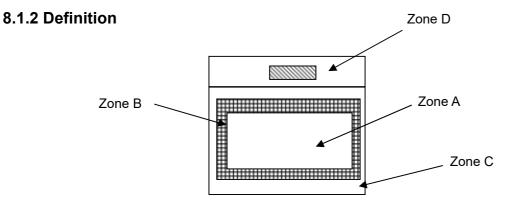
Timing chart of RGB interface HV mod

8. LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended. Temperature: 25°C ± 5°C Humidity: 65%±10%RH Viewing Angle: Normal viewing Angle. Illumination: Single fluorescent lamp (300 to 700Lux) Viewing distance: 30-50cm 0 3 Upper Polarizer Upper Bottom glass Ŕ Bottom Polarizer Light Source



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

Note: As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product Function or appearance after assembly by customer

8.1.3 Sampling Plan

According to GB/T 2828-2012, normal inspection, Class II

AQL:

Major Defect	Minor Defect
0.65	1.5

LCD: Liquid Crystal Display, LCM: Liquid Crystal Module, CTP: Capacitive Touch Panel

No	Items to be inspected	Criteria	Classification of defects	
		1) No display, Open or miss line		
1	Functional defects	2) Display abnormally, Short		
1	Functional delects	3) Backlight no lighting, abnormal lighting.		
		etc	Major	
2	Missing	Missing components and etc	,	
		Overall outline dimension beyond the drawing		
3	Outline dimension	is not allowed,deformation and etc		
4	Color tone	Color unevenness, refer to limited sample		
		Light dot,Dim spot,(Note1)		
5	Spot/Line defect	Polarizer Air Bubble,		
		Polarizer accidented spot and etc	Minor	
6		Good soldering , Peeling off is not allowed		
0	Soldering appearance	and etc		
7	LCD/Polarizer/CTP	Black/White spot/line, scratch, crack, etc.		

Note1:

- a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.
- b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

8.1.4 Criteria (Visual)

Number	Items	Criteria(mm)		
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height	(1) The edge of LCD broken			
L: Length of ITO,		X Y Z		
T: Height of LCD		≤3.0mm <inner border="" line="" of<br="">the seal ≤T</inner>		
	(2)LCD corner broken	XYZ ≤ 3.0 mm $\leq L$ $\leq T$		
	(3) LCD crack	Crack Not allowed		

Product Specification

	Spot defect	 Iight dot (black/white spot , pinhole, stain, etc.) 					
		7	Acceptable Qty				
	↓ Y	Zone Size (mm)	A	В	С		
2.0	k → x	Ф≤0.15	Ignore				
2.0	^	0.15<Ф≤0.25	3(distance≧10mm)		Ignore		
	$\Phi = (X \mid X)/2$	0.25<Ф≤0.4	2(distance≧10mm)		Ignore		
	Φ=(X+Y)/2	Ф>0.4	0				
		◎ Dim spot (light l	eakage、dent、dark sp	oot, etc)			
		Zone	Accep	able Qty			
		Size (mm)	Α	В	С		
		Ф≤0.15	Ignore				
		0.15<Φ≤0.25	3(distance≧10mm)		Ignore		
		0.25<Φ≤0.4	2(distance≧10mm)	_	5		
			Φ>0.40③ Polarizer accidented spot				
				tabla Otu			
		Zone		table Qty			
		Size (mm)	A	В	C		
		Ф≤0.2	Ignore				
		0.2<Φ≤0.5	2(distance≧10	mm)	Ignore		
		Φ>0.5	0				
		④Polarizer Bubble			·		
		Zone Acceptable Qty					
		Size (mm)	A	3	С		
		Ф≤0.2	Ignore				
		0.2<Ф≤0.4	2(distance≧10mm)		Ignore		
		Φ>0.4	0				

3.0	LCD Pixel defect	Pixel bad points				
		Item	Zone A	Acceptable Qty		
			Random	N≤2		
		Bright dot	2 dots adjacent	N≤0		
			3 dots adjacent	N≤0		
			Random	N≤3		
		Dark dot	2 dots adjacent	N≤0		
			3 dots adjacent	N≤0		
		Distance	 Minimum Distance Between Bright dots. Minimum Distance Between dark dots Minimum Distance Between dark and bright dot. 	5mm		
		Total bright and dark dot		N≤4		
		Note:		1		
		A) Bright dot	: Dots appear bright and unchanged	d in size in which		
		LCD pane	l is displaying under black pattern.			
		B) Dark dot:	Dots appear dark and unchanged in	size in which		
		LCD pane	l is displaying under pure red, green	, blue picture.		
		C) 2 dot adja Picture:	cent = 1 pair = 2 dots			
		2 dot adja	cent 2 dot adjacent			
		2 dot adjacen	t (vertical) 2 dot adjacent (slant)		

	Line defect (LCD					
	/Polarizer backlight	\\/idth(mm)	Length(m	Acce	eptable Q	ty
	black/white line,	Width(mm)	m)	А	В	С
	scratch, stain)	Ф≤0.05	Ignore	Ignore)	
4.0		0.05 <w≤0.06< td=""><td>L≤5.0</td><td>N≤3</td><td></td><td>Ignore</td></w≤0.06<>	L≤5.0	N≤3		Ignore
	Ψ W: width, L : length	0.06 <w≤0.08< td=""><td>L≤4.0</td><td>N≤2</td><td></td><td></td></w≤0.08<>	L≤4.0	N≤2		
	N : Count	W>0.08		Define as spo	t defect	
	Electronic Componen	Not allow missing parts, solderless connection, cold solder joint, mi smatch, The positive and negative polarity opposite				
5.0	ts SMT.					
6.0	Display color& Brigh tness.	 Color: Measuring the color coordinates, The measurement standa rd according to the datasheet or samples. Brightness: Measuring the brightness of White screen, The meas urement standard according to the datasheet or Samples. 				
7.0	LCD Mura/Waving/ Hot spot	Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.				

Criteria (functional items)

Number	Itoms	Criteria (mm)
Nulliber 1	Items	Not allowed
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	CTP no function	

9. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	+70°C,96h	
Low Temperature Operating	-20°C, 96h	
High Temperature Storage	+80°C, 96h	
Low Temperature Storage	-30°C, 96h	Inspection after 2~4hours storage at room
High Temperature & High	+60°C, 90% RH ,96h	temperature, the sample
Humidity Operating		shall be free of defects:
Thermal Shock (Non-	-20°C, 30 min ↔ +70°C, 30 min,	1. Air bubble in the LCD;
operation)	Change time: 5min 20CYC.	2. Non-display;
	C=150pF, R=330,5points/panel	3. Missing segments/line;
ESD test	Air:±8kV, 5times; Contact:±6kV, 5 times;	4. Glass crack;
	(Environment: 15°C~35°C, 30%~60%).	5. Current IDD is twice
	Frequency range: 10~55Hz, Stroke:1.5mm	higher than initial value.
Vibration (Non-operation)	Sweep:10Hz~55Hz~10Hz 2 hours for each direction	
	of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM BOX)	

Remark:

- 1. The test samples should be applied to only one test item.
- 2. Sample size for each test item is 5~10pcs.
- 3. For Damp Proof Test, Pure water (Resistance > $10M\Omega$) should be used.
- 4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.
 - Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and backlight unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

10.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.
 It is highly recommended to store the module with temperature from 0°C to 35°C and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed.Formation of dewdrops may cause an abnormal operation or a failure of the module.In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.