Display Elektronik GmbH

DATA SHEET

TFT MODULE

DEM 320320B VMX-PW-N

(C-TOUCH)

2,73“ TFT

Product Specification

Version: 0

16.07.2025

Revision History

Date	Rev. No.	Page	Summary
16.07.2025	0	ALL	FIRST ISSUE

Contents

1. Basic Specifications

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses a morphous silicon TFT as a switching device. This module is cimposed of a transmissive type TFT-LCD Panel, driver circuit,capacitance touch panel, backlight unit.

The resolution of a 2.73 " TFT-LCD contains 320x320 pixels, and can display up to 16.7 Million colors.

1.1 TFT Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display Area (AA)	48.96 x 48.96 (2.73 Inch)	mm	-
Driver Element	TFT Active Matrix	-	-
Display Colors	16.7 Million	colors	-
Number of Pixels	320 x RGB x 320	dots	-
Pixel Arrangement	RGB vertical stripe	-	-
Pixel Pitch	0.153 x 0.153	mm	-
Viewing Angle	ALL	o'clock	-
Controller IC	ST7796 (Sitronix)	-	-
LCM Interface	3/4 Serial 8/9/16/18-Bit-MCU 3/4SPI + 16/18-BIT-RGB	-	-
Display Mode	IPS, Transmissive / Normally Black	-	-
Operating Temperature	-30 ~ +85	°C	-
Storage Temperature	-30 ~ +85	°C	-
Module Bonding Technology	Optical Bonding between LCM and CTP	-	-

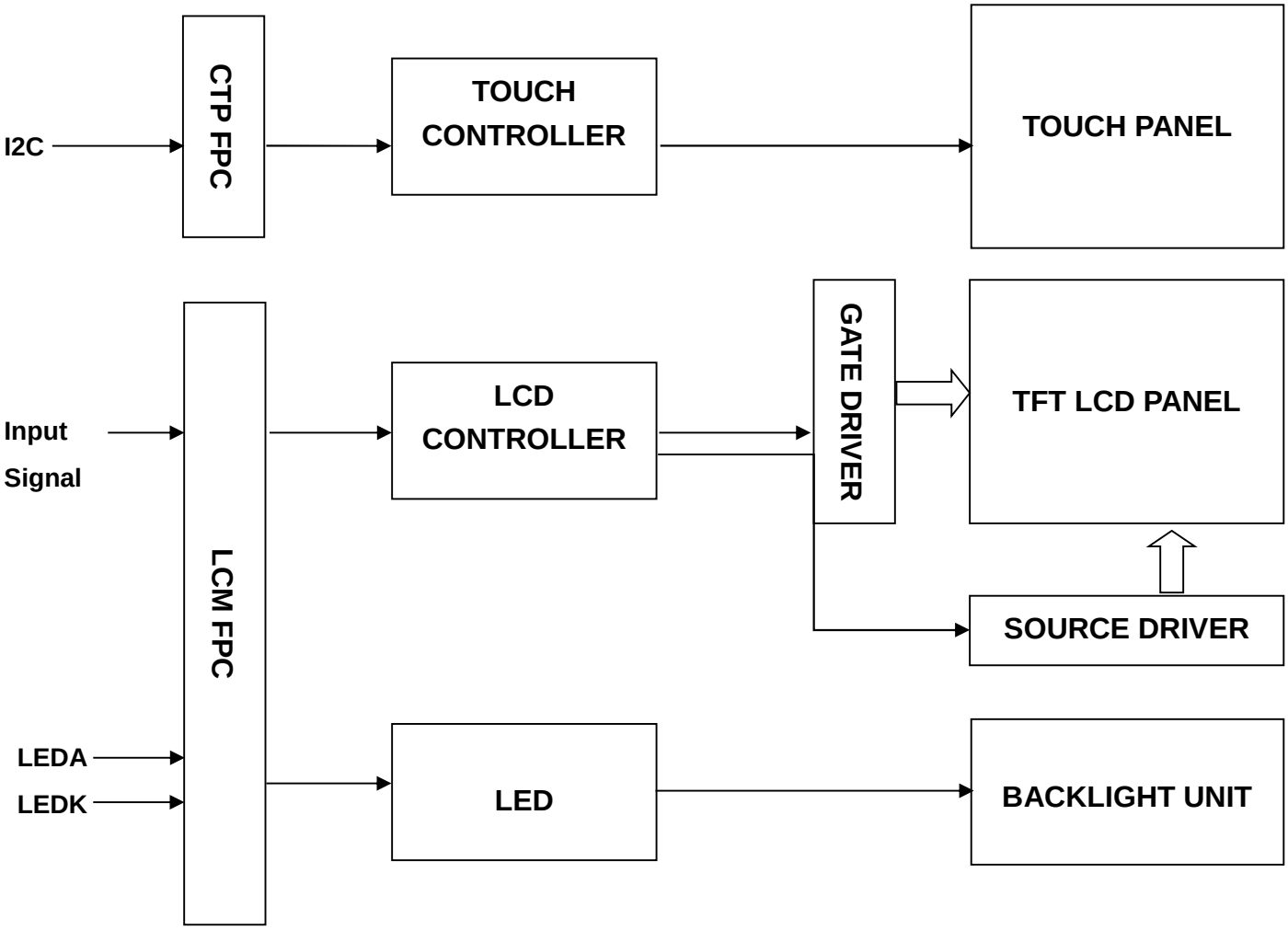
1.2 CTP Features

General Information Items	Specification	Unit	Note
	Main Panel		
Resolution	320 x 320	-	-
Structure	G+G	-	-
Controller IC	FT5446U (Focaltech)	-	-
Interface	I2C	-	-
Slave Adress	t.b.d.	-	-
Touch mode	Five Point	-	-
Logic level	1.8 or 3.3	V	Set by VDDIO

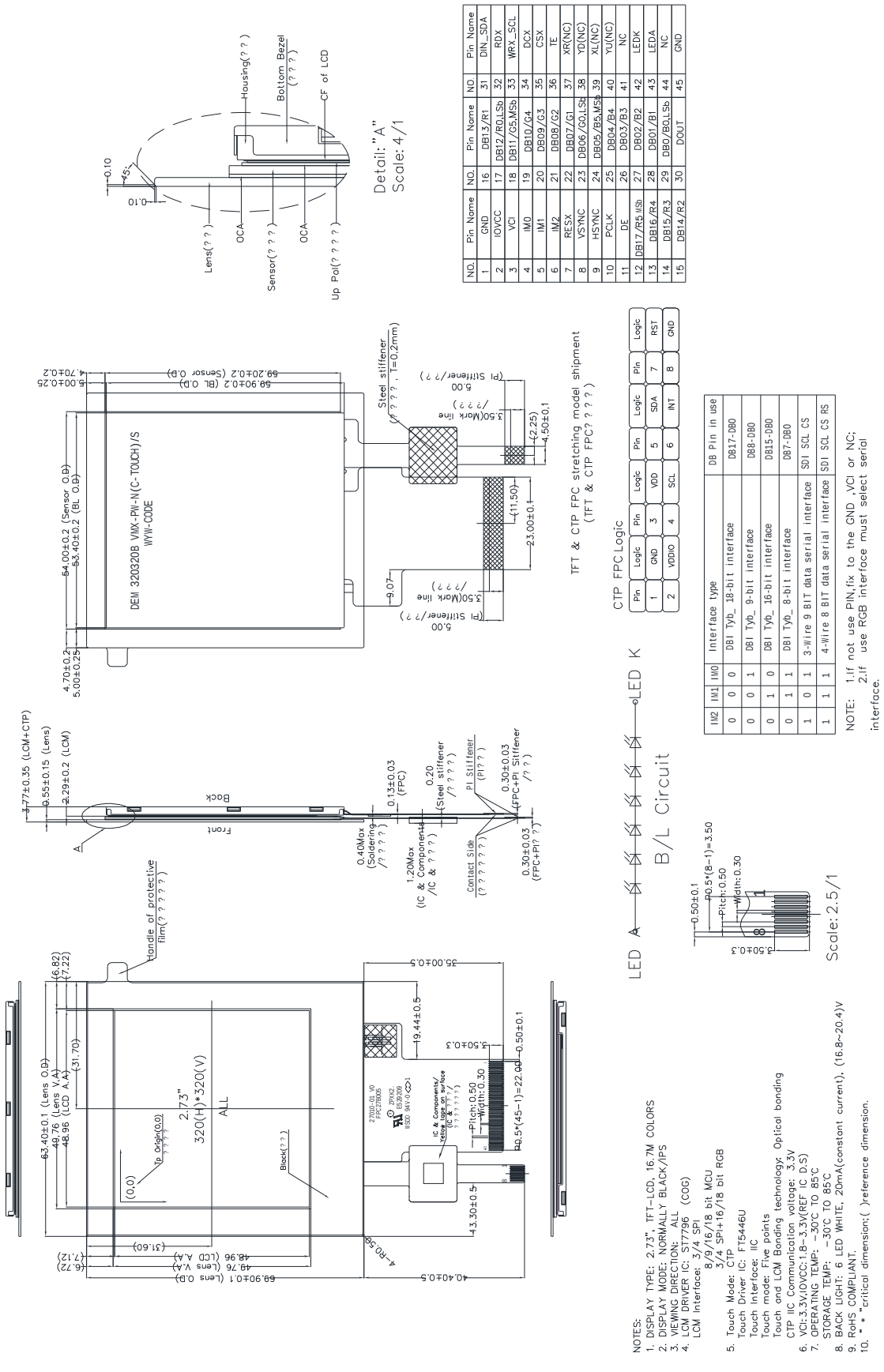
1.3 Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	-	63.4	-	mm	-
	Vertical(V)	-	69.9	-	mm	-
	Depth(D)	-	3.77	--	mm	-
Weight		-	TBD	-	g	-

2. Block Diagram



3. Outline Dimension



NO.	Pin Name	NO.	Pin Name	NO.	Pin Name
1	GND	16	DB13/R1	31	DIN_SDA
2	IOVCC	17	DB12/R0,LSb	32	RDX
3	VCI	18	DB11/G5,MSb	33	WRX_SCL
4	IM0	19	DB10/G4	34	DCX
5	IM1	20	DB09/G3	35	CSX
6	IM2	21	DB08/G2	36	TE
7	RESX	22	DB07/G1	37	XR(NC)
8	VSYNC	23	DB06/G0,LSb	38	YD(NC)
9	HSYNC	24	DB05/B5,MSb	39	XL(NC)
10	PCLK	25	DB04/B4	40	YU(NC)
11	DE	26	DB03/B3	41	NC
12	DB17/R5,MSb	27	DB02/B2	42	LEDK
13	DB16/R4	28	DB01/B1	43	LEDA
14	DB15/R3	29	DB0/B0,LSb	44	NC
15	DB14/R2	30	DOUT	45	GND

Pin	Logic	Pin	Logic	Pin	Logic	Pin	Logic
1	GND	3	VDD	5	SDA	7	RST
2	VDDIO	4	SCL	6	INT	8	GND

IM2	IM1	IM0	Interface type	DB Pin in use
0	0	0	DBI Typ_ 18-bit interface	DB17-DB0
0	0	1	DBI Typ_ 9-bit interface	DB8-DB0
0	1	0	DBI Typ_ 16-bit interface	DB15-DB0
0	1	1	DBI Typ_ 8-bit interface	DB7-DB0
1	0	1	3-Wire 9 BIT data serial interface	SDI SCL CS
1	1	1	4-Wire 8 BIT data serial interface	SDI SCL CS RS

NOTE: 1.If not use PIN,fix to the GND ,VCI or NC;
2.If use RGB interface must select serial interface.

NOTES:
1. DISPLAY TYPE: 2.73", TFT-LCD, 16.7M COLORS
2. DISPLAY MODE: NORMALLY BLACK/IPS
3. VIEWING DIRECTION: ALL
4. LCM DRIVER IC: ST7796 (COG)
   LCM Interface: 3/4 SPI
   8/9/16/18 bit MCU
   3/4 SPI+16/18 bit RGB
5. Touch Mode: CTP
   Touch Driver IC: FT5446U
   Touch Interface: IIC
   Touch mode: Five points
   Touch and LCM Bonding technology: Optical bonding
   CTP IIC Communication voltage: 3.3V
6. VCI:3.3V,IOVCC:1.8~3.3V(REF IC D.S)
7. OPERATING TEMP: -30°C TO 85°C
   STORAGE TEMP: -30°C TO 85°C
8. BACK LIGHT: 6 LED WHITE, 20mA(constant current), (16.8~20.4)V
9. RoHS COMPLIANT.
10. " * "critical dimension;( )reference dimension.

4. Input Terminal Pin Assignment

4.1 TFT PIN Definition

<table>
<tr><th>NO.</th><th>SYMBOL</th><th>DISCRIPTION</th><th>I/O</th></tr>
<tr><td>1</td><td>GND</td><td>Ground.</td><td>P</td></tr>
<tr><td>2</td><td>IOVCC</td><td>Supply voltage for IO(1.8-3.3V)</td><td>P</td></tr>
<tr><td>3</td><td>VCI</td><td>Supply voltage(3.3V).</td><td>P</td></tr>
<tr><td>4</td><td>IM0</td><td rowspan="4"><table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface type</th><th>DB Pin in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DBI Tyb_ 18-bit interface</td><td>DB17-DB0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DBI Tyb_ 9-bit interface</td><td>DB8-DB0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DBI Tyb_ 16-bit interface</td><td>DB15-DB0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DBI Tyb_ 8-bit interface</td><td>DB7-DB0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-Wire 9 BIT data serial interface</td><td>SDA SCL CS</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>4-Wire 8 BIT data serial interface</td><td>SDA SCL CS RS</td></tr>
</table></td><td rowspan="4">I</td></tr>
<tr><td>5</td><td>IM1</td></tr>
<tr><td>6</td><td>IM2</td></tr>
<tr><td>7</td><td>RESX</td><td>- This signal will reset the device and it must be applied to properly initialize the chip.
- Signal is active low.</td><td>I</td></tr>
<tr><td>8</td><td>VSYNC</td><td>Frame synchronizing signal for RGB interface operation.
fix this pin at VCI or GND when not in use.</td><td>I</td></tr>
<tr><td>9</td><td>HSYNC</td><td>Line synchronizing signal for RGB interface operation.
fix this pin at VCI or GND when not in use</td><td>I</td></tr>
<tr><td>10</td><td>PCLK</td><td>Dot clock signal for RGB interface operation
Fix this pin at VCI or GND when not in use.</td><td>I</td></tr>
<tr><td>11</td><td>DE</td><td>Data enable signal for RGB interface operation.
fix this pin at VCI or GND when not in use.</td><td>I</td></tr>
<tr><td>12-29</td><td>DB17-DB0</td><td>18-bit parallel bi-directional data bus for MCU system and RGB interface mode .
Fix to GND level when not in use</td><td>I/O</td></tr>
<tr><td>30</td><td>DOUT</td><td>- SPI interface output pin.
- The data is outputted on the falling edge of the SCL signal.
- If not used, please fix this pin at floating.</td><td>O</td></tr>
<tr><td>31</td><td>DIN_SDA</td><td>- SPI interface input/output pin.
- The data is latched on the rising edge of the SCL signal.
- If not used, please fix this pin GND level.</td><td>I</td></tr>
<tr><td>32</td><td>RDX</td><td>- Read enable in 8080 MCU parallel interface. Low-active.
- If not used, please fix this pin GND level.</td><td>I</td></tr>
<tr><td>33</td><td>WRX_SCL</td><td>- Write enable in MCU parallel interface.
- In SPI mode, this pin is used as SCL.</td><td>I</td></tr>
</table>

		- If not used, please fix this pin GND level.	
34	DCX	-Display data/command selection (RS) pin in MCU interface. DCX= ' 1 ' : display data or parameter. DCX= ' 0 ' : register index / command. - If not used, please fix this pin at GND level.	I
35	CSX	Chip select input pin ("Low" enable). fix this pin at VCI or GND when not in use.	I
36	TE	Serve as a TE (Tearing Effect) output signal Leave the pin open when not in use	O
37	XR(NC)	Touch panel Right Glass Terminal	A/D
38	YD(NC)	Touch panel Bottom Film Terminal	A/D
39	XL(NC)	Touch panel LEFT Glass Terminal	A/D
40	YU(NC)	Touch panel Top Film Terminal	A/D
41	NC	NC	
42	LEDK	Cathode pin OF backlight	P
43	LEDA	Anode pin of backlight	P
44	NC	NC	-
45	GND	Ground.	P

4.2 CTP PIN Definition

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VDDIO	I/O power supply voltage.	P
3	VDD	Supply voltage.	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P

5. LCD Optical Characteristics

5.1 Optical Specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal Viewing Angle	1000	1200	--		(1)(2)
Response Time	Rising	$T_{R+}T_F$		--	30	35	msec	(1)(3)
	Falling							
Color Gamut		S(%)		--	63	--	%	
Color Filter Chromacicity	White	W_X		-0.04	0.3012	+0.04	--	(1)(4) CA-310
		W_Y			0.3417			
	Red	R_X			0.6418			
		R_Y			0.3523			
	Green	G_X			0.3209			
		G_Y			0.5835			
	Blue	B_X			0.1427			
		B_Y			0.0900			
Viewing Angle	Hor.	ΘL	CR>10	80	85	--	--	(1)(4)
		ΘR		80	85	--		
	Ver.	ΘU		80	85	--		
		ΘD		80	85	--		
Option View Direction		ALL						

* The data comes from the LCD specification.

Measuring Condition

Measuring surrounding: dark room

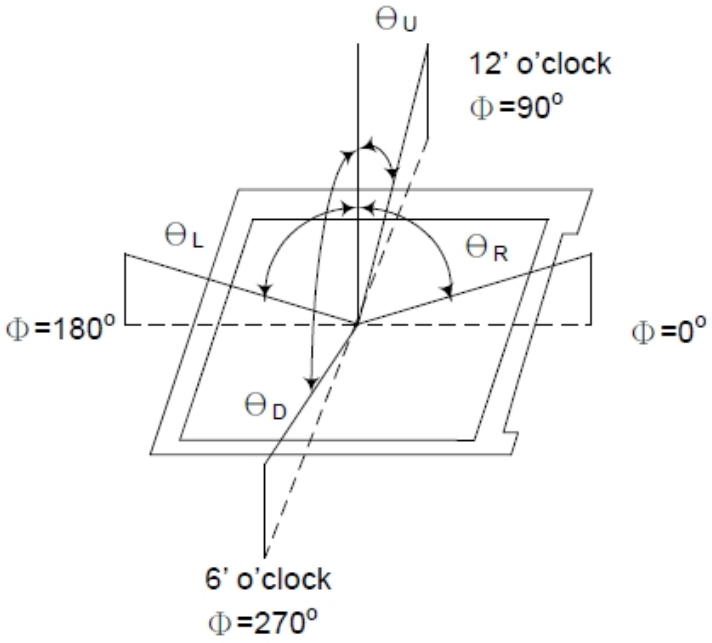
Ambient temperature: 25°C ± 2°C

15min. warm-up time

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

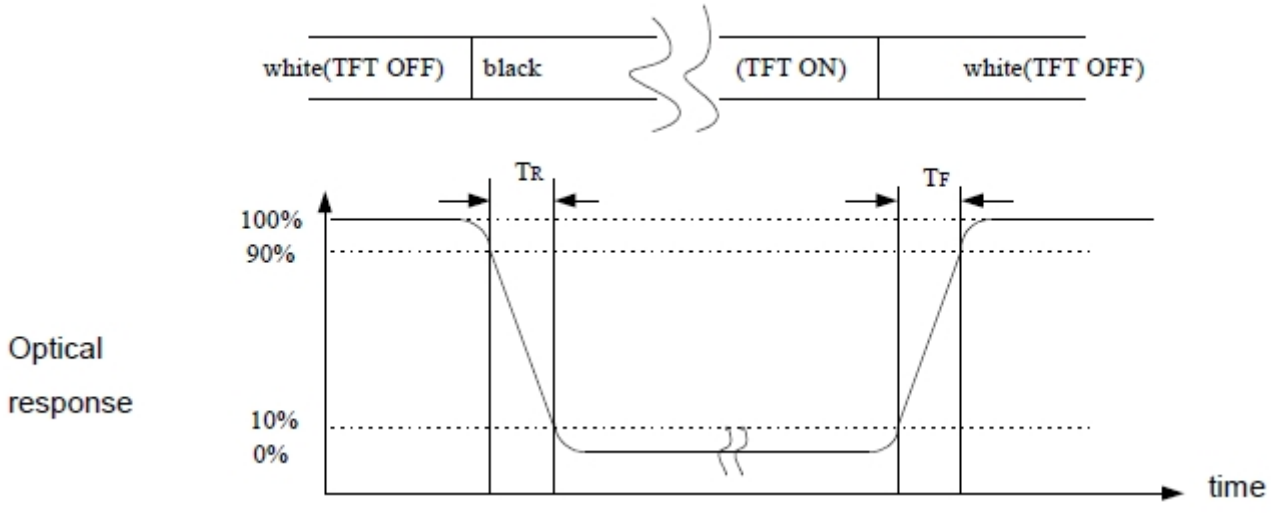
Note (1): Definition of Viewing Angle:



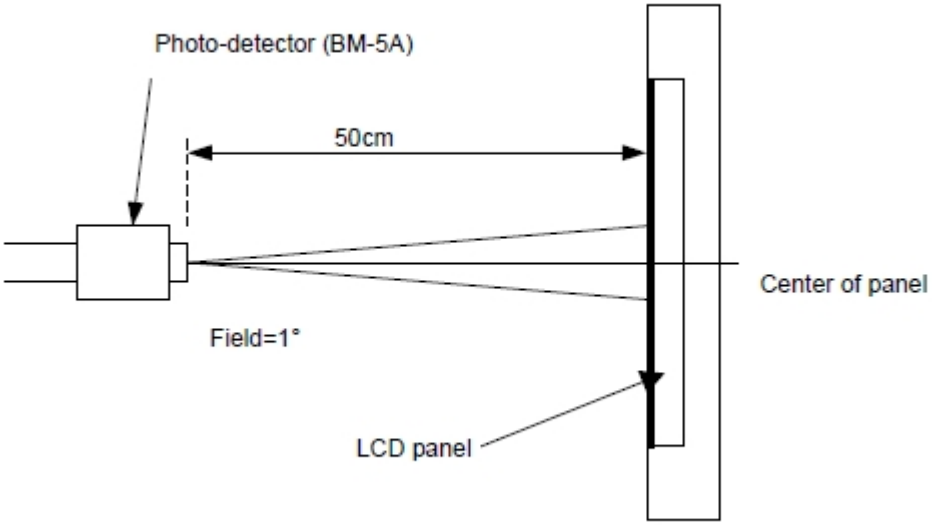
Note (2): Definition of Contrast Ratio (CR): measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time:



Note (4): Definition of optical measurement setup



6. Electrical Characteristics

6.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VCI	-0.3	+4.6	V	Note1
Digital Interface Supply Voltage	IOVCC	-0.3	+4.6	V	Note1
Operating Temperature	T_{OP}	-30	+85	°C	-
Storage Temperature	T_{ST}	-30	+85	°C	-

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

6.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.5	3.3	3.6	V	--
Digital Interface Supply Voltage	IOVCC	1.65	1.8	3.3	V	--
Normal Mode Current Consumption	IDD	--	13	--	mA	--
Level Input Voltage	V_{IH}	0.7*IOVCC	--	IOVCC	V	--
	V_{IL}	GND	--	0.3*IOVCC	V	--
Level Output Voltage	V_{OH}	0.8*IOVCC	--	IOVCC	V	--
	V_{OL}	GND	--	0.2*IOVCC	V	--

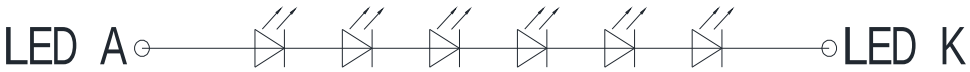
6.3 LED Backlight Characteristics

The backlight system is edge-lighting type with 6 chips LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	--	20	--	mA	--
Forward Voltage	V_F	16.8	19.2	20.4	V	--
LCM Luminance	Lv	700	800	--	cd/m2	Note3
LED Lifetime	Hr	50000	--	--	Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

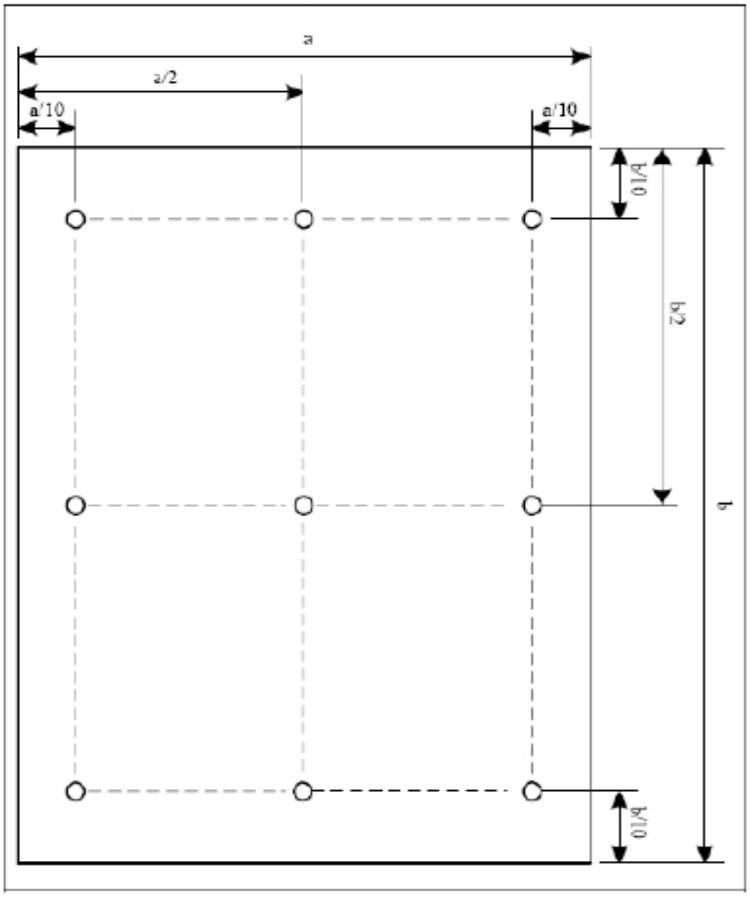
Note1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25°C ± 3°C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 20mA. The constant current driving method is suggested.



B/L Circuit

Note (3) Luminance Uniformity of these 9 points is defined as below:

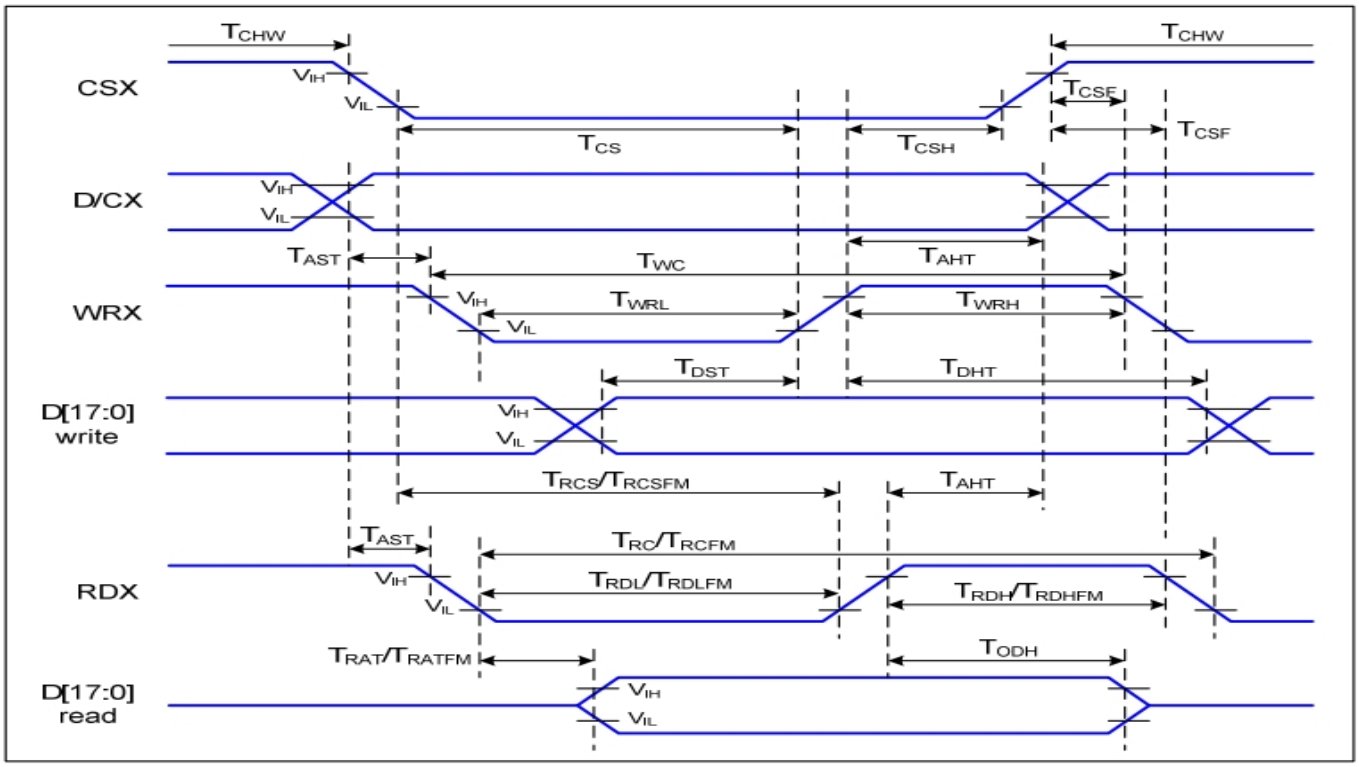


$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

7. AC Characteristics

7.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus



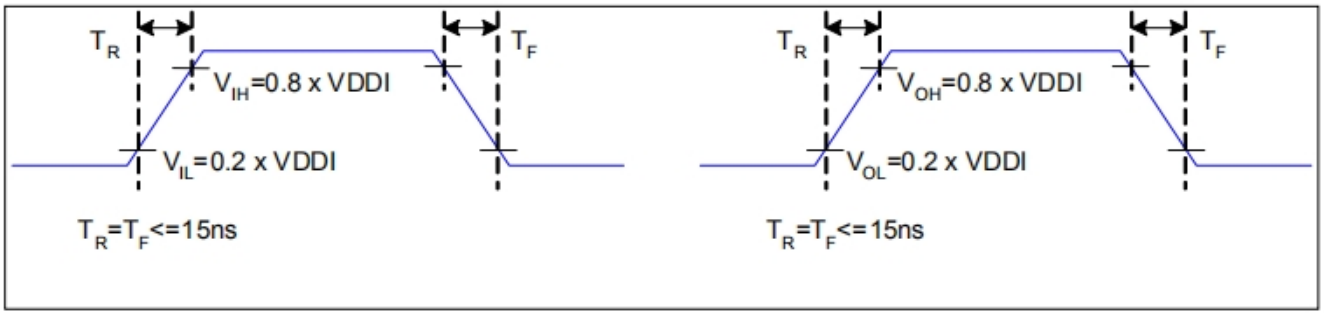
Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	

	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)	-	40	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	
	T_{ODH}	Output disable time	20	80	ns	

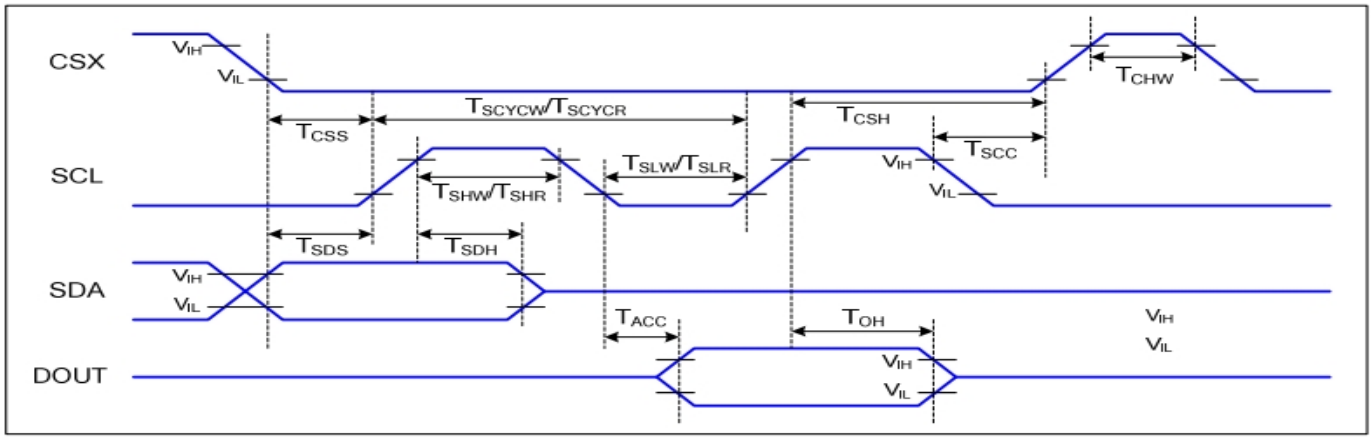
8080 Parallel Interface Characteristics



Rising and Falling Timing for I/O Signal

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

7.2 3-SPI Serial Data Transfer Interface Characteristics:



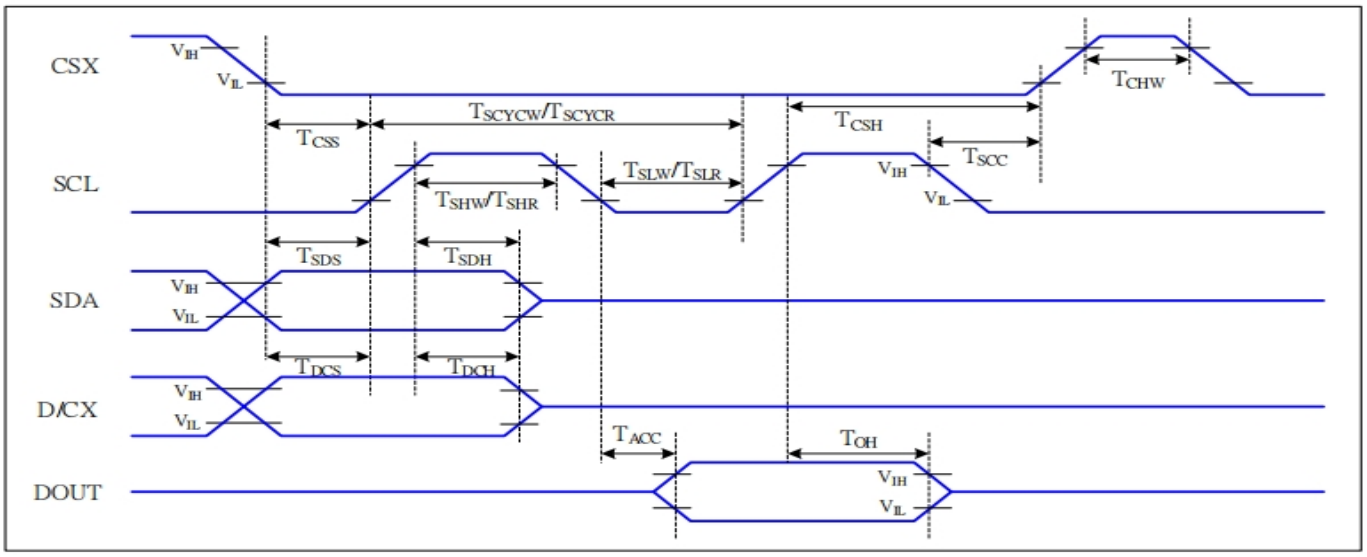
3-SPI Interface Timing Characteristics

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

3-SPI Interface Characteristics

7.3 4-SPI Serial Data Transfer Interface Characteristics:

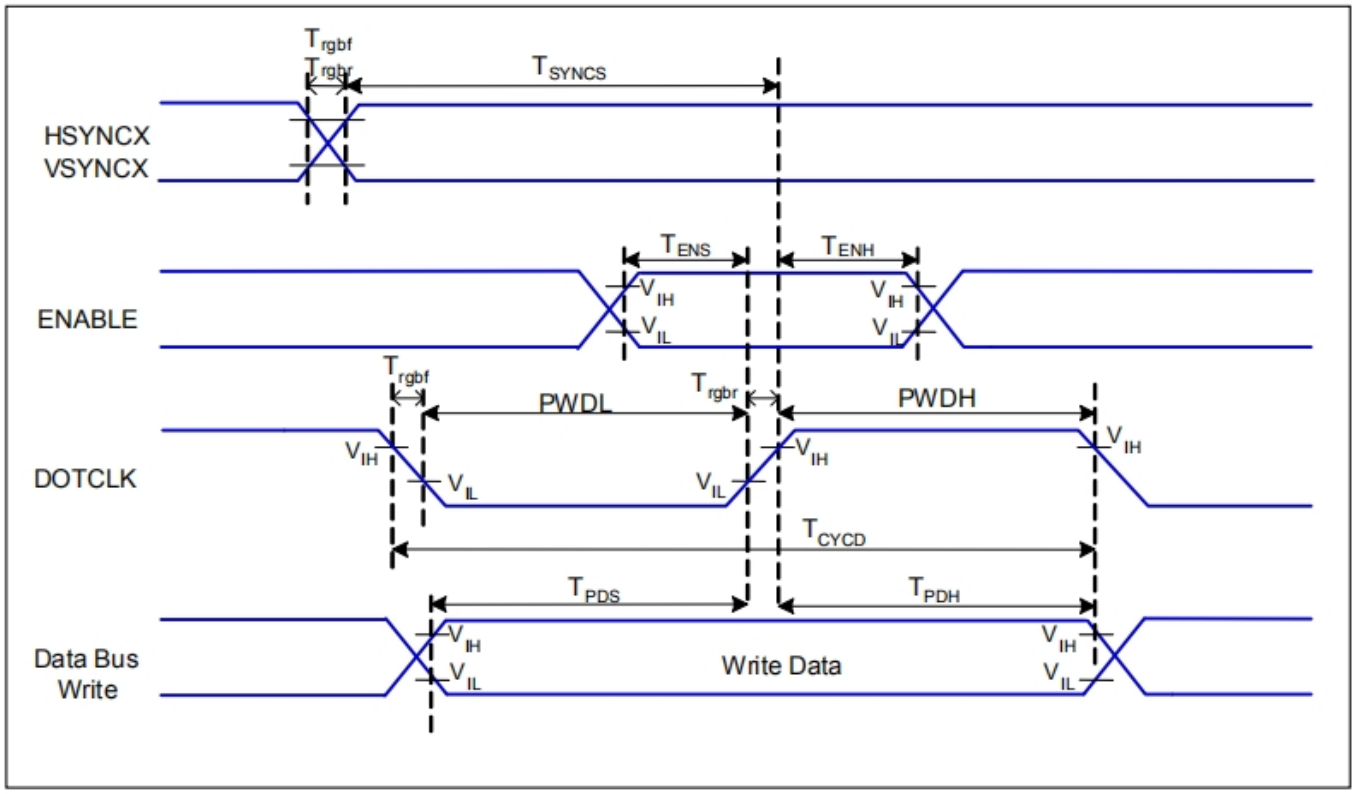


4-SPI Interface Timing Characteristics

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

7.4 RGB Interface Characteristics:

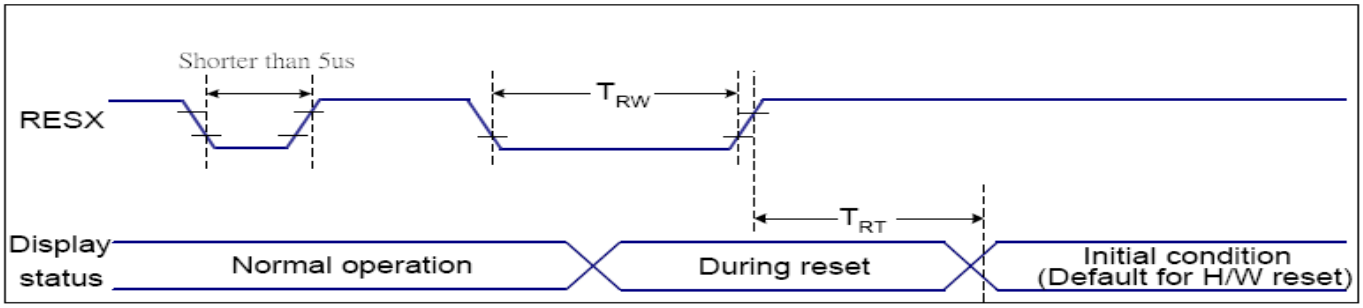


VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	15	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	15	-	ns	
	T_{ENH}	Enable Hold Time	15	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	30	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	30	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	66	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	15	-	ns	
	T_{PDH}	PD Data Hold Time	15	-	ns	

RGB Interface Timing Characteristics

7.5 Reset Timing



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

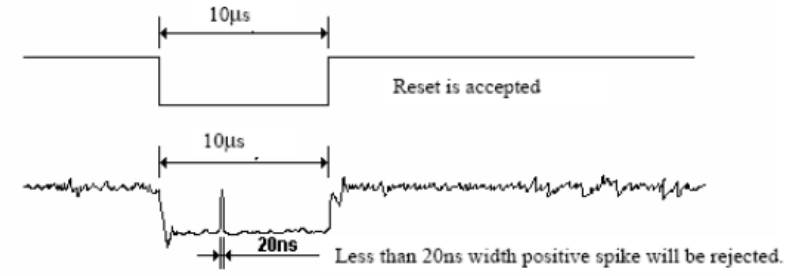
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. CTP Specification

8.1 Electrical Characteristics

8.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	2.7	3.6	V	1
I/O Digital Voltage	VDDIO	1.71	3.6	V	1
Operating Temperature	T_{OP}	-40	+85	°C	-
Storage Temperature	T_{ST}	-55	+150	°C	-

NOTES:

If used beyond the absolute maximum ratings, FT5446U may be permanently damaged. It is strongly recom-manded that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

8.1.2 DC Electrical Characteristics (Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	-	2.8	3.3	3.6	V	-
I/O Digital Supply Voltage	VDDIO	-	1.8	3.3	3.6	V	-
Normal Operation Mode Current Consumption	I_{opr}	VDD=2.8V Ta=25°C MCLK= 17.5Mhz	-	9.8	-	mA	-
Monitor Mode Current Consumption	I_{mon}		-	0.5	-	mA	-
Sleep Mode Current Consumption	I_{slp}		-	75	-	uA	-
Level Input Voltage	V_{IH}	-	$0.7V_{DDIO}$	-	V_{DDIO}	V	-
	V_{IL}	-	-0.3	-	$0.3V_{DDIO}$	V	-
Level Output Voltage	V_{OH}	I_{OH}=3mA	$0.7V_{DDIO}$	-	-	V	-
	V_{OL}	I_{OL}=4.5mA	-	-	$0.3V_{DDIO}$	V	-

8.2 AC Characteristics

AC Characteristics of Oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	Fosc1	MHz	VDD3 = 2.8V; Ta=25℃	62.7	64	65.3	

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 2	Fosc2	MHz	VDD3 = 2.8V; Ta=25℃	50	51.2	52.4	

Table 3-3 AC Characteristics of TX & RX

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
TX acceptable clock	ftx		50	150	400	KHz	
TX output rise time	Ttxr		--	210	--	nS	
TX output fall time	Ttxf		--	210	--	nS	
RX input voltage	Trxi		1.2	--	1.6	V	

8.3 POWER ON / Reset Sequence

Reset should be pulled down to be low before powering on and powering down. I2C shouldn't be used by other devices during Reset time after VDD powering on (Trtp). INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Tpdt is more than 1ms.

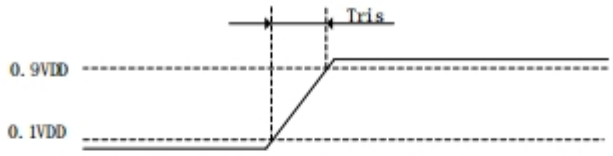


Figure 3-3 Power on time

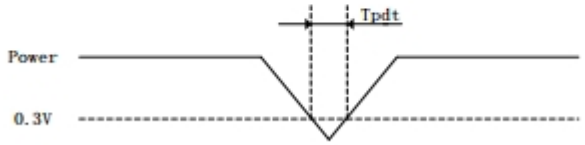


Figure 3-4 Power Cycle requirement

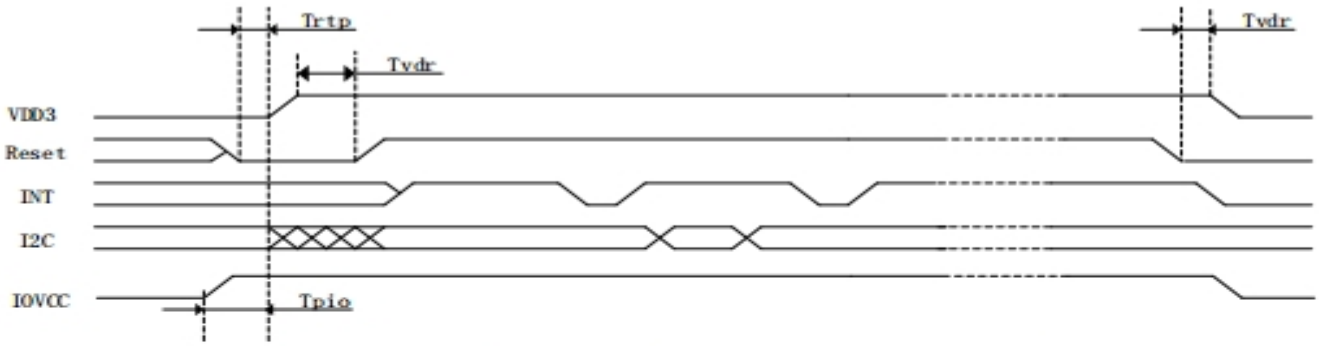


Figure 3-5 Power on Sequence (Dual power)

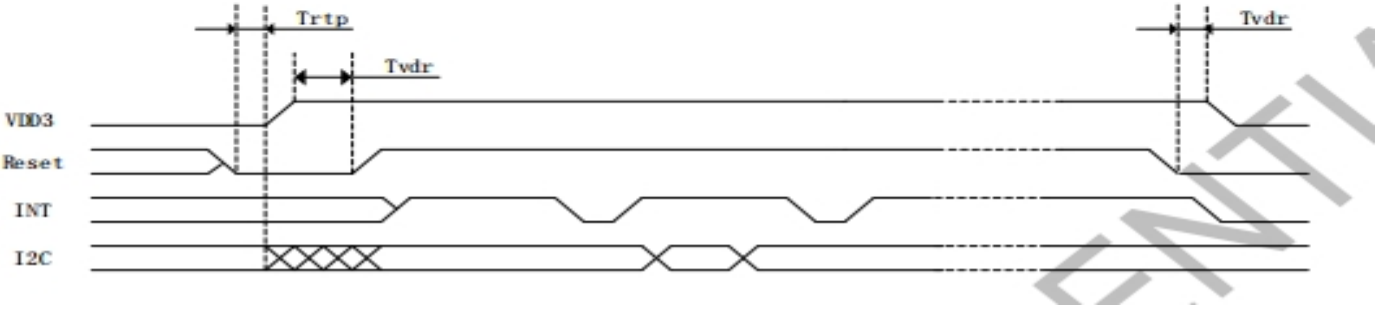


Figure 3-6 Power on Sequence（Single power）

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

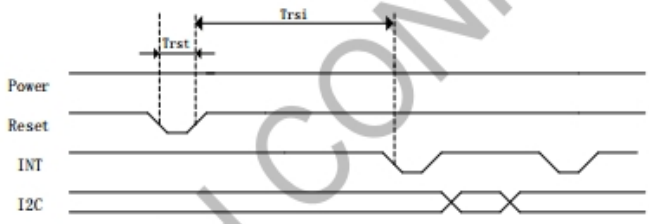


Figure 3-7 Reset Sequence

Table 3-5 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	5	--	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	--	200	ms
Trst	Reset time	1	--	ms
Tpio	Time of IOVCC to be high before powering on	0		ms

8.4 I2C Timing

FT5446U supports the I2C interfaces, which can be used by a host processor or other devices.

The I2C is always configured in the Slave mode. The data transfer format is shown in **Figure 2-4.**

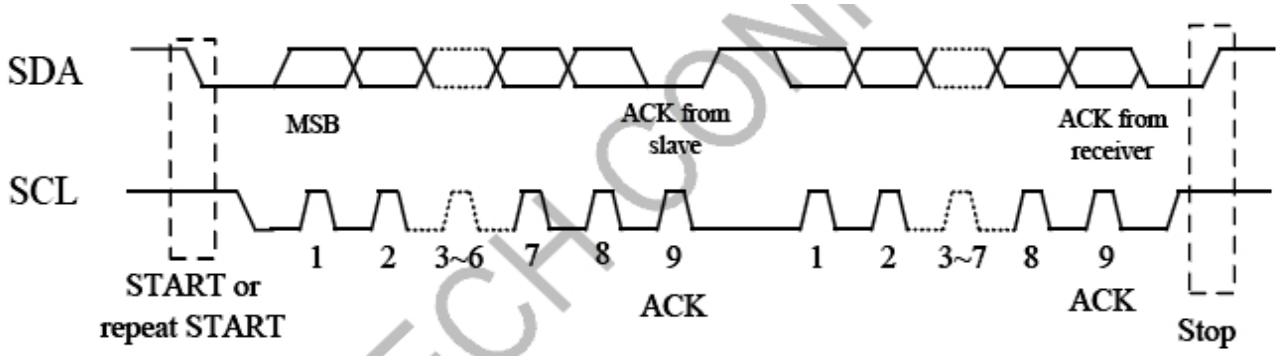


Figure 2-4 I2C Serial Data Transfer Format

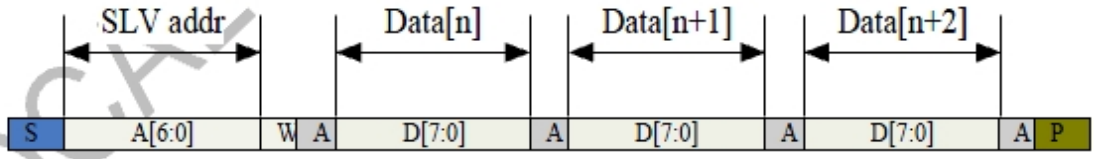


Figure 2-5 I2C master write, slave read

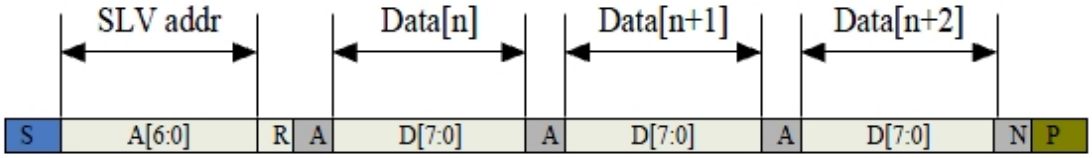


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/ W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK) bit
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	0	400	KHz
Bus free time between a STOP and START condition	1.3		us
Hold time (repeated) START condition	0.6		us
Data setup time	100		ns
Setup time for a repeated START condition	0.6		us
Setup Time for STOP condition	0.6		us

9. LCD Module Out-Going Quality Level

9.1 VISUAL & FUNCTION INSPECTION STANDARD

9.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

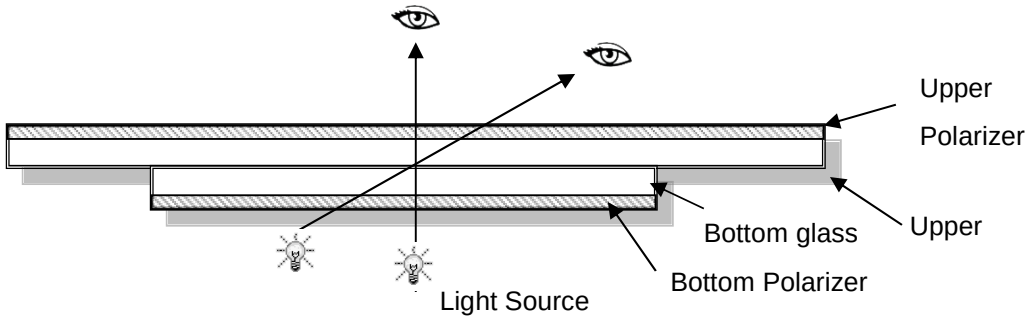
Temperature: 25°C ± 5°C

Humidity: 65% ± 10% RH

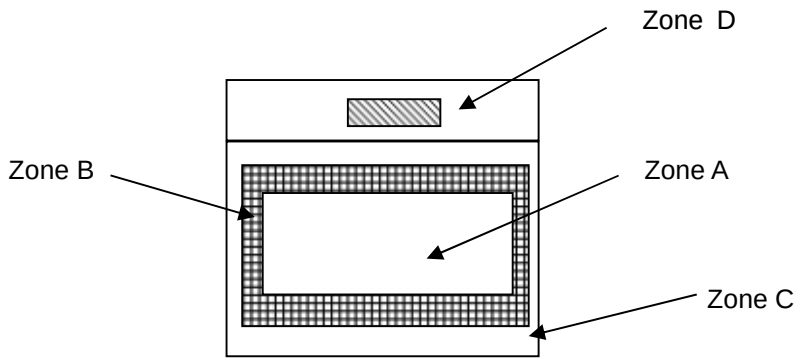
Viewing Angle: Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance: 30-50cm



9.1.2 Definition



Zone A : Effective Viewing Area (Character or Digit can be seen)

Zone B: Viewing Area except Zone A

Zone C: Outside (Zone A+Zone B) which can not be seen after assembly by customer

Zone D: IC Bonding Area

Note: As a general rule, visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

9.1.3 Sampling Plan

According to GB/T 2828-2003; Normal Inspection, Class II

AQL:

Major Defect	Minor Defect
0.65	1.5

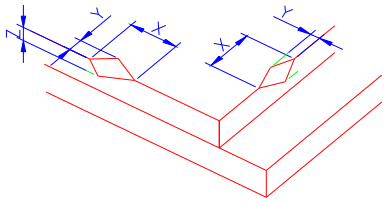
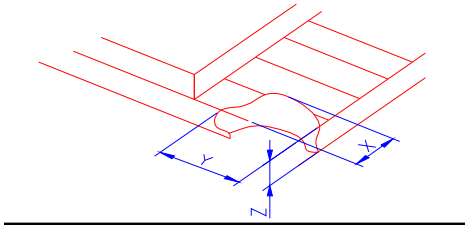
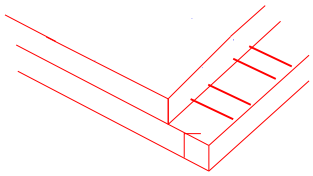
LCD: Liquid Crystal Display, LCM: Liquid Crystal Module, CTP: Capacitive Touch Panel

No	Items to be inspected	Criteria	Classification of Defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc	Major
2	Missing	Missing components and etc	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed,deformation and etc	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot, Dim spot,(Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering, Peeling off is not allowed and etc.	
7	LCD/Polarizer/CTP	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

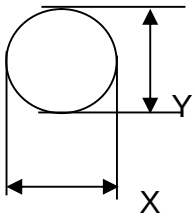
b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

9.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

2.0

Spot defect



Φ=(X+Y)/2

① light dot（ black/white spot , pinhole, stain，etc.）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧10mm)		
0.25<Φ≤0.4	2(distance≧10mm)		
Φ>0.4	0		

② Dim spot（light leakage、dent、dark spot，etc）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧10mm)		
0.25<Φ≤0.4	2(distance≧10mm)		
Φ>0.4	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.5	2(distance≧10mm)		
Φ>0.5	0		

④Polarizer Bubble

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.4	3(distance≧10mm)		
Φ>0.4	0		

3.0 LCD Pixel defect

Pixel bad points

Item	Zone A	Acceptable Qty
Bright dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Dark dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm
Total bright and dark dot		N≤4

Note:

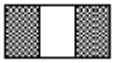
A) Bright dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

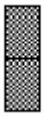
C) 2 dot adjacent = 1 pair = 2 dots

Picture:

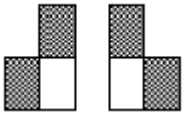
2 dot adjacent



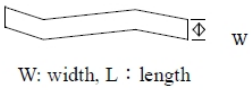
2 dot adjacent



2 dot adjacent (vertical)



2 dot adjacent (slant)

<table>
<tr>
<td>4.0</td>
<td>Line defect (LCD /Polarizer backlight black/white line, scratch, stain)
 

N：Count</td>
<td>
<table>
<tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.05</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L≤4.0</td><td colspan="2">N≤3</td></tr>
<tr><td>0.06<W≤0.08</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>W>0.08</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td>
</tr>
<tr>
<td>5.0</td>
<td>Electronic Components SMT.</td>
<td>Not allow missing parts，solderless connection，cold solder joint，mismatch，The positive and negative polarity opposite</td>
</tr>
<tr>
<td>6.0</td>
<td>Display color& Brightness.</td>
<td>1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td>
</tr>
<tr>
<td>7.0</td>
<td>LCD Mura/Wavin g/
Hot spot</td>
<td>Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.</td>
</tr>
</table>

<table>
<tr>
<td>8.0</td>
<td>CTP Related</td>
<td>CTP Cover sensor accidented black/white spot</td>
<td>
<table>
<tr><th rowspan="2">Size Φ(mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.1<Φ≤0.2</td><td colspan="2">3（distance≧10mm）</td></tr>
<tr><td>0.20<Φ≤0.25</td><td colspan="2">2（distance≧10mm）</td></tr>
<tr><td>Φ > 0.25</td><td colspan="2">0</td></tr>
</table>
</td>
</tr>
</table>

CTP Cover scratch

Width(mm)	Ignore(mm)	Acceptable Qty		
		A	B	C
Φ≤0.05	Ignore	Ignore		
0.05<W≤0.06	L≤4.0	N≤3		
0.06<W≤0.08	L≤3.0	N≤2		
0.08<W	Define as spot defect			

CTP Cover Pinhole/ Lack of ink

Zone / Size (mm)	Acceptable Qty
	C
Φ≤0.1	Ignore
0.1<Φ≤0.25	3(distance≧10mm)
0.25<Φ≤0.3	2(distance≧10mm)
Φ>0.3	0

CTP Bonding bubble/ accidented spot

Size Φ(mm)	Acceptable Qty	
	A	B
Φ≤0.1	Ignore	
0.1<Φ≤0.2	3(distance≧10mm)	
0.2<Φ≤0.25	2(distance≧10mm)	
Φ>0.25	0	

Assembly deflection

beyond the edge of backlight ≤0.2mm

CTP cover broken

X：length

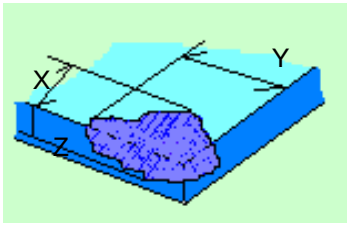
Y：width

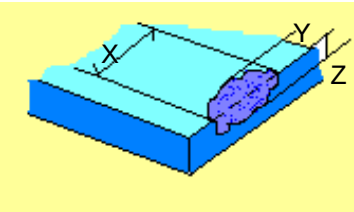
Z：height

X	Y	Z
X≤0.5mm	Y≤0.5mm	Z<cover thickness

*

Circuitry broken is not allowed.



		CTP cover broken X：length Y：width Z：height	X: X≤0.3mm; Y: Y≤0.3mm; Z: Z<cover thickness * Circuitry broken is not allowed.	

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	CTP no function	Not allowed

10. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	+85°C,96h	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1. Air bubble in the LCD; 2. Non-display; 3. Missing segments/line; 4. Glass crack; 5. Current IDD is twice higher than initial value.
Low Temperature Operating	-30°C, 96h	
High Temperature Storage	+85°C, 96h	
Low Temperature Storage	-30°C, 96h	
High Temperature & High Humidity Operating	+60°C, 90% RH, 96h	
Thermal Shock (Non-operation)	-30°C,30 min ↔ 85°C, 30 min, Change time: 5min 20CYC.	
ESD Test	C=150pF, R=330,5points/panel Air:±8kV, 5times; Contact:±6kV, 5 times; (Environment: 15°C~35°C, 30%~60%).	
Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.5mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX)	

Remark:

1. The test samples should be applied to only one test item.
2. Sample size for each test item is 5~10pcs.
3. For Damp Proof Test, Pure water (Resistance > 10MΩ) should be used.
4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
5. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6. The color fading mura of polarizing filter should not care.

11. Cautions and Handling Precautions

11.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the “Power ON” condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

11.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35°C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed.
Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.