Display Elektronik GmbH

DATA SHEET

TFT MODULE

DEM 320240S1 TMH-PW-N

2,3“ TFT

Product Specification ***Version: 1***

24.07.2024

Revision History

Date	Rev. No.	Page	Summary
20.07.2024	0	ALL	FIRST ISSUE
24.07.2024	1	4	UPDATE FORMAT, IC Number, WEIGHT

Contents

* Description

This is a color Active Matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorph ous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver Circuit, Backlight Unit. The resolution of a 2.3" TFT-LCD contains 320x240 pixels, and can display up to 65K/262K colors.

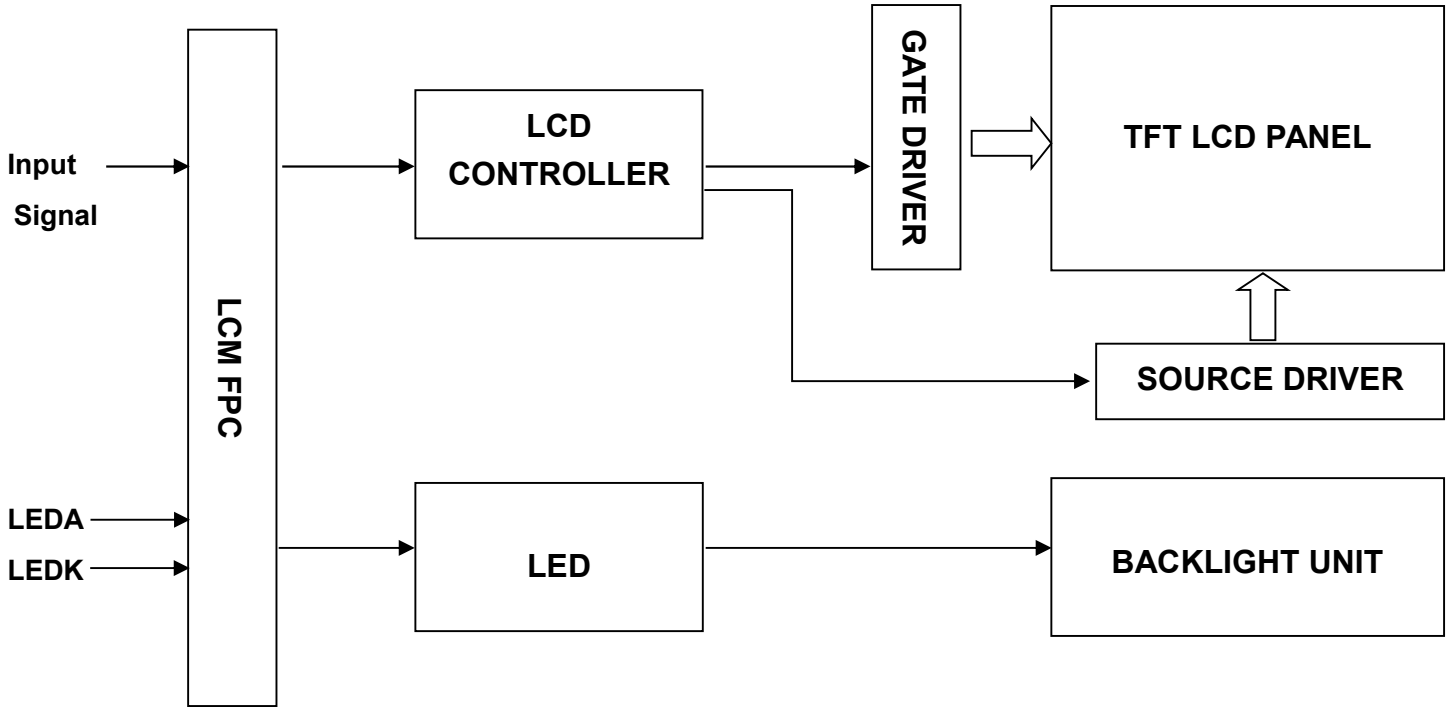
*** Features**

General Information Items	Specification	Unit	Note
	Main Panel		
Display Area(AA)	46.75 x 35.06 (2.3 Inch)	mm	-
Driver Element	TFT Active Matrix	-	-
Display Colors	65k / 262k	colors	-
Number of Pixels	320 x (RGB) x 240	dots	-
TFT Pixel Arrangement	RGB Vertical Stripe	-	-
Pixel Pitch	0.146 x 0.146	mm	-
Viewing Angle	12:00	o'clock	-
TFT Controller IC	ILI9342C (Ilitek)	-	-
Display Interface	8/9/16/18BIT MCU 3/4-Line SPI+16/18BIT RGB 3/4-Line SPI	-	-
Display Mode	TN,Transmissive, Normally White	-	-
Operating Temperature	-20 ~ +70	°C	-
Storage Temperature	-30 ~ +80	°C	-

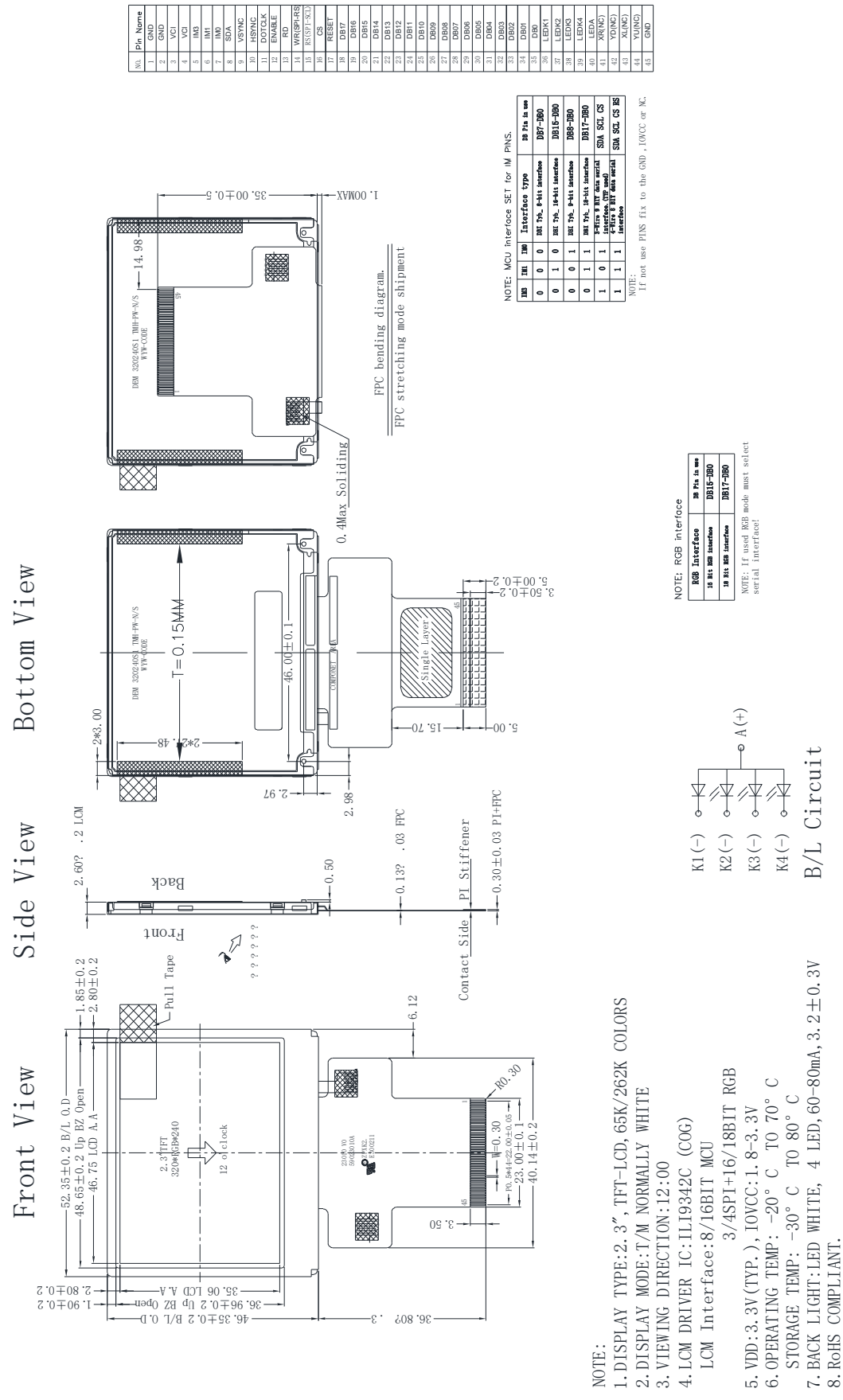
*** Mechanical Information**

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	-	52.35	-	mm	-
	Vertical(V)	-	46.35	-	mm	-
	Depth(D)	-	2.60	-	mm	-
Weight		-	15	-	g	-

1. Block Diagram



2. Outline Dimension



NO.	Pin Name
1	GND
2	GND
3	VCI
4	VCI
5	IM3
6	IM1
7	IM0
8	SDA
9	VSYNC
10	HSYNC
11	DOTCLK
12	ENABLE
13	RD
14	WR(SPI-RS)
15	RS(SPI-SCL)
16	CS
17	RESET
18	DB17
19	DB16
20	DB15
21	DB14
22	DB13
23	DB12
24	DB11
25	DB10
26	DB09
27	DB08
28	DB07
29	DB06
30	DB05
31	DB04
32	DB03
33	DB02
34	DB01
35	DB0
36	LEDK1
37	LEDK2
38	LEDK3
39	LEDK4
40	LEDA
41	XR(NC)
42	YD(NC)
43	XL(NC)
44	YU(NC)
45	GND

NOTE: MCU Interface SET for IM PINS.

IM3	IM1	IM0	Interface type	DB Pin in use
0	0	0	18bit 8-bit interface	DB17-DB10
0	1	0	16bit 16-bit interface	DB15-DB00
0	0	1	16bit 8-bit interface	DB08-DB01
0	1	1	18bit 18-bit interface	DB17-DB00
1	0	1	9-Bits 9 BIT data serial interface (SPI used)	SDA SCL CS
1	1	1	8-Bits 8 BIT data serial interface	SDA SCL CS RS

NOTE:
If not use PINS fix to the GND ,IOVCC or NC.

NOTE: RGB interface

RGB Interface	DB Pin in use
16 Bit RGB interface	DB15-DB00
18 Bit RGB interface	DB17-DB00

NOTE: If used RGB mode must select serial interface!

NOTE:
1. DISPLAY TYPE:2.3",TFT-LCD,65K/262K COLORS
2. DISPLAY MODE:T/M NORMALLY WHITE
3. VIEWING DIRECTION:12:00
4. LCM DRIVER IC:ILI9342C (COG)
   LCM Interface:8/16BIT MCU
   3/4SPI+16/18BIT RGB
5. VDD:3.3V(TYP.),IOVCC:1.8~3.3V
6. OPERATING TEMP: -20° C TO 70° C
   STORAGE TEMP: -30° C TO 80° C
7. BACK LIGHT:LED WHITE, 4 LED,60-80mA,3.2±0.3V
8. RoHS COMPLIANT.

3. Input terminal Pin Assignment

3.1 TFT

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	GND	Ground.	P
3	VCI	Supply voltage(3.3V).	P
4	VCI	Supply voltage(3.3V).	P
5	IM3	MPU Parallel interface bus and serial interface select If use RGB I nterface must select serial interface. Fix this pin at VCI and GND.	I
6	IM1		I
7	IM0		I
8	SDA	The data is applied on the rising edge of the SCL signal. If not us ed,fix this pin at VCI or GND when not in use.	I
9	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
10	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
11	DOTCLK	Dot clock signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
12	ENABLE	Data enable signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
13	RD	Serves as a read signal and MCU read data at the rising edg e. fix this pin at VCI or GND when not in use.	I
14	WR(SPI_RS)	Serves as a write signal and writes data at the rising edge. 4-line system (D/CX): Serves as command or parameter select. fix this pin at VCI or GND when not in use.	I
15	RS(SPI_SCL)	This pin is used to select “Data or Command” in the parallel interface. Whe n D/CX = ’1’, data is selected. When D/CX = ’0’, command is selected. Thi s pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. fix this pin at VCI or GND when not in use.	I
16	CS	Chip select input pin (“Low” enable). fix this pin at VCI or GND when not in use.	I
17	RESET	This signal will reset the device and must be applied to prop erly initialize the chip.	I

18-35	DB17-DB0	18-bit parallel bi-directional data bus for MCU system and RGB interface mode . Fix to GND level when not in use	I/0
36	LEDK1	Cathode pin OF backlight	P
37	LEDK2	Cathode pin OF backlight	P
38	LEDK3	Cathode pin OF backlight	P
39	LEDK4	Cathode pin OF backlight	P
40	LEDA	Anode pin of backlight	P
41	XR(NC)	Touch panel Right Glass Terminal	A/D
42	YD(NC)	Touch panel Bottom Film Terminal	A/D
43	XL(NC)	Touch panel LIFT Glass Terminal	A/D
44	YU(NC)	Touch panel Top Film Terminal	A/D
45	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Optical Specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0	400	500			(1)(2)
Response Time	Rising	T_R		--	4	8	msec	(1)(3)
	Falling	T_F		--	12	24		
Color Gamut		S(%)	-	--	50	--	%	
Color Filter Chromacicity	White	W_X	-	-0.04	0.303	+0.04	-	(1)(4)
		W_Y	-		0.324			
	Red	R_X	-		0.609			
		R_Y	-		0.330			
	Green	G_X	-		0.287			
		G_Y	-		0.527			
	Blue	B_X	-		0.147			
		B_Y	-		0.138			
Viewing Angle	Hor.	$Θ_L$	CR>10	--	70	--	-	(1)(4)
		$Θ_R$		--	70	--		
	Ver.	$Θ_U$		--	70	--		
		$Θ_D$		--	50	--		
Option View Direction		12 o'clock						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding: dark room

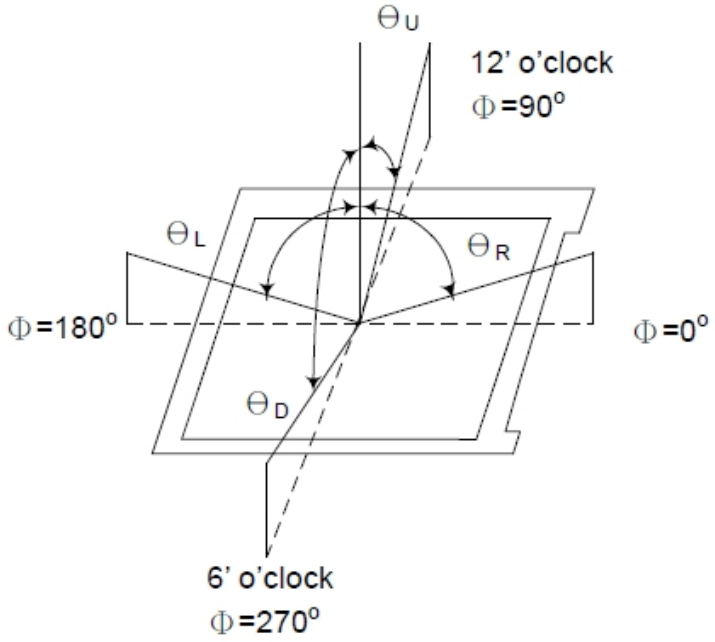
Ambient temperature: 25°C ± 2°C

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

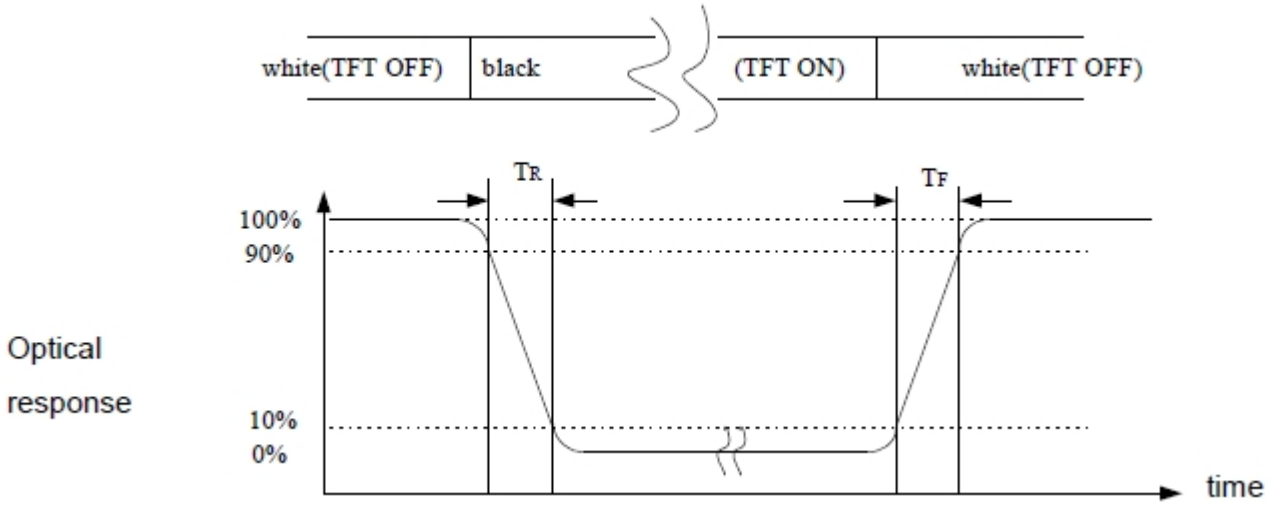
Note (1): Definition of Viewing Angle:



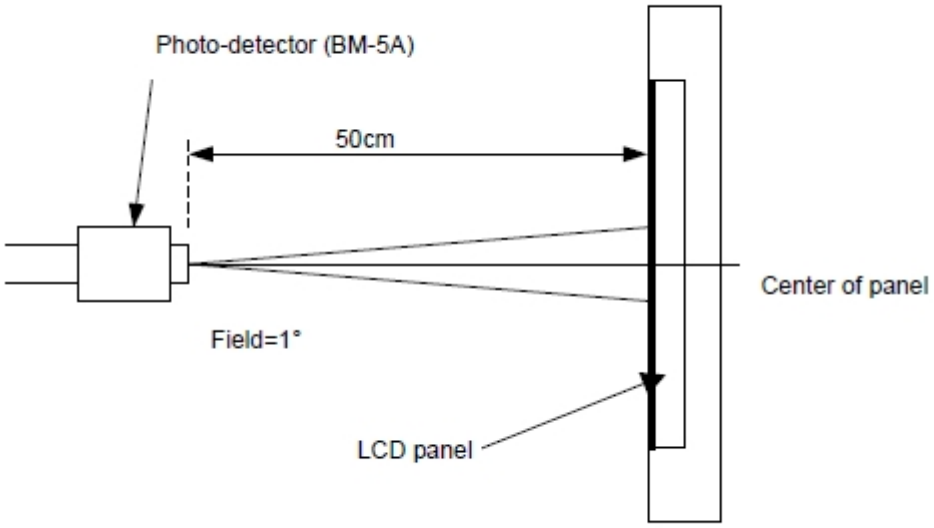
Note (2): Definition of Contrast Ratio (CR): measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time:



Note (4): Definition of optical measurement setup



5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	4.6	V
Digital Interface Supple Voltage	VDDIO	-0.3	VDD	V
Operating Temperature	T_{OP}	-20	+70	°C
Storage Temperature	T_{ST}	-30	+80	°C

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	3.0	3.3	4.2	V	-
Digital Interface Supply Voltage	VDDIO	1.65	3.3	4.2	V	-
Normal Mode Current Consumption	IDD	--	8	16	mA	-
Level Input Voltage	V_{IH}	0.7VDDIO	--	VDDIO	V	-
	V_{IL}	GND	--	0.3VDDIO	V	-
Level Output Voltage	V_{OH}	0.8VDDIO	--	VDDIO	V	-
	V_{OL}	GND	--	0.2VDDIO	V	-

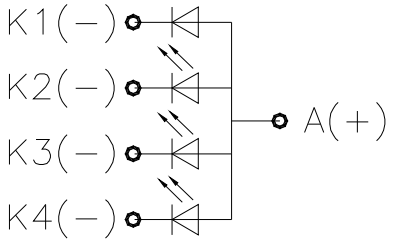
5.3 LED Backlight Characteristics

The Backlight system is edge-lighting type with 4 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	60	80	--	mA	
Forward Voltage	V_F	--	3.2	--	V	
LCM Luminance	L_V	300	350	--	cd/m2	If=80mA
LED Lifetime	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25°C ± 3°C, typical IL value indicated in the above table until the brightness becomes less than 50%.

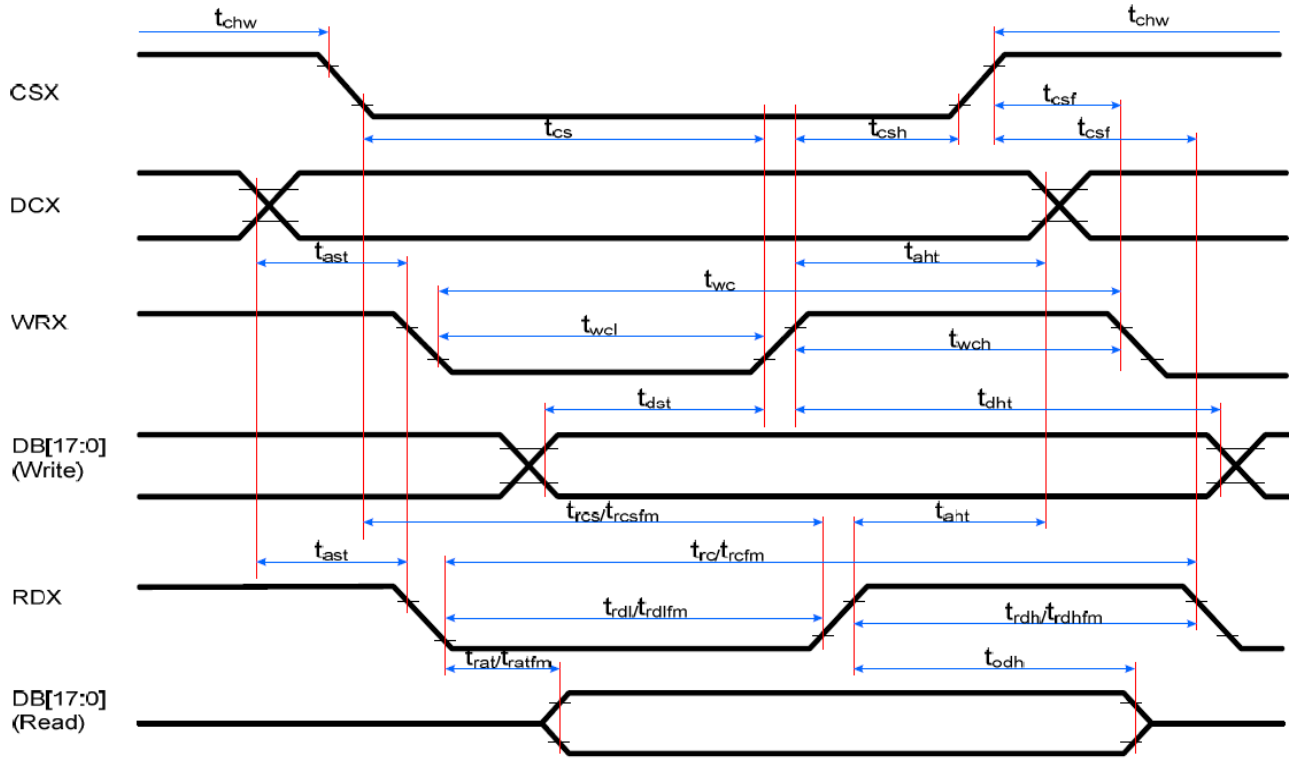
Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=80mA. The LED lifetime could be decreased if operating IL is larger than 80mA. The constant current driving method is suggested.



BLU CIRCUIT DIAGRAM

6. TFT AC Characteristic

6.1 DBI Type B Timing Characteristics



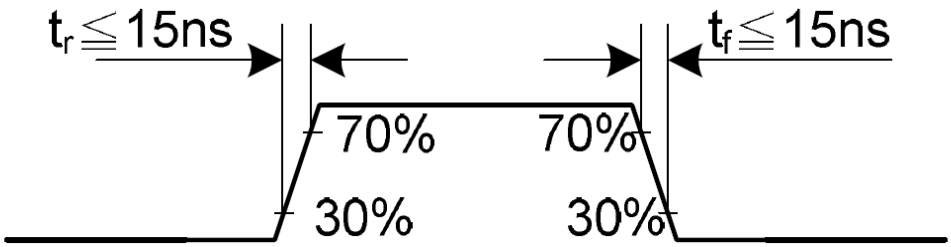
	Symbol	Parameter	Spec		Unit.	Description
			Min.	Max.		
DCX	t_{ast}	Address setup time	0	--	ms	
	t_{hat}	Address hold time (Write/Read)	10	--	us	
CSX	t_{chw}	CSX “H” pulse width	0	--	ns	
	t_{cs}	Chip Select setup time (Write)	15	--	%	
	t_{rcs}	Chip Select setup time (Read ID)	45	--	ns	
	t_{rcsfm}	Chip Select setup time (Read FM)	355	--	ns	
	t_{csf}	Chip Select Wait time (Write/Read)	10	--	ns	
WRX	t_{wc}	Write cycle	66	--	ns	
	t_{wrh}	Write Control pulse H duration	15	--	ns	
	t_{wrl}	Write Control pulse L duration	15	--	ns	
RDX(FM)	t_{rcfm}	Read Cycle (FM)	450	--	ns	When read from Frame Memory
	t_{rdhfm}	Read Control H duration (FM)	90	--	ns	
	t_{rdlfm}	Read Control L duration (FM)	355	--	ns	
RDX(ID)	t_{rc}	Read cycle (ID)	160	--	ns	When read ID data
	t_{rdh}	Read Control pulse H duration	90	--	ns	
	t_{rdl}	Read Control pulse L duration	45	--	ns	
DB[23:0],	t_{dst}	Write data setup time	10	--	ns	For maximum,
	t_{dht}	Write data hold time	10	--	ns	

DB[17:0],	t_{rat}	Read access time	--	40	ns	CL=30pF
DB[15:0],	t_{ratfm}	Read access time	--	340	ns	For minimum,
DB [8:0],	t_{rod}	Read output disable time	20	80	ns	CL=8pF

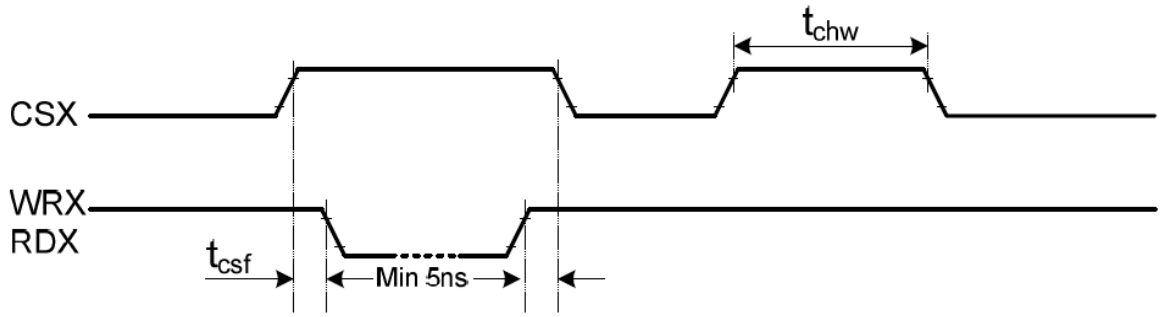
Note: 1. Ta = -30 to 70 °C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V

2. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.

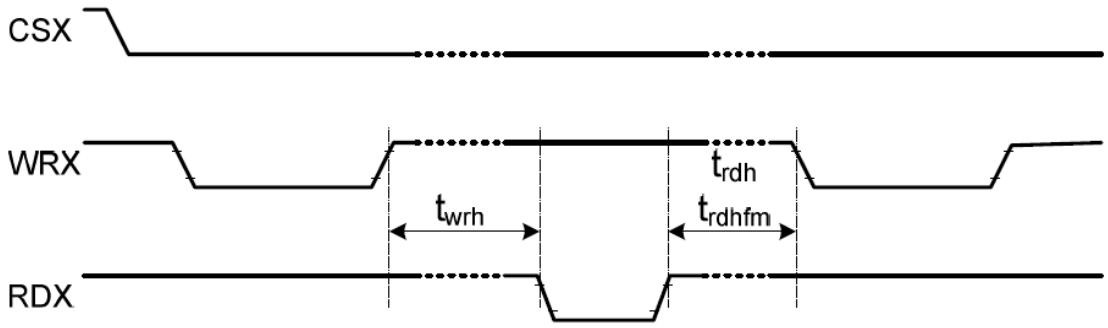
3. Input signal rising time and falling time.:



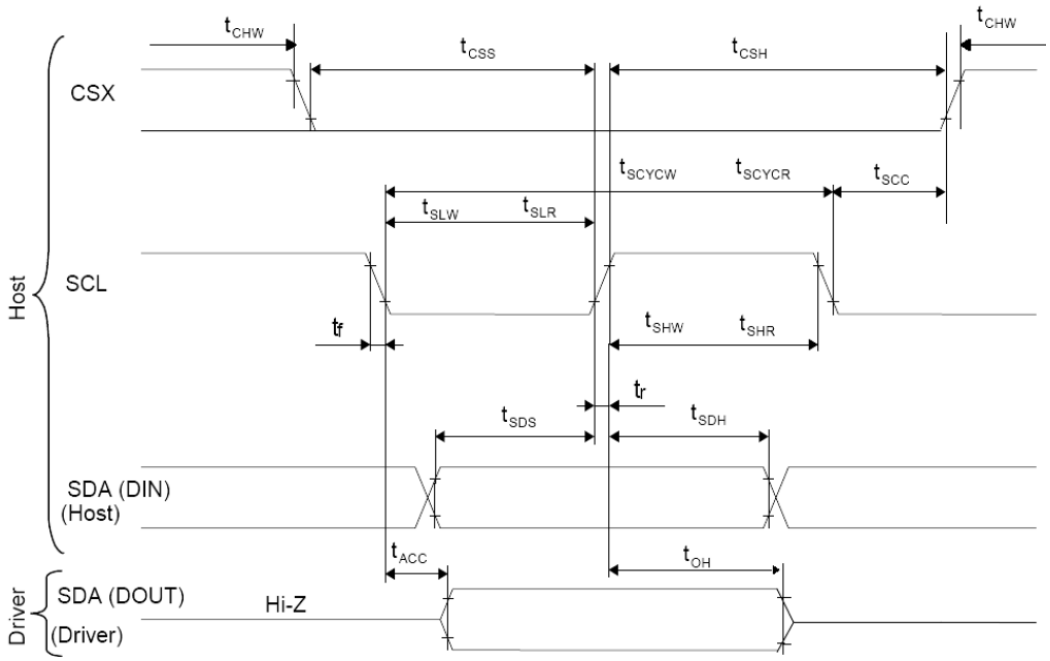
4. The CSX timing:



5. The Write to Read or the Read to Write timing:

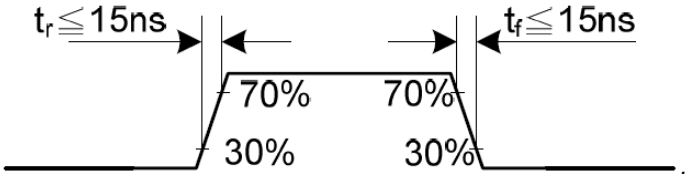


6.2 Display Serial Interface Timing Characteristics (3-line SPI system)

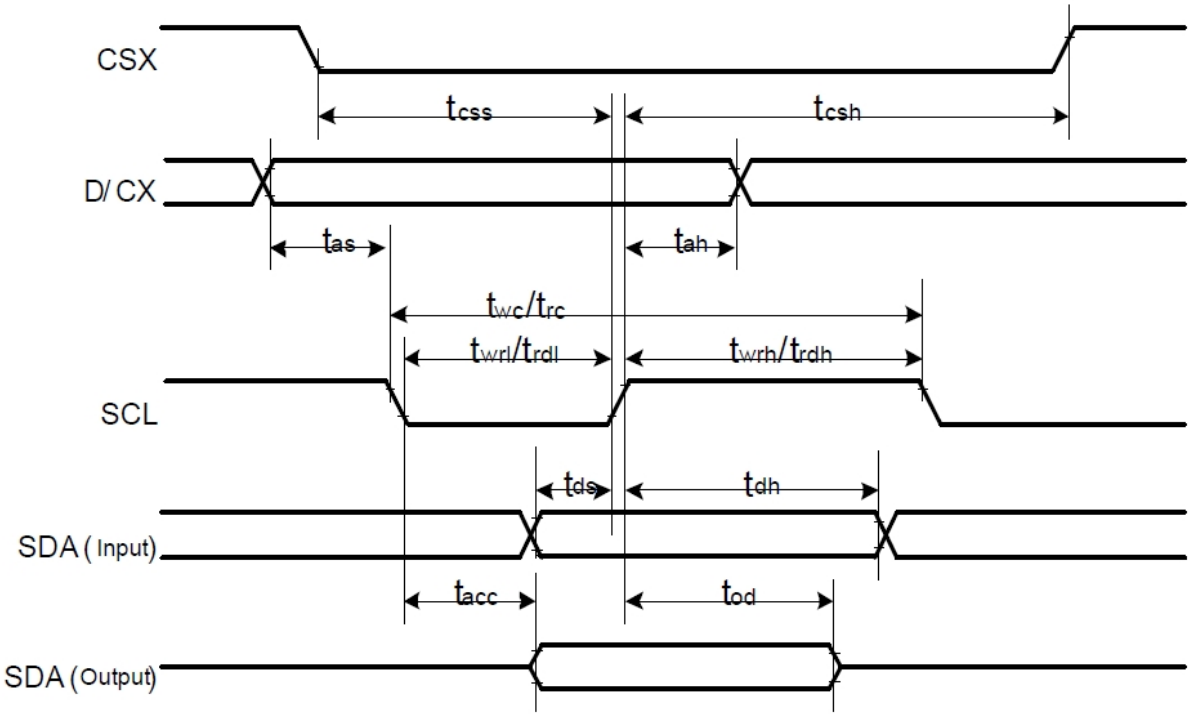


Signal	Symbol	Parameter	Spec		Unit	Description
			Min.	Max	.	
CSX	t_{scc}	SCL-CSX	20	--	ns	
	t_{chw}	CSX H Pulse Width	40	--	ns	
	t_{css}	CSX-SCL Time(write)	30	--	ns	
	t_{csh}		30			
SCL	t_{scycw}	Serial clock cycle (Write)	66	--	ns	
	t_{shw}	SCL H pulse width (Write)	15	--	ns	
	t_{slw}	SCL L pulse width (Write)	15	--	ns	
	t_{scycr}	Serial clock cycle (Read)	150	--	ns	
	t_{shr}	SCL H pulse width (Read)	60	--	ns	
	t_{slr}	SCL L pulse width (Read)	60	--	ns	
SDA (Input)	t_{sds}	Data setup time(Write)	30	--	ns	
	t_{sdh}	Data hold time(Write)	30	--	ns	
SDA/SDO	t_{acc}	Access time(Read)	10	--	ns	
	t_{oh}	Output disable time(Read)	15	50	ns	

NOTES: Ta = -30 to 70 °C, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns



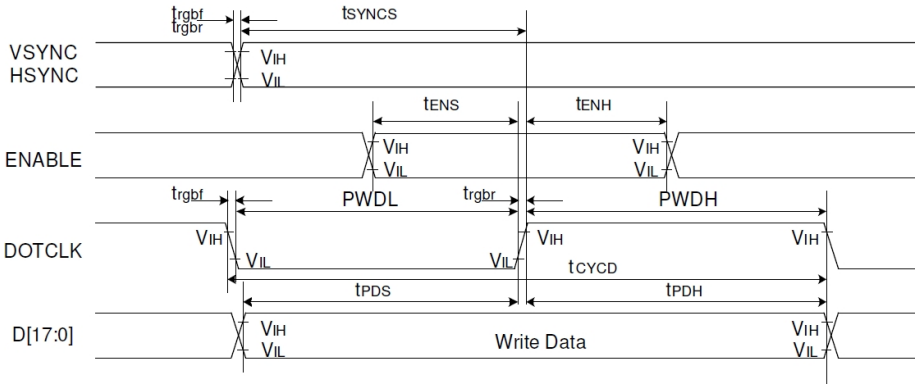
6.3 Display Serial Interface Timing Characteristics (4-line SPI system)



Signal	Symbol	Parameter	Spec		Unit.	Description
			Min.	Max		
CSX	t_{css}	Chip select time (Write)	30	--	ns	
	t_{csh}	Chip select hold time (Read)	30	--	ns	
SCL	t_{wc}	Serial clock cycle (Write)	100	--	ns	
	t_{wrhf}	SCL H pulse width (Write)	35	--	ns	
	t_{wrl}	SCL L pulse width (Write)	35	--	ns	
	t_{rc}	Serial clock cycle (Read)	150	--	ns	
	t_{rdh}	SCL H pulse width (Read)	60	--	ns	
	t_{rdl}	SCL L pulse width (Read)	60	--	ns	
D/CX	t_{as}	D/CX setup time	10	--	ns	
	t_{ah}	D/CX hold time (Write/Read)	10	--	ns	
SDA (Input)	t_{ds}	Read cycle (ID)	10	--	ns	
	t_{dh}	Read Control pulse H duration	10	--	ns	
SDA/SDO (Output)	t_{acc}	Write data setup time	10	50	ns	For maximum CL=30pF
	t_{od}	Write data hold time	15	50	ns	

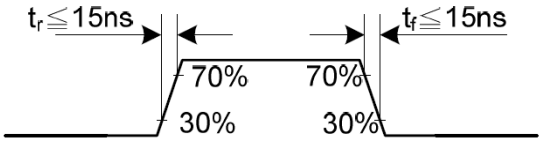
1. *Ta = -30 to 70 °C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V, T = 10+/-0.5ns.*
2. *Does not include signal rising and falling times.*

6.4 Parallel 18/16/6-bit RGB Interface Timing Characteristics

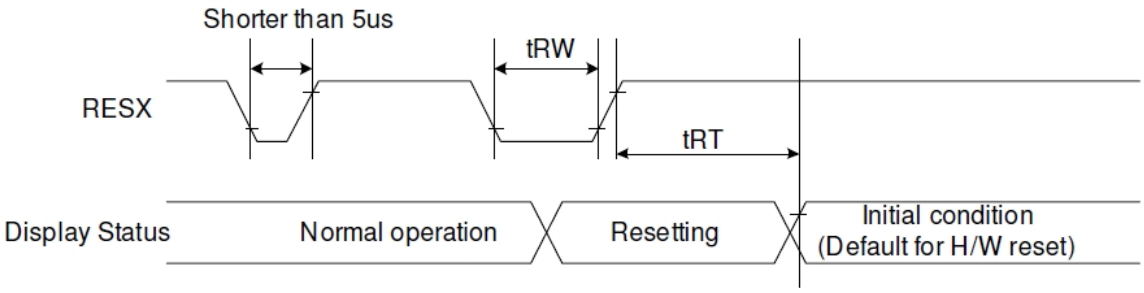


Signal	Symbol	Parameter	Spec		Unit.	Description
			Min.	Max.		
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	--	ns	16-/18-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	--	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	--	ns	
	t_{ENH}	ENABLE hold time	15	--	ns	
DB[23:0]	t_{POS}	Data setup time	15	--	ns	
	t_{POH}	Data hold time	15	--	ns	
DOTCLK	PWDH	DOTCLK high-level period	33	--	ns	
	PWDL	DOTCLK low-level period	33	--	ns	
	t_{CYCD}	DOTCLK cycle time	100	--	ns	
	t_{rgbr},t_{rgbr}	DOTCLK,HSYNC,VSYNC rise/fall time	--	15	ns	
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	--	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	--	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	--	ns	
	t_{ENH}	ENABLE hold time	15	--	ns	
DB[23:0]	t_{POS}	Data setup time	15	--	ns	
	t_{POH}	Data hold time	15	--	ns	
DOTCLK	PWDH	DOTCLK high-level period	25	--	ns	
	PWDL	DOTCLK low-level period	25	--	ns	
	t_{CYCD}	DOTCLK cycle time	50	--	ns	
	t_{rgbr},t_{rgbr}	DOTCLK,HSYNC,VSYNC rise/fall time	--	15	ns	

NOTES: Ta = -30 to 70 °C, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns



6.5 Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

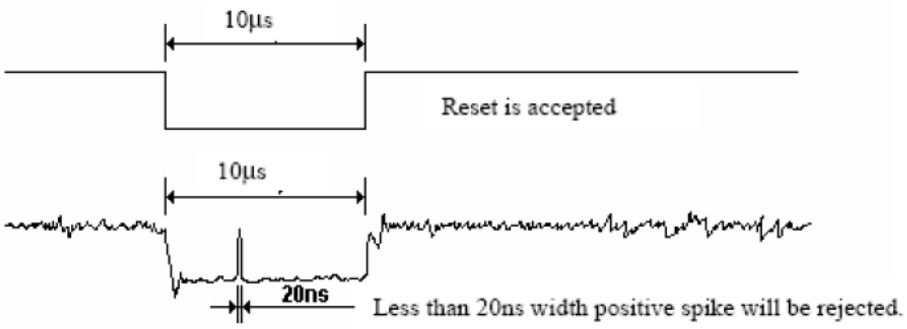
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed und.er the following conditions is recommended.

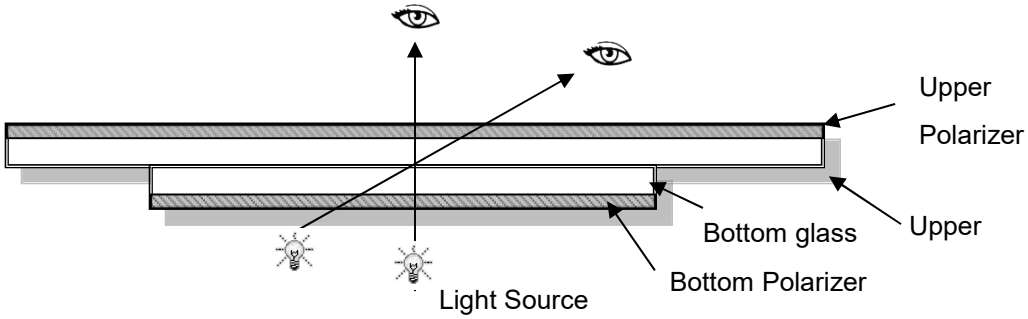
Temperature: 25°C ± 5°C

Humidity: 65% ± 10%RH

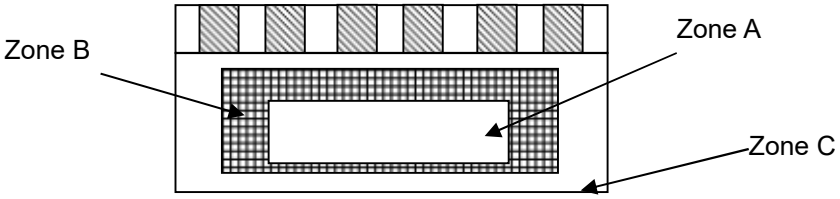
Viewing Angle: Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance: 30-50cm



7.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which cannot be seen after assembly by customer .)

Note:

As a general rule, visual defects in Zone C can be ignored when it doesn't affect product function or appearance after assembly by customer.

7.1.3 Sampling Plan

According to GB/T 2828-2012; Normal inspection, Class Ⅱ

AQL:

Major defect	Minor defect
0.65	1.5

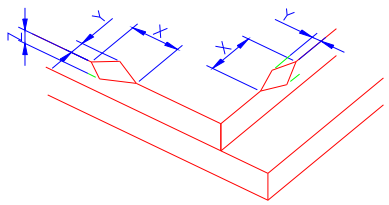
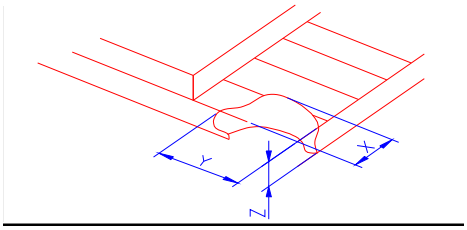
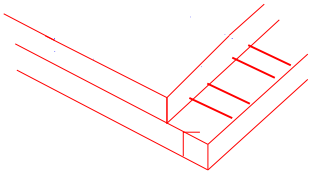
LCD: Liquid Crystal Display, LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc	Major
2	Missing	Missing components and etc	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed,deformation and etc	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot,Dim spot,(Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc.	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

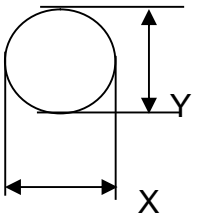
b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

7.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

2.0

Spot defect



Φ=(X+Y)/2

light dot（ black/white spot , pinhole, stain，etc.）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧6mm)		
0.25<Φ≤0.4	2(distance≧6mm)		
Φ>0.4	0		

Dim spot（light leakage、dent、dark spot，etc）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧6mm)		
0.25<Φ≤0.4	2(distance≧6mm)		
Φ>0.4	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.5	2(distance≧6mm)		
Φ>0.5	0		

④Polarizer Bubble

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.4	3(distance≧6mm)		
Φ>0.4	0		

3.0 LCD Pixel defect

Pixel bad points

Item	Zone A	Acceptable Qty
Bright dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Dark dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Distance	Minimum Distance Between Bright dots. Minimum Distance Between dark dots Minimum Distance Between dark and bright dot.	5mm
Total bright and dark dot		N≤4

Note:

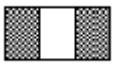
Bright dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

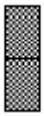
2 dot adjacent = 1 pair = 2 dots

Picture:

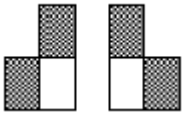
2 dot adjacent



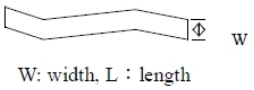
2 dot adjacent



2 dot adjacent (vertical)



2 dot adjacent (slant)

<table>
<tr>
<td>4.0</td>
<td>Line defect (LCD /Polarizer backlight black/white line, scratch, stain)
 

N：Count</td>
<td>
<table>
<tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.03</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.04</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.04<W≤0.05</td><td>L≤2.0</td><td colspan="2">N≤1</td></tr>
<tr><td>W>0.05</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td>
</tr>
<tr>
<td>5.0</td>
<td>Electronic Components SMT.</td>
<td>Not allow missing parts，solderless connection，cold solder joint，mismatch，The positive and negative polarity opposite</td>
</tr>
<tr>
<td>6.0</td>
<td>Display color& Brightness.</td>
<td>Color：Measuring the color coordinates, the measurement standard according to the datasheet or samples.
Brightness：Measuring the brightness of White screen, the measurement standard according to the datasheet or Samples.</td>
</tr>
<tr>
<td>7.0</td>
<td>LCD Mura/Waving/ Hot spot</td>
<td>Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.</td>
</tr>
</table>

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	CTP no function	Not allowed

8. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5. Current IDD is twice higher than initial value.
Low Temperature Operating	-20℃, 96HR	
High Temperature Storage	80℃, 96HR	
Low Temperature Storage	-30℃, 96HR	
High Temperature & High Humidity Operating	+60℃, 90% RH, 96 hours.	
Thermal Shock (Non-operation)	-10℃,30 min ↔ +60℃,30 min, Change time: 5min 20CYC.	
ESD Test	C=150pF, R=330,5points/panel Air: ±8kV, 5times; Contact: ±6kV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz Two hours for each direction of X.Y.Z. (6	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM	

Remark:

1. The test samples should be applied to only one test item.
2. Sample size for each test item is 5~10pcs.
3. For Damp Proof Test, Pure water (Resistance > 10MΩ) should be used.
4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
5. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6. The color fading mura of polarizing filter should not care.

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power. On Sequence & 6.2 Power Off Sequence

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35°C and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.