

DISPLAY Elektronik GmbH

DATA SHEET

LCD MODULE

DEM 240160A FGH-PW

Product Specification

Version: 2

30.09.2020

GENERAL SPECIFICATION

MODULE NO. :

DEM 240160A FGH-PW

CUSTOMER P/N:

VERSION NO.	CHANGE DESCRIPTION	DATE
0	Original Version	02.11.2009
1	Change Production Line	19.01.2018
2	Update Viewing Direction	30.09.2020

PREPARED BY: HZH

DATE: 30.09.2020

APPROVED BY: MH

DATE: 30.09.2020

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1. FUNCTIONS & FEATURES

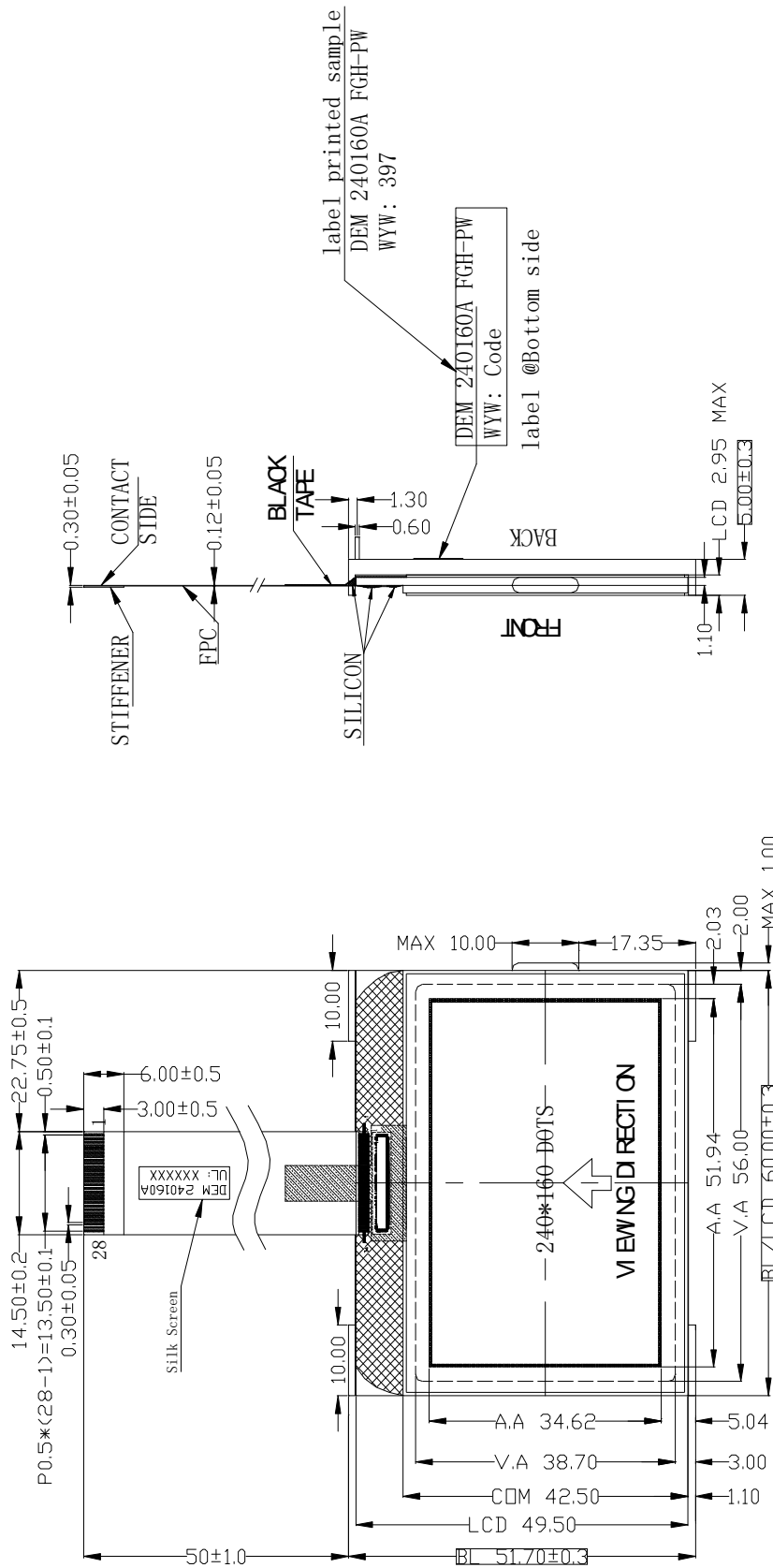
MODULE NAME	LCD TYPE
DEM 240160A FGH-PW	FSTN Transflective Positive Mode

- Viewing Direction : Please refer to drawing and depending on contrast voltage also
- Driving Scheme : 1/160Duty Cycle, 1/12Bias
- Power Supply Voltage : 3.3 Volt (typ.)
- LCD Operation Voltage : 15.6 Volt (typ.)
- Display Format : 240 x 160 Dots

2. MECHANICAL SPECIFICATIONS

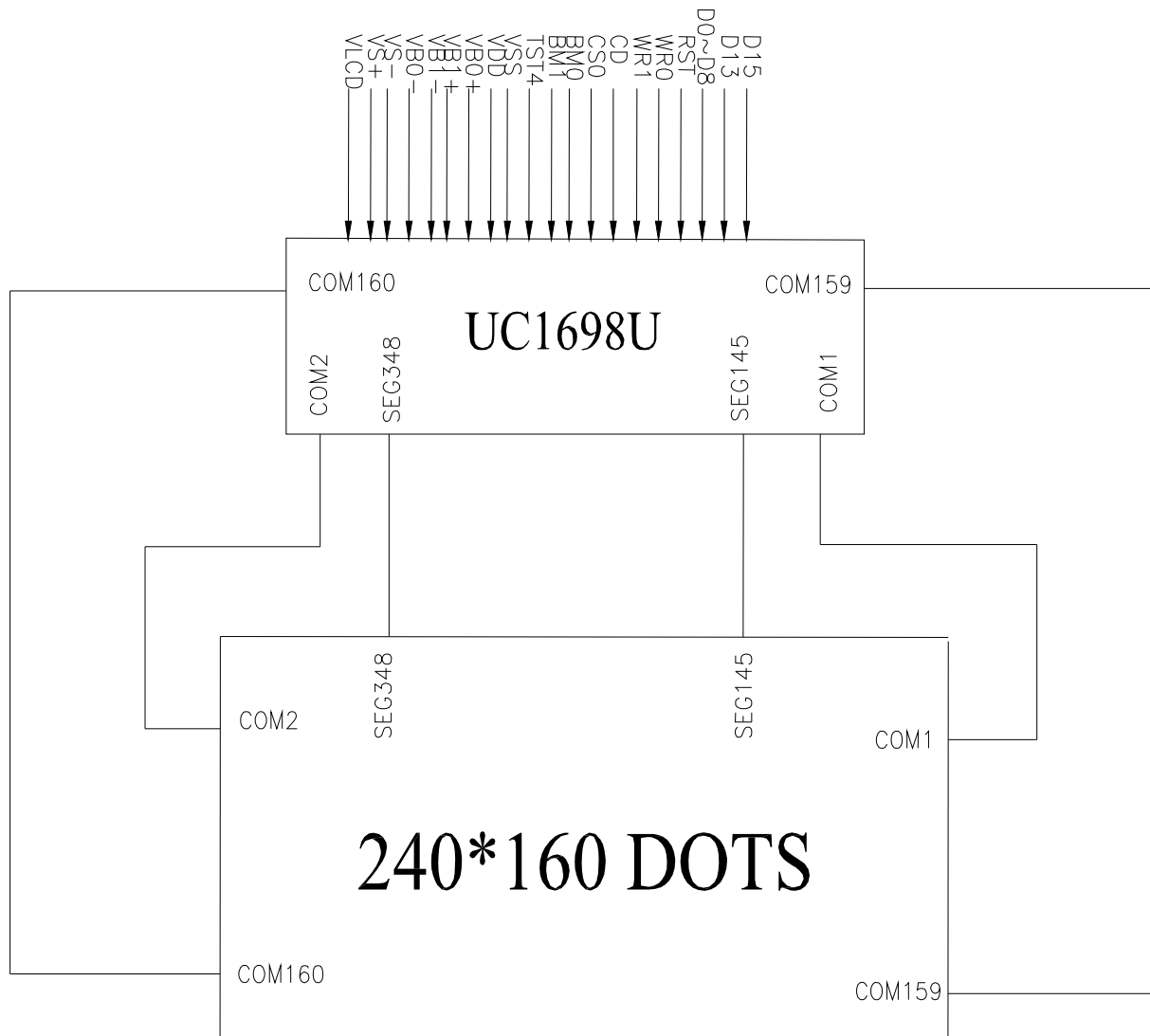
- Module Size : 60.00 x 51.70 x 5.00 mm
- Viewing area : 56.00 x 38.70 mm
- Active Area Size : 51.94 x 34.62 mm

3. EXTERNAL DIMENSIONS



- Remarks:
1. Unmarked tolerance is ± 0.3 ;
 2. All material comply with ROHS;
 3. ...critical dimension;

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

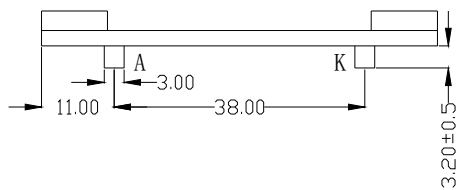
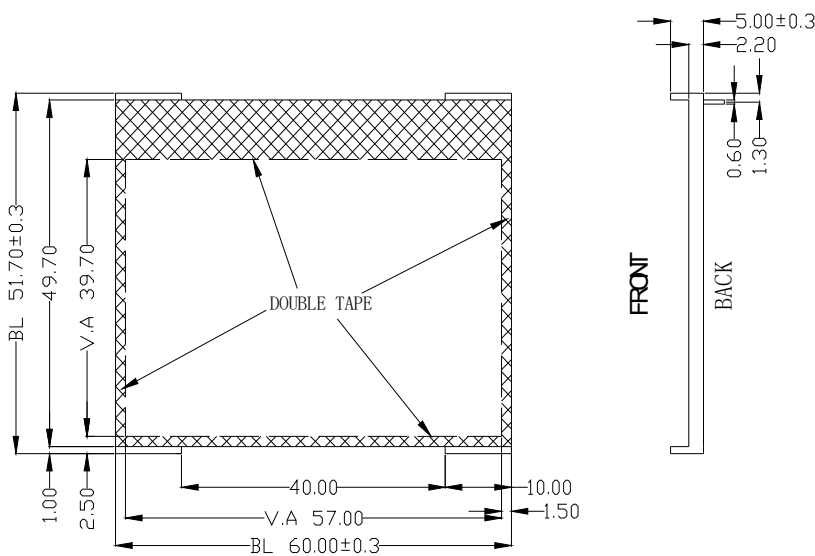
Pin No.	Name	Description																																																																																																																		
1	VLCD	Power supply for LCD voltage																																																																																																																		
2	VS+	LCD SEG driving voltage																																																																																																																		
3	VS-																																																																																																																			
4	VB0-																																																																																																																			
5	VB1-																																																																																																																			
6	VB1+																																																																																																																			
7	VB0+																																																																																																																			
8	VDD	Power supply for logic (+3.3V)																																																																																																																		
9	VSS	Ground																																																																																																																		
10	TST4	TST4 is also used as one of the high voltage power supply for MTP																																																																																																																		
11	BM1	Select Bus Mode																																																																																																																		
12	BM0	BM1:BM0=1:1 6800/16-bit ; BM1:BM0=1:0 8080/16-bit BM1:BM0=0:x 4-wire SPI w/8-bits token																																																																																																																		
13	CS0	Chip select pins																																																																																																																		
14	CD	Select Control data or Display data for read/write operation “L”:Control data “H”: Display data																																																																																																																		
15	WR1	Control the read/write operation of the host interface (When BM1:BM0=0:x,these two pins are not used)																																																																																																																		
16	WR0																																																																																																																			
17	RST	Reset																																																																																																																		
18~26	D0~D8	<table border="1"> <tr> <td colspan="6">Bi-directional bus for parallel host interfaces.</td> </tr> <tr> <td colspan="6">In serial modes, connect DB[0] to SCK, DB[8] to SDA.</td> </tr> <tr> <td></td> <td>16-bit (BM=1x)</td> <td>8-bit (BM=0x ID1=0)</td> <td>8-bit (BM=0x ID1=1)</td> <td>S8/S8uc (BM=00)</td> <td>S9 (BM=01)</td> </tr> <tr> <td>DB0</td> <td>D0</td> <td>D0/D8</td> <td>D0/D8</td> <td>SCK</td> <td>SCK</td> </tr> <tr> <td>DB1</td> <td>D1</td> <td>-</td> <td>D1/D9</td> <td>-</td> <td>-</td> </tr> <tr> <td>DB2</td> <td>D2</td> <td>D1/D9</td> <td>D2/D10</td> <td>-</td> <td>-</td> </tr> <tr> <td>DB3</td> <td>D3</td> <td>-</td> <td>D3/D11</td> <td>-</td> <td>-</td> </tr> <tr> <td>DB4</td> <td>D4</td> <td>D2/D10</td> <td>D4/D12</td> <td>-</td> <td>-</td> </tr> <tr> <td>DB5</td> <td>D5</td> <td>-</td> <td>D5/D13</td> <td>-</td> <td>-</td> </tr> <tr> <td>DB6</td> <td>D6</td> <td>D3/D11</td> <td>D6/D14</td> <td>-</td> <td>-</td> </tr> <tr> <td>DB7</td> <td>D7</td> <td>-</td> <td>D7/D15</td> <td>-</td> <td>-</td> </tr> <tr> <td>DB8</td> <td>D8</td> <td>D4/D12</td> <td>-</td> <td>SDA</td> <td>SDA</td> </tr> <tr> <td>DB9</td> <td>D9</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> </tr> <tr> <td>DB10</td> <td>D10</td> <td>D5/D13</td> <td>-</td> <td>-</td> <td>-</td> </tr> <tr> <td>DB11</td> <td>D11</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> </tr> <tr> <td>DB12</td> <td>D12</td> <td>D6/D14</td> <td>-</td> <td>-</td> <td>-</td> </tr> <tr> <td>DB13</td> <td>D13</td> <td>-</td> <td>-</td> <td>0:S8/1:S8uc</td> <td>0</td> </tr> <tr> <td>DB14</td> <td>D14</td> <td>D7/D15</td> <td>-</td> <td>-</td> <td>-</td> </tr> <tr> <td>DB15</td> <td>D15</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> </table> <p>Always connect unused pins to either V_{SS} or V_{DD}.</p>	Bi-directional bus for parallel host interfaces.						In serial modes, connect DB[0] to SCK, DB[8] to SDA.							16-bit (BM=1x)	8-bit (BM=0x ID1=0)	8-bit (BM=0x ID1=1)	S8/S8uc (BM=00)	S9 (BM=01)	DB0	D0	D0/D8	D0/D8	SCK	SCK	DB1	D1	-	D1/D9	-	-	DB2	D2	D1/D9	D2/D10	-	-	DB3	D3	-	D3/D11	-	-	DB4	D4	D2/D10	D4/D12	-	-	DB5	D5	-	D5/D13	-	-	DB6	D6	D3/D11	D6/D14	-	-	DB7	D7	-	D7/D15	-	-	DB8	D8	D4/D12	-	SDA	SDA	DB9	D9	-	-	-	-	DB10	D10	D5/D13	-	-	-	DB11	D11	-	-	-	-	DB12	D12	D6/D14	-	-	-	DB13	D13	-	-	0:S8/1:S8uc	0	DB14	D14	D7/D15	-	-	-	DB15	D15	0	0	1	1
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DB1	D1	-	D1/D9	-	-																																																																																																															
DB2	D2	D1/D9	D2/D10	-	-																																																																																																															
DB3	D3	-	D3/D11	-	-																																																																																																															
DB4	D4	D2/D10	D4/D12	-	-																																																																																																															
DB5	D5	-	D5/D13	-	-																																																																																																															
DB6	D6	D3/D11	D6/D14	-	-																																																																																																															
DB7	D7	-	D7/D15	-	-																																																																																																															
DB8	D8	D4/D12	-	SDA	SDA																																																																																																															
DB9	D9	-	-	-	-																																																																																																															
DB10	D10	D5/D13	-	-	-																																																																																																															
DB11	D11	-	-	-	-																																																																																																															
DB12	D12	D6/D14	-	-	-																																																																																																															
DB13	D13	-	-	0:S8/1:S8uc	0																																																																																																															
DB14	D14	D7/D15	-	-	-																																																																																																															
DB15	D15	0	0	1	1																																																																																																															
27	D13																																																																																																																			
28	D15																																																																																																																			

6. BACKLIGHT ELECTRICAL/OPTICAL SPECIFICATIONS

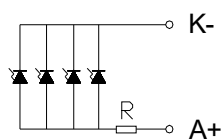
ELECTRICAL–OPTICAL CHARACTERISTICS

Ta=25°C. Unless specified, The Ambient temperature Ta=25°C

Item	Symbol	min.	typ.	max.	Unit	Condition
Forward Voltage	Vf	2.9	3.1	3.3	V	If= 60 mA
Power Dissipation	Pd	–	300	--	mW	If= 60 mA
Luminous Uniformity	D Lv	70			%	MIN/MAX*100%
Luminance	Lv	350	400		cd/m ²	If= 60 mA T=25°C
Color Coordinate	X	0.280		0.320		
	Y	0.280		0.320		



Remarks:
 1.Unmarked tolerance is ±0.3;
 2.All material comply with ROHS;
 3. []...critical dimension;
 4.Color:White



7. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	VDD	-0.3~+4.0	V
LCD Generator Supply Voltage	VDD2	-0.3~+4.0	V
Analog Circuit Supply Voltage	VDD3	-0.3~+4.0	V
Voltage Difference between VDD2/3 and VDD	VDD2/3-VDD	~+1.6	V
LCD Driving Voltage	VLCD	-0.3~+19.8	V
Digital Input Signal	VIN	-0.4~+VDD+0.5	V
Operating Temperature	TOPR	-20~+70	°C
Storage Temperature	TSTR	-30 to +80	°C

8. DC CHARACTERISTICS

(Ta = 0 to+50°C)

ITEM	symbol	STANDARD VALUE			TEST CONDITION	UNIT
		MIN.	TYP.	MAX.		
Power Supply Voltage	VDD	2.7	3.3	3.465	--	V
Operating Voltage	VLCD	15.3	15.6	15.9	--	
Current Consumption	IDD	--	TBD		--	mA

9. AC CHARACTERISTICS

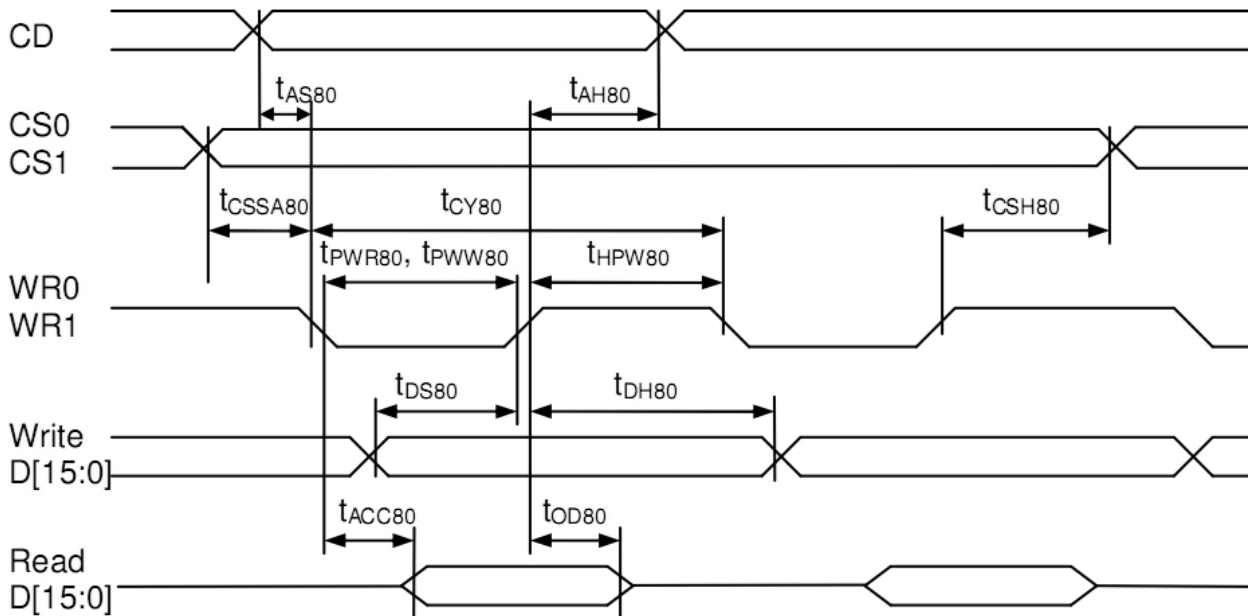


FIGURE 15: Parallel Bus Timing Characteristics (for 8080 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V _{DD} ≤ 3.3V, T _a = -40 to +85°C)				(Read / Write)		
t_{AS80}	CD	Address setup time		0	-	nS
t_{AH80}	CD	Address hold time		10	-	nS
t_{CY80}		System cycle time	16-bit bus 8-bit bus LC[7:6]=10b LC[7:6]=01b	200 / 160 130 / 110 / 120	-	nS
t_{PWR80} / t_{PWW80}	WR1 / WR0	Pulse width	16-bit bus 8-bit bus LC[7:6]=10b LC[7:6]=01b	85 / 65 50 / 40 / 45	-	nS
t_{HPW80}	WR0, WR1	High pulse width	16-bit bus 8-bit bus LC[7:6]=10b LC[7:6]=01b	85 / 65 50 / 40 / 45	-	nS
t_{DS80}	D15~D0	Data setup time		30	-	nS
t_{DH80}	D15~D0	Data hold time		10	-	nS
t_{ACC80}		Read access time	C _L = 100pF	-	80	nS
t_{OD80}		Output disable time		15	30	nS
t_{CSSA80}	CS1/CS0	Chip select setup time		5		nS
t_{CSH80}	CS1/CS0	Chip select hold time		15		nS

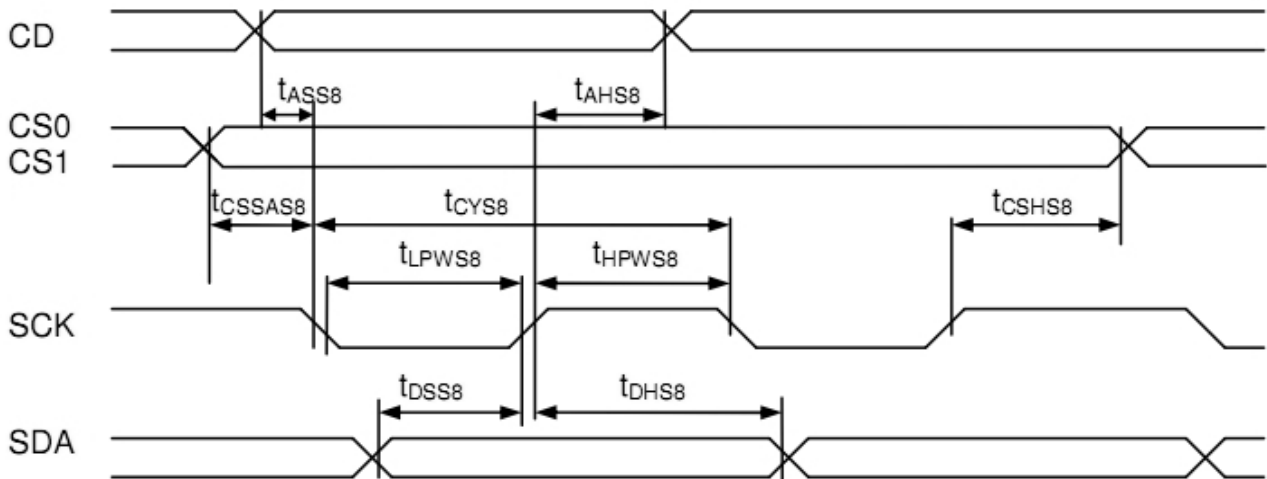


FIGURE 17: Serial Bus Timing Characteristics (for S8/S8uc)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
$(2.5V \leq V_{DD} \leq 3.3V, T_a = -40 \text{ to } +85^\circ\text{C})$				(Read / Write)		
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		10	–	nS
t_{CSSAS8}	CS1/CS0	Chip select setup time		5		nS
t_{CSHS8}				5		
t_{CYS8}	SCK	System cycle time		70	–	nS
t_{LPWS8}		Low pulse width		20	–	nS
t_{HPWS8}		High pulse width		20	–	nS
t_{DSS8}	SDA	Data setup time		15	–	nS
t_{DHS8}		Data hold time		10	–	nS

10. INSTRUCTION

#	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default	
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A	
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A	
3	Get Status & PM	0	1	GE	MX	MY	WA	DE	WS	MD	MS	Get (Status, Ver, PMO, Product Code, PID, MID)	Product Code: 8h	
				Ver						PMO[6:0]				
				Product Code				PID[1:0]		MID[1:0]				
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0	
	Set Column Address MSB	0	0	0	0	0	1	0	#	#	#	Set CA[6:4]	0	
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0	
6	Set Power Control	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b	
7	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0], R = 0 or 1	N/A	
		0	0	#	#	#	#	#	#	#	#			
8	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0	
	Set Scroll Line MSB	0	0	0	1	0	1	#	#	#	#	Set SL[7:4]	0	
9	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0	
	Set Row Address MSB	0	0	0	1	1	1	#	#	#	#	Set RA[7:4]	0	
10	Set V _{POS} Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	40H	
		0	0	#	#	#	#	#	#	#	#			
11	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[8]	0	
12	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b	
13	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set (FLT, FLB)	0	
		0	0	#	#	#	#	#	#	#	#			
14	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LO[4:3]	10b	
15	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0	
16	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0	
17	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b	
18	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	0	
19	Set N-Line Inversion	0	0	1	1	0	0	1	0	0	0	Set NIV[4:0]	1DH	
20	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0 (BGR)	
21	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b	
22	Set OOM Scan Function	0	0	1	1	0	1	1	#	#	#	Set CSF[2:0]	000b	
23	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A	
24	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A	
25	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A	
		0	0	#	#	#	#	#	#	#	#			
26	Set LOD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 12	
27	Set OOM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	159	
		0	0	-	#	#	#	#	#	#	#			
28	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0	
		0	0	-	#	#	#	#	#	#	#			
29	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	159	
		0	0	-	#	#	#	#	#	#	#			
30	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Shared with MTP commands	Set WPC0	0
		0	0	-	#	#	#	#	#	#	#			
31	Set Window Program Starting Row Address	0	0	1	1	1	1	0	1	0	1	Shared with MTP commands	Set WPP0	0
		0	0	#	#	#	#	#	#	#	#			
32	Set Window Program Ending Column Address	0	0	1	1	1	1	0	1	1	0	Shared with MTP commands	Set WPC1	127
		0	0	-	#	#	#	#	#	#	#			
33	Set Window Program Ending Row Address	0	0	1	1	1	1	0	1	1	1	Shared with MTP commands	Set WPP1	159
		0	0	#	#	#	#	#	#	#	#			
34	Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC[3]	0: Inalde	
35	Set MTP Operation control	0	0	1	0	1	1	1	0	0	0	Set MTPC[4:0]	10H	
		0	0	-	-	-	#	#	#	#	#			

#	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default	
36	Set MTP Write Mask	0 0 0	0 0 0	1 - -	0 # -	1 # -	1 # -	1 # -	0 # -	0 # -	1 # #	Set MTPM[6:0] MTPM1[1:0]	0	
37	Set V _{MTP1} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with Window Program commands	Set MTP1	N/A
38	Set V _{MTP2} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set MTP2	N/A
39	Set MTP Write Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #		Set MTP3	N/A
40	Set MTP Read Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set MTP4	N/A

NOTE:

- All other bit patterns other than commands listed above may result in undefined behavior.
- The interpretation of commands (36)~(40) depends on the setting of register MTPC[3].
 - Commands (37)~(40) are shared with commands (30)~(33). These two sets of commands share exactly the same code and control registers. When MTPC[3]=0, they are interpreted as Window Program commands and registers. When MTPC[3]=1, they function as MTP Control commands and registers.
- After MTP ERASE or PROGRAM operation, before resuming normal operation, please always
 - a) Remove TST4 power source,
 - b) Do a full V_{DD} ON-OFF-ON cycle.
- Under 16-bit bus mode and CD=0, D[15:8] is ignored and only D[7:0] is used. As a result, the bus cycles for commands under 16-bit bus and 8-bit bus are the same, and double-byte commands still need two bus cycles under 16-bit bus mode.

Example:

8-bit bus mode:

Set PL[1:0] = 2'b11 : D[7:0] = 0010 1011

Set PM[7:0] = 8'h8b : 1st D[7:0] = 1000 0001

2nd D[7:0] = 1000 1011

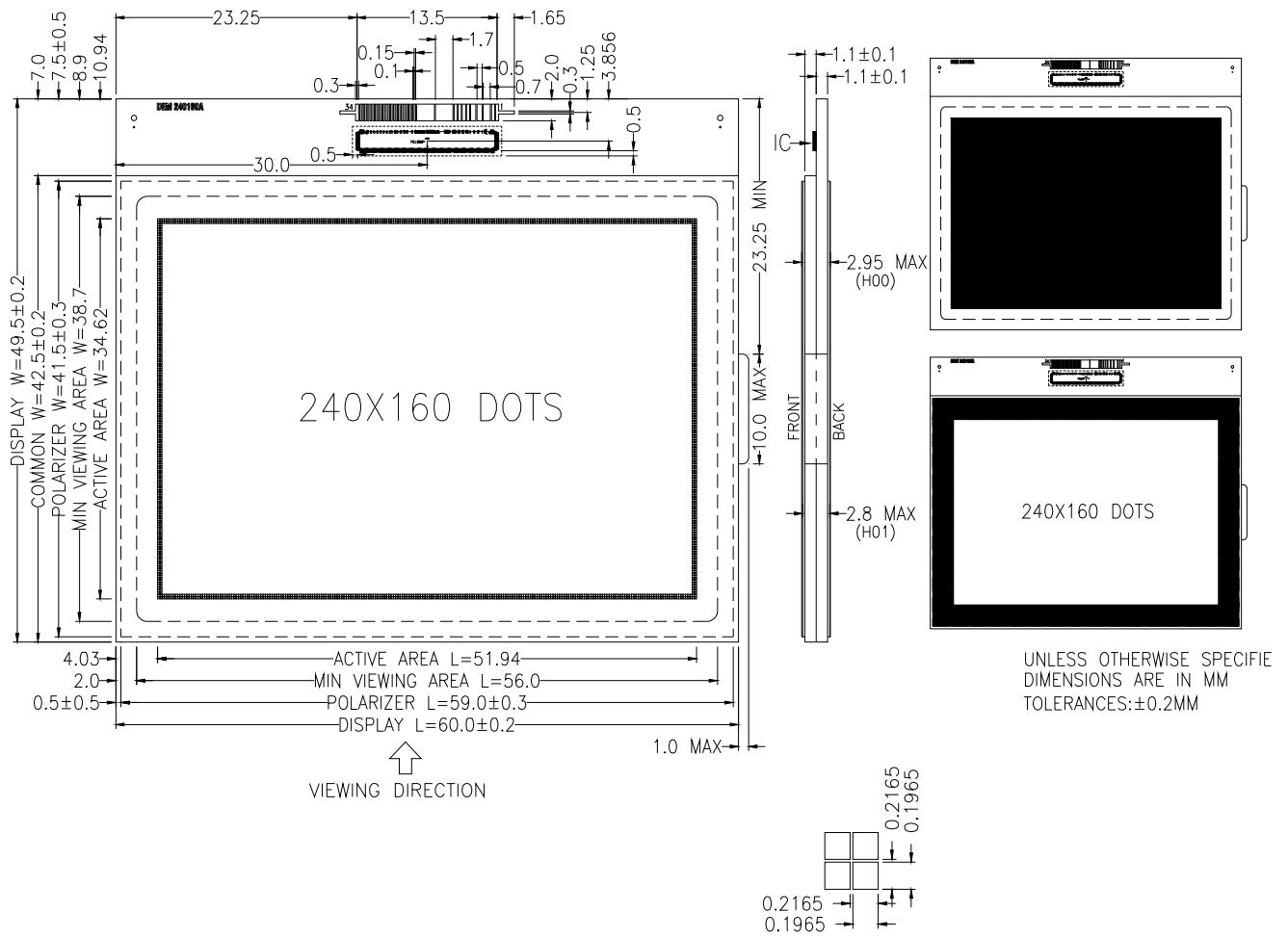
16-bit bus mode:

Set PL[1:0] = 2'b11: D[15:0] = 0000 0000 0010 1011

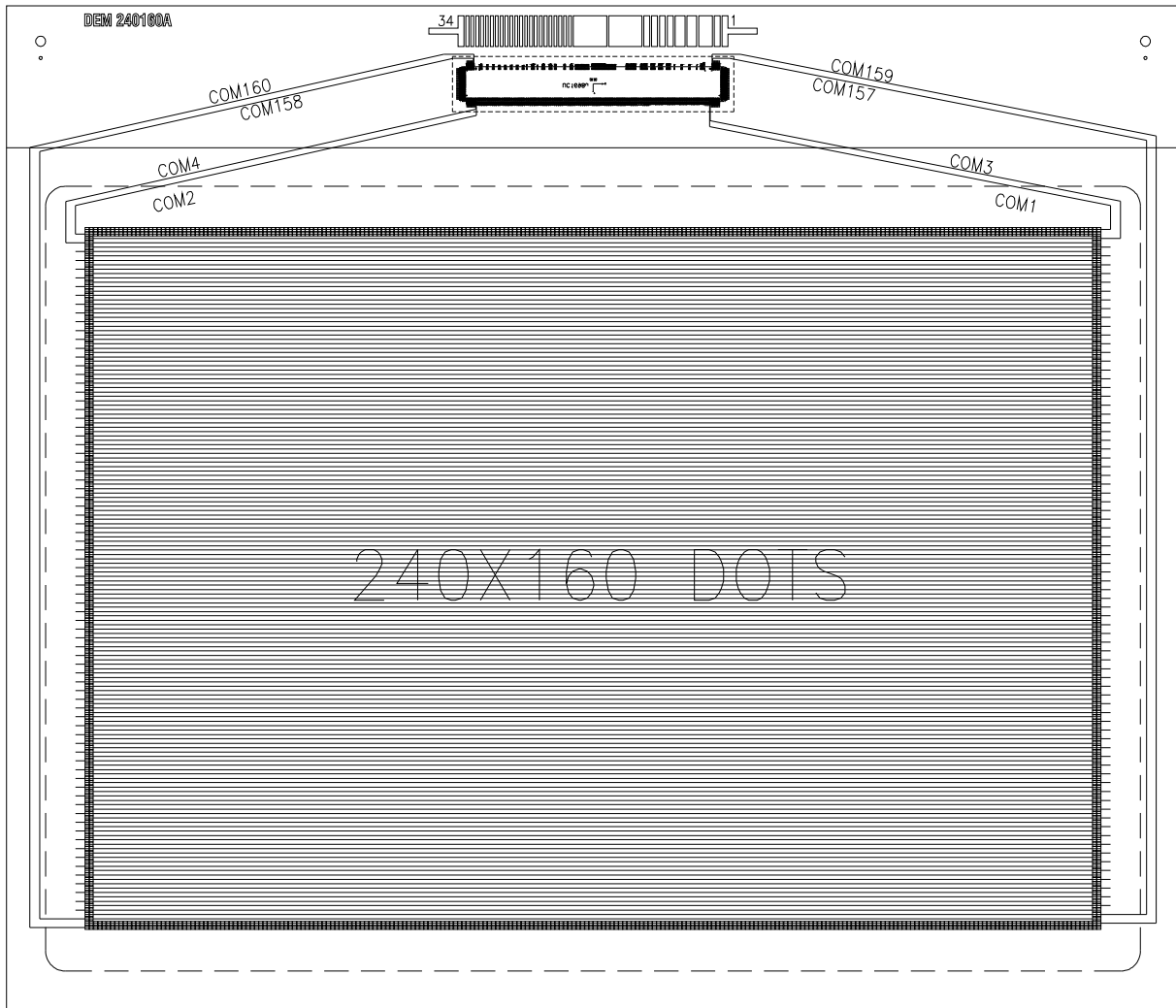
Set PM[7:0] = 8'h8b: 1st D[15:0] = 0000 0000 1000 0001

2nd D[15:0] = 0000 0000 1000 1011

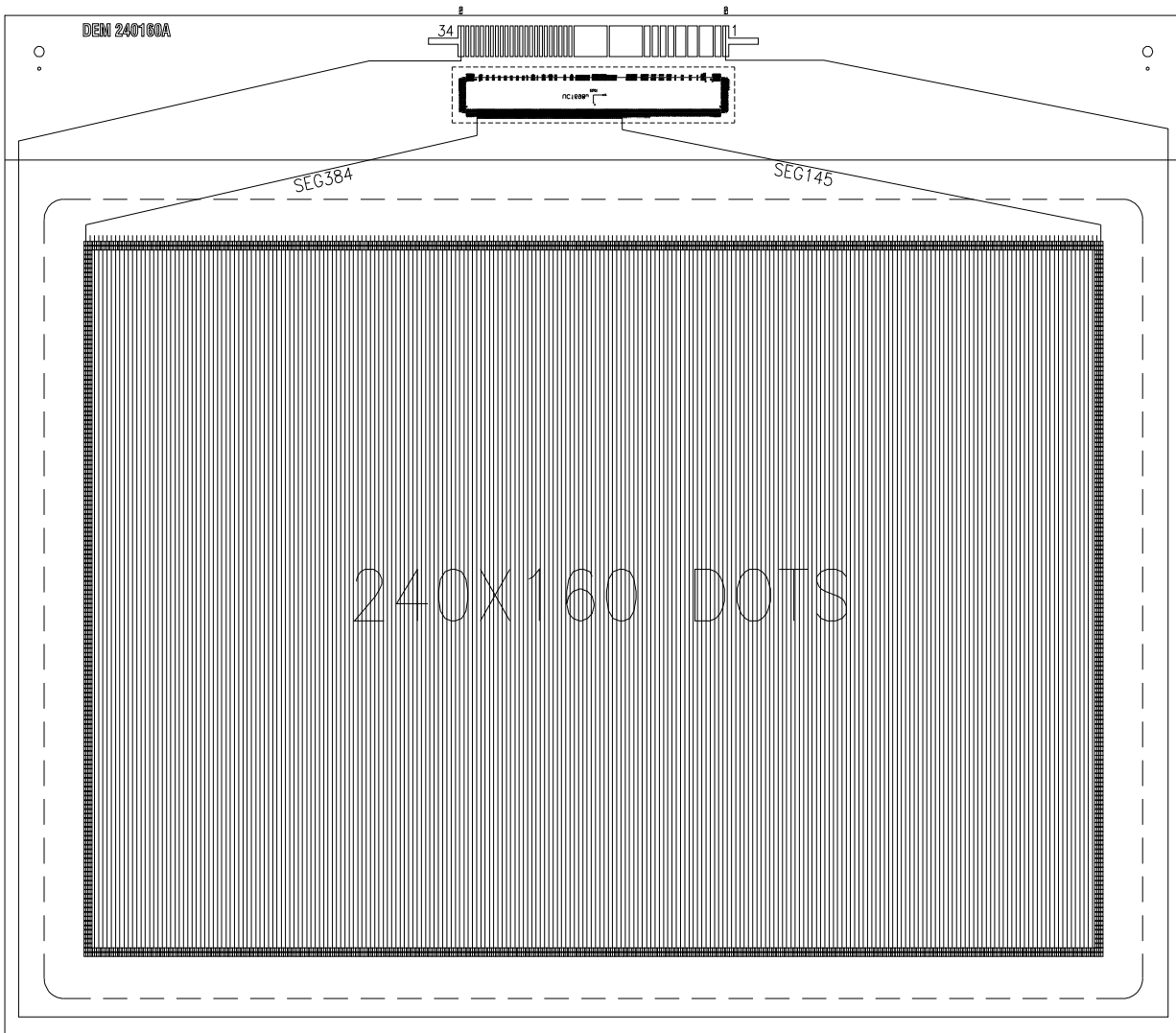
11. LCD ARTWORK



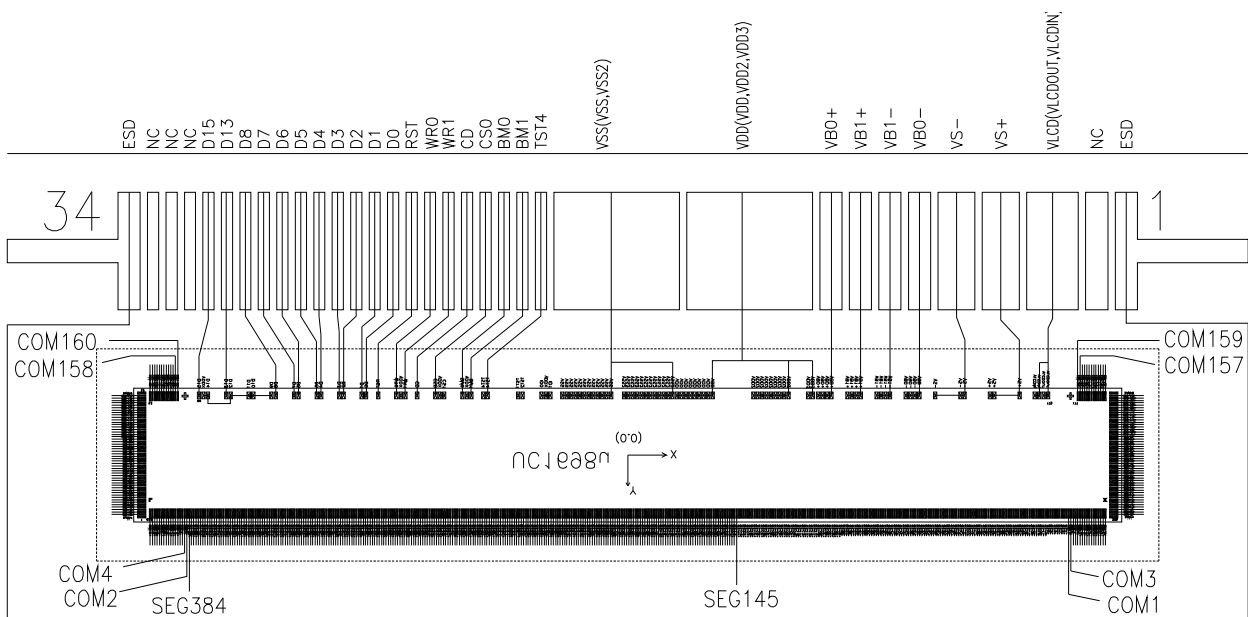
12. COMMON LAYOUT



13. SEGMENT LAYOUT



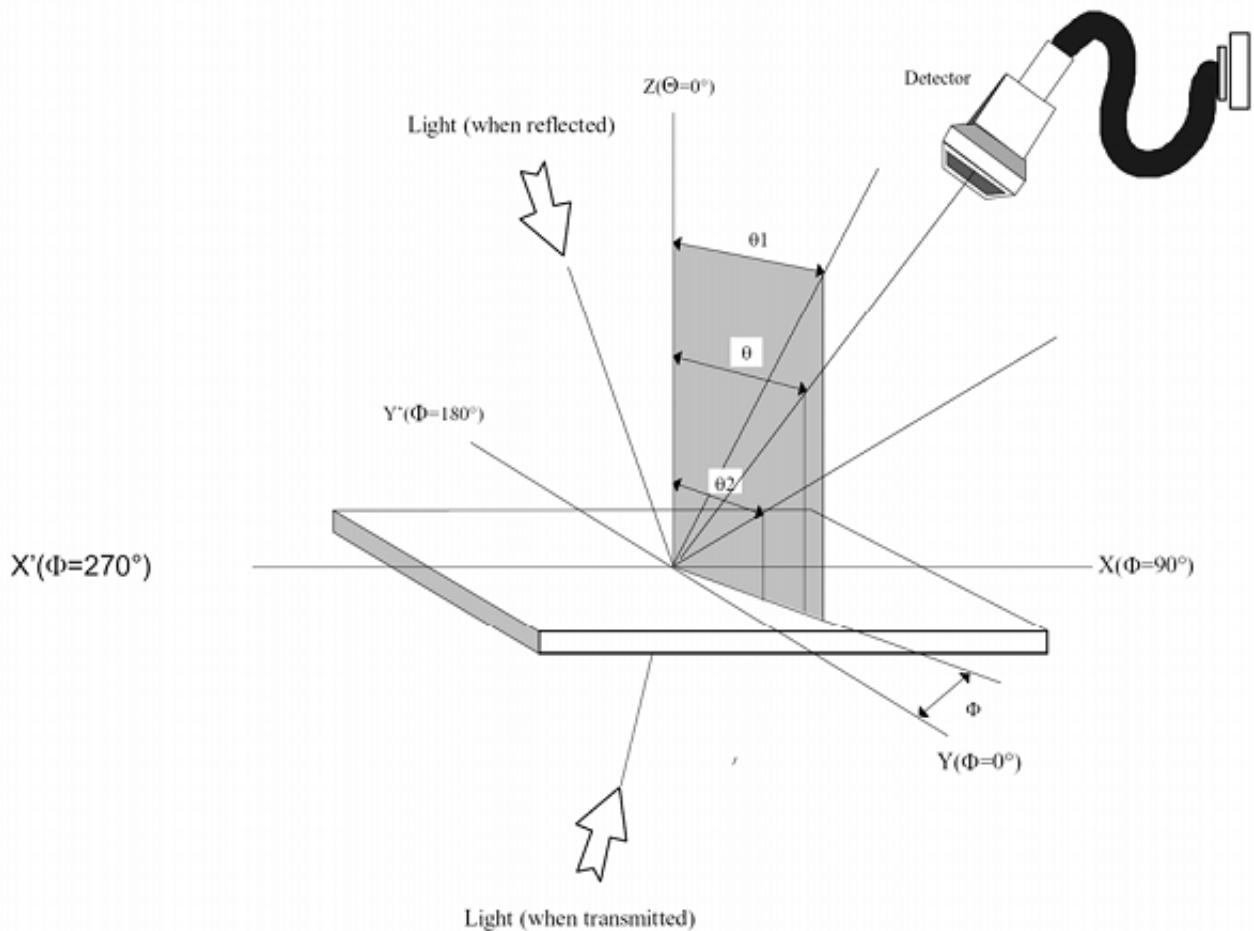
14. IC LAYOUT



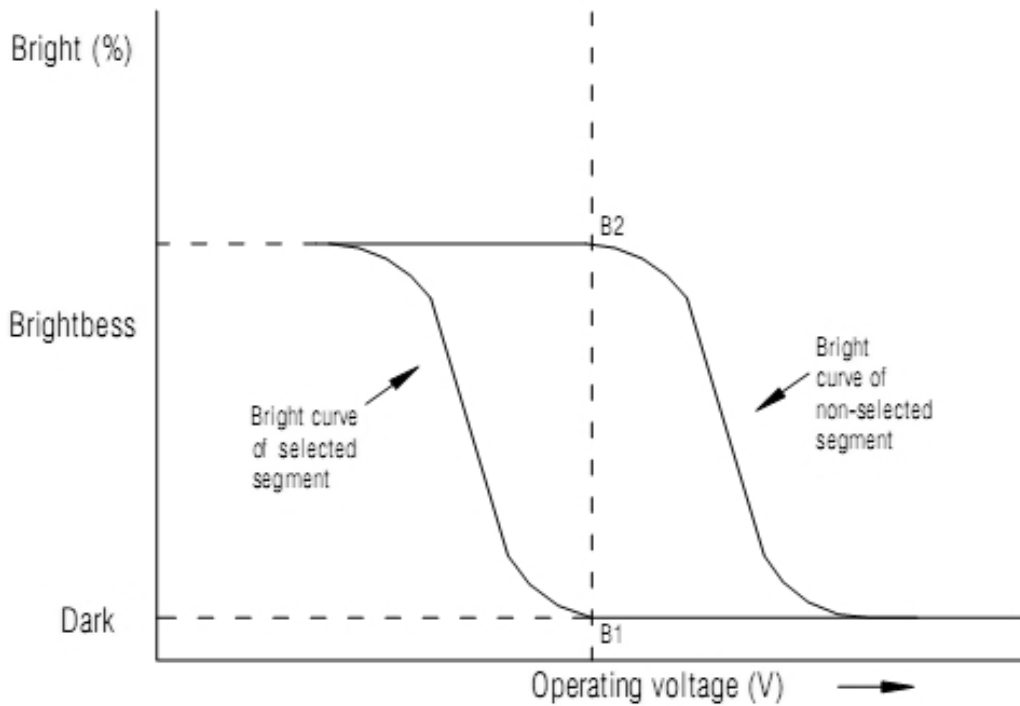
15. LCD ELECTRICAL& OPTICAL CHARACTERISTICS

Item	Symbol	Description	Condition	Temp.	Min.	Typ.	Max.	Unit
Operating Voltage for LCD	Vop		Ta=20°C		15.8	16.1	16.4	V
			Ta=25°C		15.3	15.6	15.9	
			Ta=70°C		14.8	15.1	15.4	
Contrast	Cr		VDD=3.3V±3%	25°C	2	4	—	
Viewing Angle	θ	6 o'clock axis (θ=0°)	Cr≥2.0 VDD=3.3V±3%	25°C	—	40	—	
		12 o'clock axis (θ=180°)	VDD=3.3V±3%		—	35	—	
		3 o'clock axis (θ=90°)	VDD=3.3V±3%		—	35	—	
		9 o'clock axis (θ=270°)	VDD=3.3V±3%		—	35	—	
Response Time	Tr	Rise		25°C	—	250	500	ms
	Tf	Fall		25°C	—	360	600	

15.1 Definition of Characteristics.

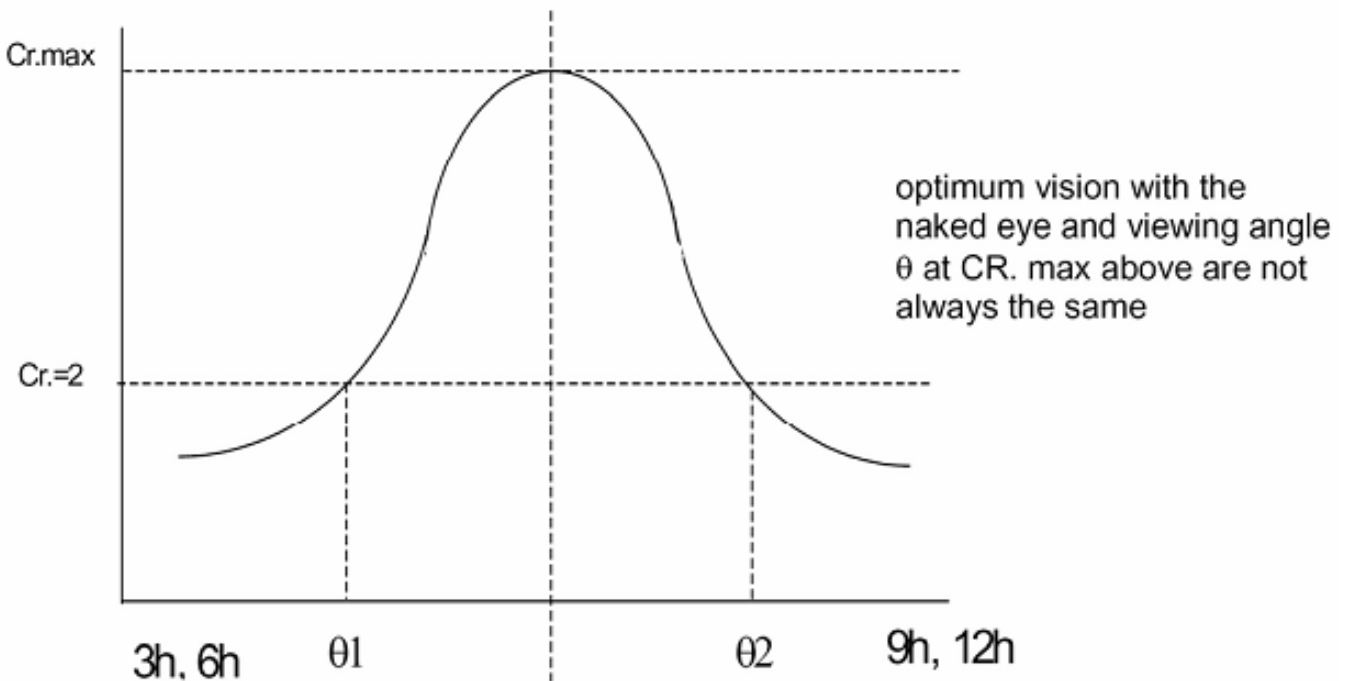


Definition of contrast $Cr. = \frac{B2}{B1} = \frac{\text{Bright curve of not selected segment}}{\text{Bright curve of selected segment}}$

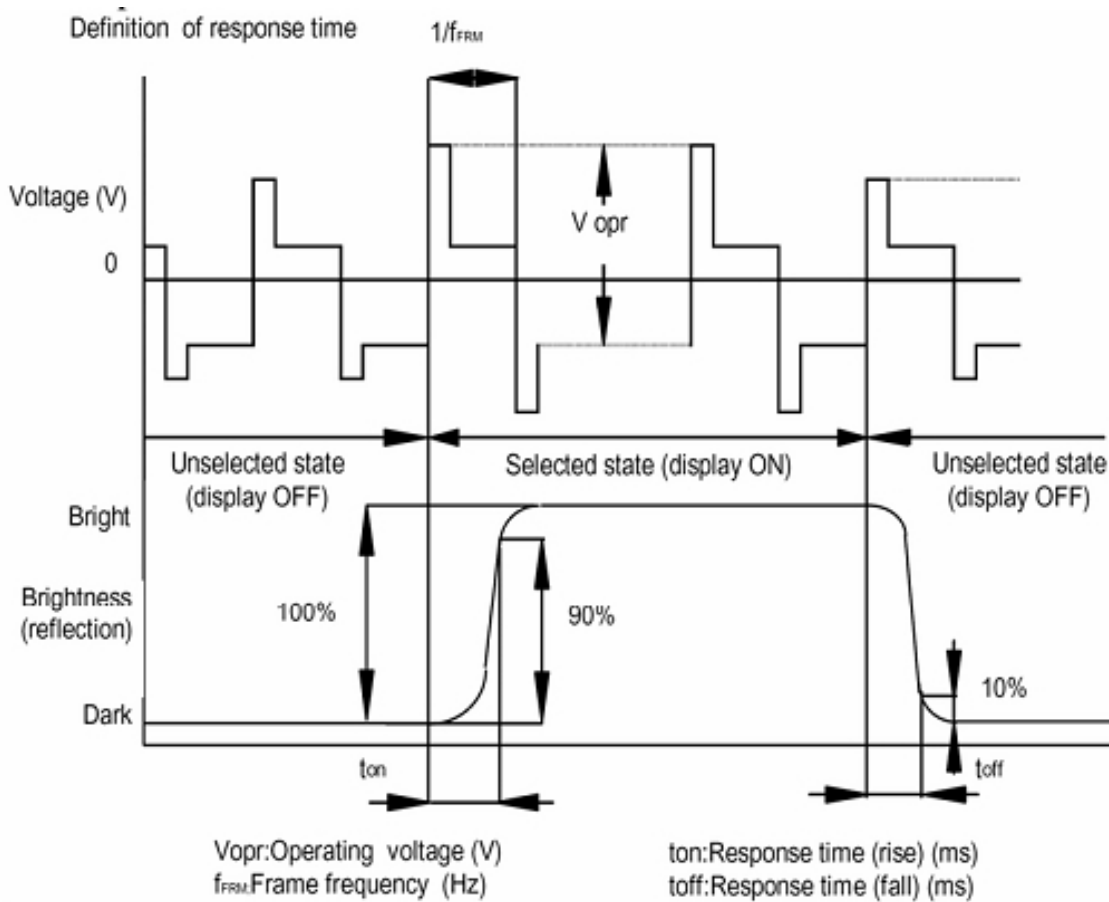


15.2 Definition of Viewing Angle

Definition of viewing angle θ_1 and θ_2



15.3 Definition of Response Time



16. ACCEPT QUALITY LEVEL (AQL)

16.1 Inspection Plan: ANSI Z-1.4, Normal Inspection Level II, Single Sampling Plan.

17. RELIABILITY TEST

Operating LCD lifetime: Longer than 50000 hours (at room temperature without direct irradiation of sunlight)
 Reliability characteristics shall meet following requirements.

TEMPERATURE TESTS	NORMAL GRADE
High Temperature Storage	+ 80°C x 240hrs
Low Temperature Storage	-30°C x 240hrs
High Temperature Operation	+70° C x 96hrs
Low Temperature Operation	-20°C x 96hrs
High Temperature, High Humidity	+60°C x 90%RH x 240hrs
Thermal Shock	0°C x 30min → +25°C x 10s → +70°C x 30min 5Cycles
Vibration Test	Frequency x Swing x Time 40Hz x 4mm x 4hrs
Drop Test	Drop Height x No. of drops 1.0m x 6 drops

18. LCD MODULES HANDLING PRECAUTIONS

- Please remove the protection foil of polarizer before using.
- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.
- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.
- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
 - Be sure to ground the body when handling the LCD module.
 - Tools required for assembly, such as soldering irons, must be properly grounded.
 - To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
 - The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.
- Storage precautions
When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

19. OTHERS

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.
- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.
- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules:
 - Exposed area of the printed circuit board
 - Terminal electrode sections