

**DISPLAY Elektronik GmbH**

**DATA SHEET**

**LCD MODULE**

**DEM 1280640 FGH**

*Product Specification*

*Version: 1*

**02/Dec/2011**



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**1. FUNCTIONS & FEATURES**

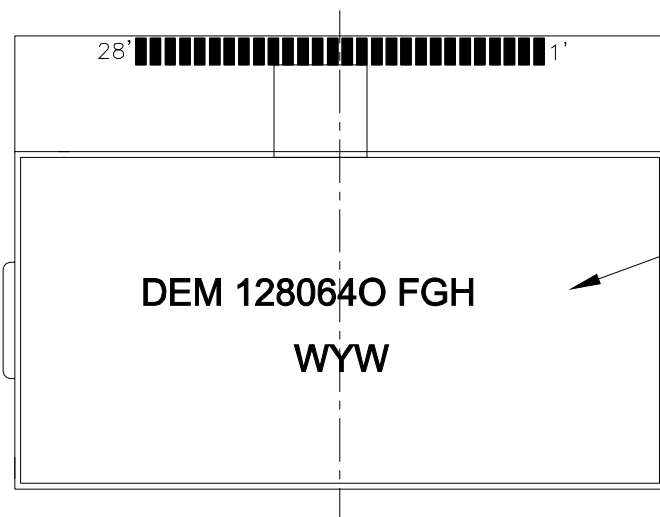
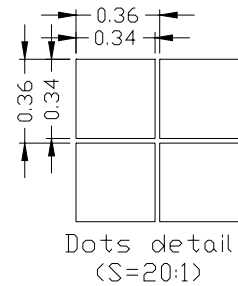
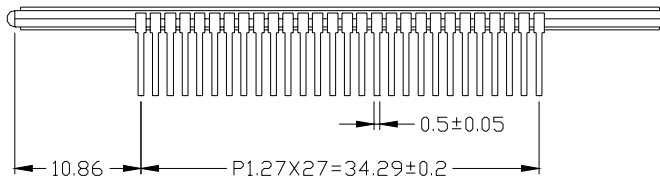
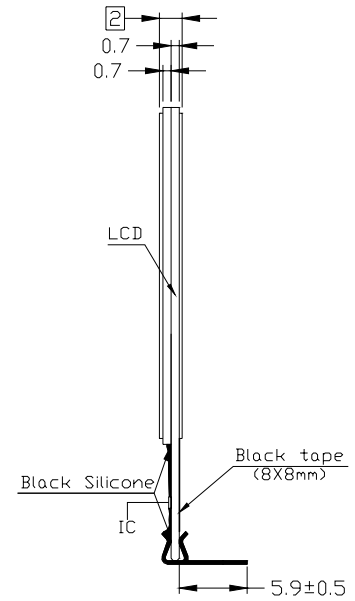
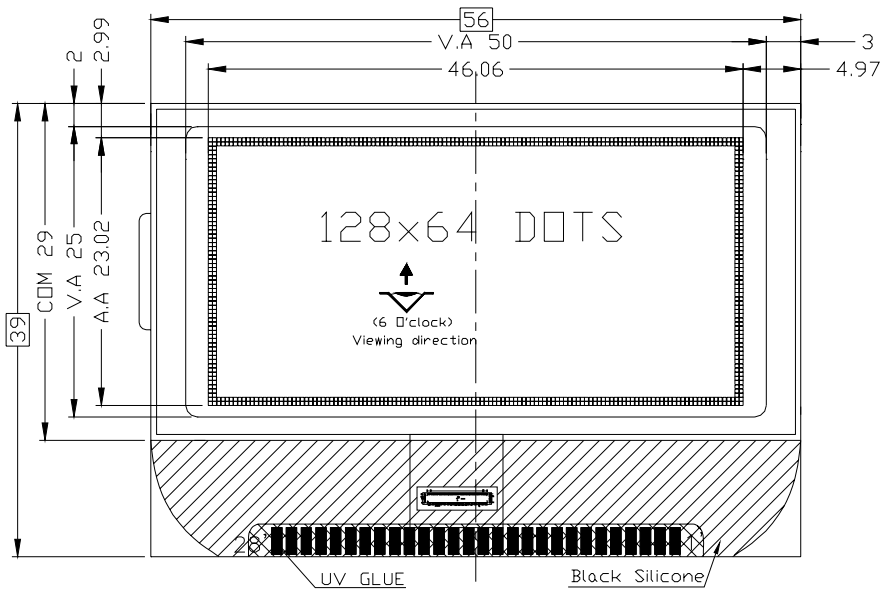
<b>MODULE NAME</b>	<b>LCD TYPE</b>
DEM 1280640 FGH	FSTN Reflective Positive Mode

- Viewing Direction : 6 o'clock
- Driving Scheme : 1/65 Duty, 1/9 Bias
- Power Supply Voltage : 3.0 Volt (typ.)
- V<sub>LCD</sub> : 9.0 Volt (typ.)
- Display Contents : 128 x 64 Dots
- Driver IC : ST7565R (Sitronix)
- RoHS : Compliant

**2. MECHANICAL SPECIFICATIONS**

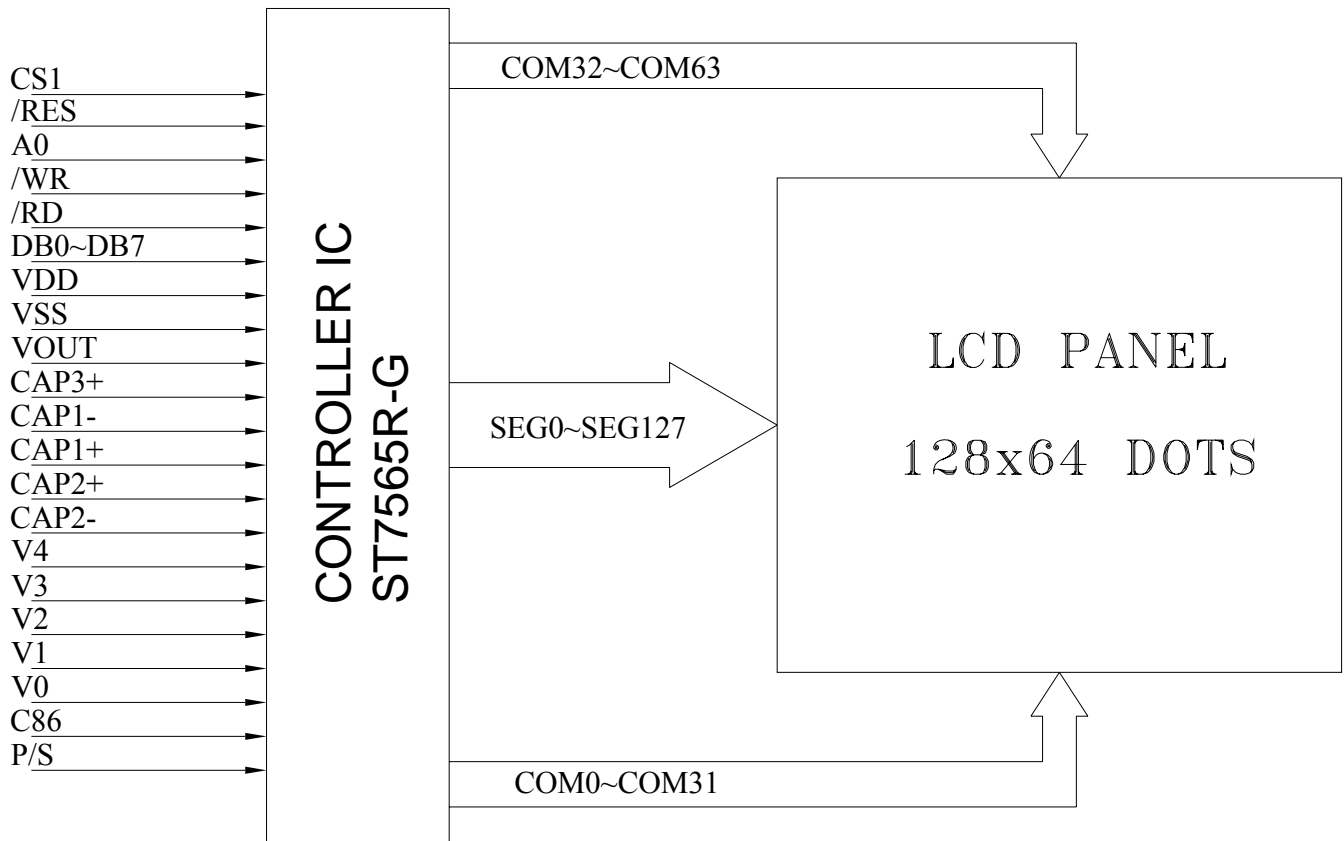
- Module Size : 56.00 x 39.00 x 2.00 mm
- Viewing Area : 50.00 x 25.00 mm
- Active Area : 46.06 x 23.02 mm
- Dot Size : 0.34 x 0.34 mm
- Dot Gap : 0.02 mm

3. EXTERNAL DIMENSIONS



- Remarks:
1. Unmarked tolerance is  $\pm 0.3$
  2. All materials comply with RoHs
  3.  ...critical dimension.

4. BLOCK DIAGRAM



5. PIN ASSIGNMENT

PIN No.	Symbol	I/O	Description										
1	CS1	I	the chip select signal.										
2	/RES	I	When /RES is set to "L", the register settings are initialized (cleared). The reset operation is performed by the /RES signal level.										
3	A0	I	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.										
4	/WR	I	When connected to 8080 series MPU, this pin is treated as the "/WR" signal of the 8080 MPU and is LOW-active. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to 6800 series MPU, this pin is treated as the "R/W" signal of the 6800 MPU and decides the access type : When R/W = "H": Read. When R/W = "L": Write.										
5	/RD	I	When connected to 8080 series MPU, this pin is treated as the "/RD" signal of the 8080MPU and is LOW-active. The data bus is in an output status when this signal is "L". When connected to 6800 series MPU, this pin is treated as the "E" signal of the 6800 MPU and is HIGH-active. This is the enable clock input terminal of the 6800 Series MPU.										
6~13	DB0~DB7	I/O	Data bus. This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.										
14	VDD	Power	Power Supply.										
15	VSS	Power	Ground										
16	VOUT	O	DC/DC voltage converter. Connect a capacitor between this terminal and VSS or VDD terminal.										
17	CAP3+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.										
18	CAP1-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.										
19	CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.										
20	CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.										
21	CAP2-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.										
22	V4	I/O	This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on Vss, and must maintain the relative magnitudes shown below. $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{ss}$										
23	V3	I/O											
24	V2	I/O											
25	V1	I/O											
26	V0	I/O											
			<table border="1"> <thead> <tr> <th></th> <th>1/65 DUTY</th> </tr> </thead> <tbody> <tr> <td>V1</td> <td><math>8/9 * V_0, 6/7 * V_0</math></td> </tr> <tr> <td>V2</td> <td><math>7/9 * V_0, 5/7 * V_0</math></td> </tr> <tr> <td>V3</td> <td><math>2/9 * V_0, 2/7 * V_0</math></td> </tr> <tr> <td>V4</td> <td><math>1/9 * V_0, 1/7 * V_0</math></td> </tr> </tbody> </table>		1/65 DUTY	V1	$8/9 * V_0, 6/7 * V_0$	V2	$7/9 * V_0, 5/7 * V_0$	V3	$2/9 * V_0, 2/7 * V_0$	V4	$1/9 * V_0, 1/7 * V_0$
	1/65 DUTY												
V1	$8/9 * V_0, 6/7 * V_0$												
V2	$7/9 * V_0, 5/7 * V_0$												
V3	$2/9 * V_0, 2/7 * V_0$												
V4	$1/9 * V_0, 1/7 * V_0$												
27	C86	I	This is the MPU interface selection pin.C86 = "H": 6800 Series MPU interface. C86 = "L": 8080 Series MPU interface.										
28	P/S	I	This pin configures the interface to be parallel mode or serial mode. P/S = "H": Parallel data input/output. P/S = "L": Serial data input.										

## 6. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power Supply for Logic	VDD-VSS	-0.3	---	3.6	V
Power Supply for LCD	V0-VSS	-0.3	---	13.5	V
Input Voltage	VIN	-0.3	---	VDD+0.3	V
Operating Temperature	Top	-20	---	70	°C
Storage Temperature	Tst	-30	---	80	°C

## 7. ELECTRICAL CHARACTERISTICS

### 7-1. Electrical Characteristics (Ta=25°C, VDD=3.0V)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply for LCM	VDD-VSS	---	2.85	3.0	3.15	V
LCD Module Driving Voltage	V0-VSS	25°C		9.0		V
Input Voltage	VIL	L level	Vss	---	0.2VDD	V
	VIH	H level	0.8VDD	---	VDD	V
Supply Current for LCM	IDD	VDD=3.0V	---	0.5	---	mA
	Ie	---	---	---	---	

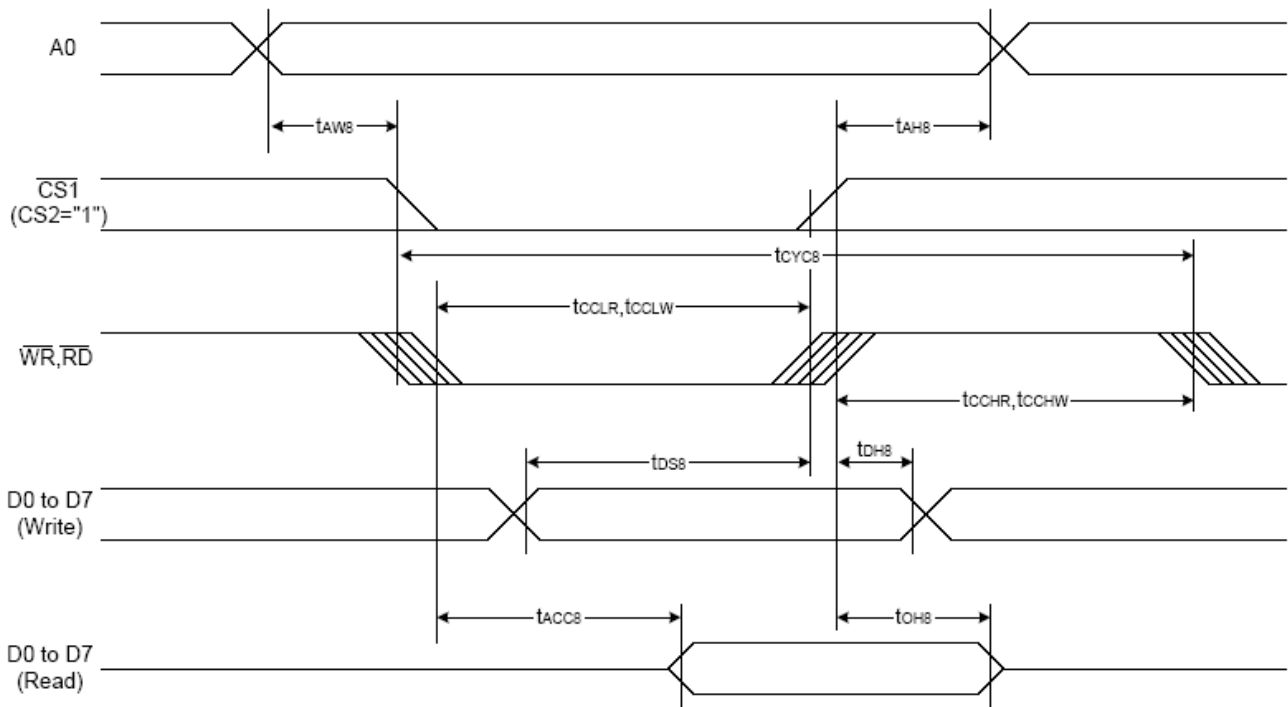
### 7-2 Electro-Optical Characteristics

Item	Symbol	Measuring Condition	STD. Value			Unit	
			°C	Min	Typ		Max
Recommended Operating Voltage	VLCD	$\theta = 0$ $\Phi = 0$	25	-	9.0	-	V
Operating Voltage	Vth	$\theta = 0$ $\Phi = 0$	0	-	-	-	
			25	-	9.0	-	
			40	-	-	-	
	Vsat	$\theta = 0$ $\Phi = 0$	0	-	-	-	
			25	-	-	-	
			40	-	-	-	
Response time	Tr	$\theta = 0$ $\Phi = 10$	0	-	-	-	
			25	-	218	268	
			40	-	-	-	
	Tf	$\theta = 0$ $\Phi = 10$	0	-	-	-	
			25	-	115	165	
			40	-	-	-	
Viewing Angle (Cr ≥ 2)	$\theta$	$\Phi = 0^\circ$	25	-10	10	40	Deg
	$\theta$	$\Phi = 180^\circ$	25	30	10	-	
	$\theta$	$\Phi = 90^\circ$	25	30	-	-	
	$\theta$	$\Phi = 270^\circ$	25	-	-	-	
Current Consumption	ILCD	Hz = 64	25		82		uA



7-3 AC characteristics

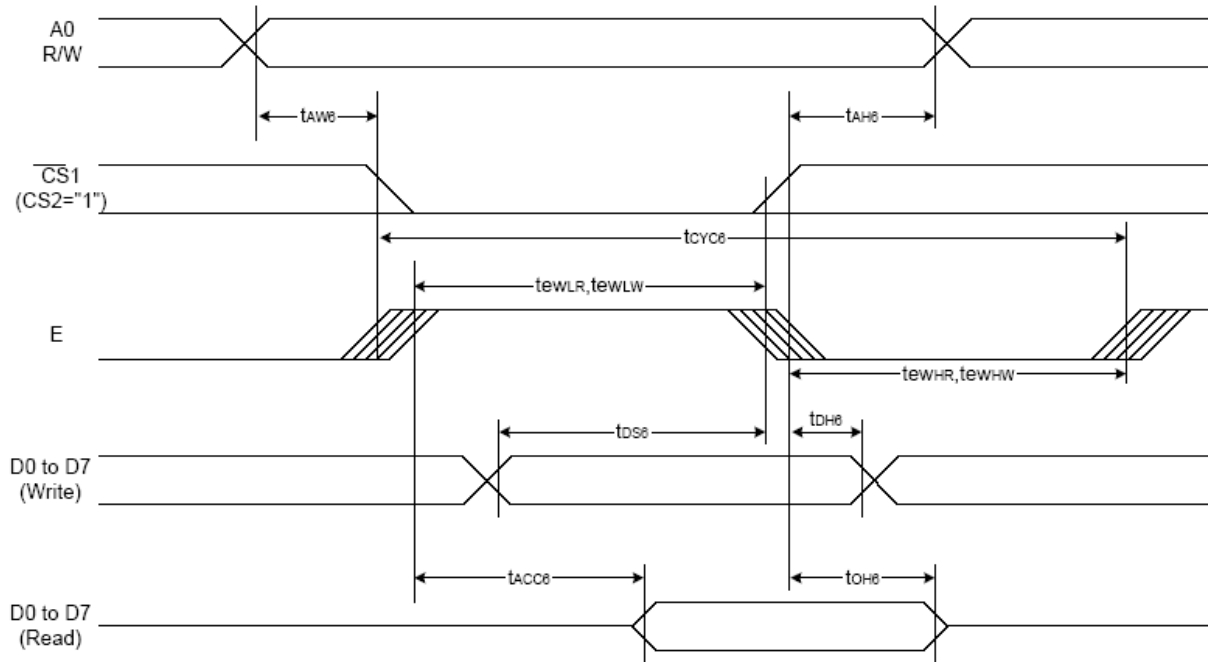
System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)



(V<sub>SS</sub> = 0V, V<sub>DD</sub> = 3.0V, TA=25°C)

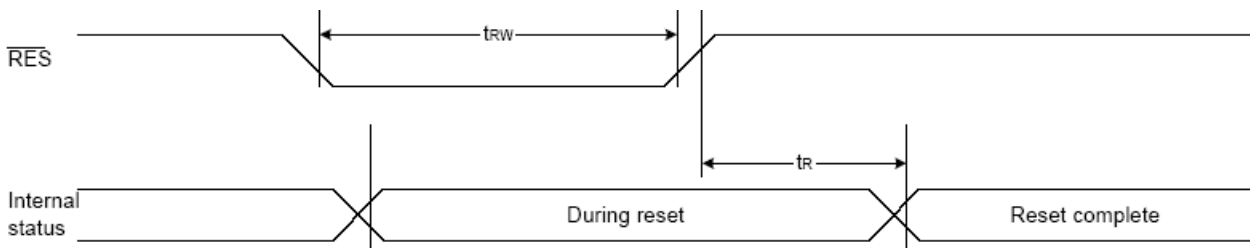
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t <sub>AH8</sub>		0	—	Ns
Address setup time		t <sub>AW8</sub>		0	—	
System cycle time		t <sub>CYC8</sub>		240	—	
Enable L pulse width (WRITE)	WR	t <sub>CCLW</sub>		80	—	
Enable H pulse width (WRITE)		t <sub>CCHW</sub>		80	—	
Enable L pulse width (READ)	RD	t <sub>CCLR</sub>		140	—	
Enable H pulse width (READ)		t <sub>CCHR</sub>		80	—	
WRITE Data setup time	D0 to D7	t <sub>DS8</sub>		40	—	
WRITE Address hold time		t <sub>DH8</sub>		0	—	
READ access time		t <sub>ACC8</sub>	CL = 100 pF	—	70	
READ Output disable time		t <sub>OH8</sub>	CL = 100 pF	5	50	

System Bus Read/Write Characteristics 2 (For the 6800 Series MPU)



Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	$t_{AH6}$		0	—	ns
Address setup time		$t_{AW6}$		0	—	
System cycle time		$t_{CYC6}$		240	—	
Enable L pulse width(WRITE)	WR	$t_{EWLW}$		80	—	
Enable H pulse width (WRITE)		$t_{EWHW}$		80	—	
Enable L pulse width (READ)	RD	$t_{EWLR}$		80	—	
Enable H pulse width (READ)		$t_{EWHR}$		140	—	
WRITE Data setup time	D0 to D7	$t_{DS6}$		40	—	
WRITE Address hold time		$t_{DH6}$		0	—	
READ access time		$t_{ACC6}$	CL = 100 pF	—	70	
READ Output disable time		$t_{OH6}$	CL = 100 pF	5	50	

7-4. Reset Characteristics



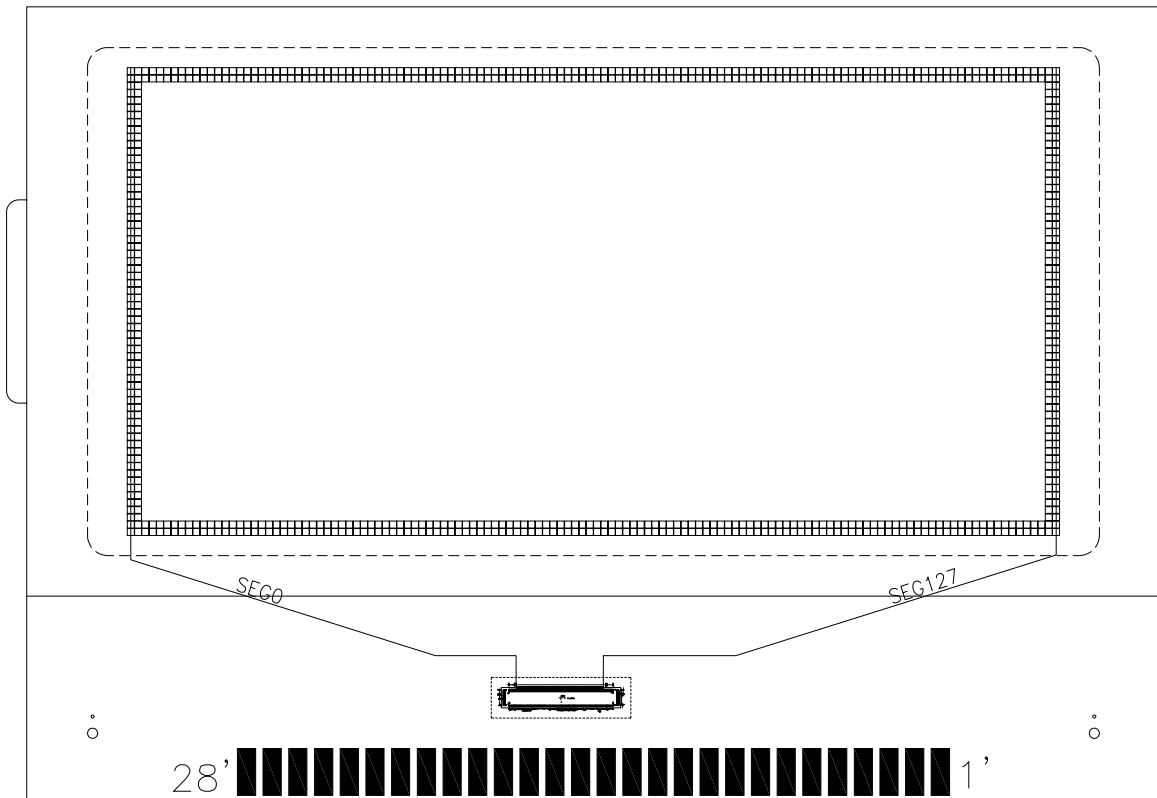
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		$t_r$		—	—	1.0	us
Reset "L" pulse width	/RES	$t_{rw}$		1.0	—	—	us

8. COMMAND TABLE

Command	Command Code									Function		
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2		D1	D0
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address					Sets the display RAM display start line address	
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address.
Column address set lower bit				0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status			0	0	0	0	Reads the status data	
(6) Display data write	1	1	0	Write data							Writes to the display RAM	
(7) Display data read	1	0	1	Read data							Reads from the display RAM	
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565R)
(12) Read-modify-write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode		Select internal power supply operating mode	
(17) V <sub>0</sub> voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio		Select internal resistor ratio(Rb/Ra) mode	
(18) Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	Set the V <sub>0</sub> output voltage electronic volume register
Electronic volume register set				0	0	Electronic volume value						
(19) Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0	0: OFF, 1: ON
Static indicator register set				0	0	0	0	0	0	0	0	Mode
(20) Booster ratio set	0	1	0	1	1	1	1	1	0	0	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power save	0	1	0								Display OFF and display all points ON compound command	
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

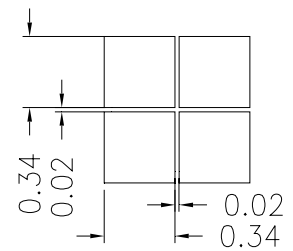


**9-3. SEGMENT LAYOUT**



**9-4. GRAPHIC DIMENSION & PAD CONFIGURATION**

<u>PAD NO.</u>	<u>PAD CONFIGURATION</u>
1	COM63[R63(C0-C127)]
32	COM32[R32(C0-C127)]
33	SEG127[C127(R0-R63)]
160	SEG0[C0(R0-R63)]
161	COM0[R0(C0-C127)]
192	COM31[R31(C0-C127)]



9-5. IC LAYOUT

