

DISPLAY Elektronik GmbH

DATA SHEET

LCD MODULE

DEM 128064G FGH-P(RGB)

Product specification

Version: 5

19/Aug/2013

GENERAL SPECIFICATION

MODULE NO. :

DEM 128064G FGH-P(RGB)

CUSTOMER P/N:

Version No.	Change Description	Date
0	Original Version	17.12.2008
1	Update Module Drawing	07.05.2009
2	Update Backlight Parameter	15.06.2009
3	Update Backlight Parameter	26.06.2009
4	Change UL	29.03.2013
5	Change Customer P/N	19.08.2013

PREPARED BY: LX

DATE: 19.08.2013

APPROVED BY: MHO

DATE: 19.08.2013

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1. FUNCTIONS & FEATURES

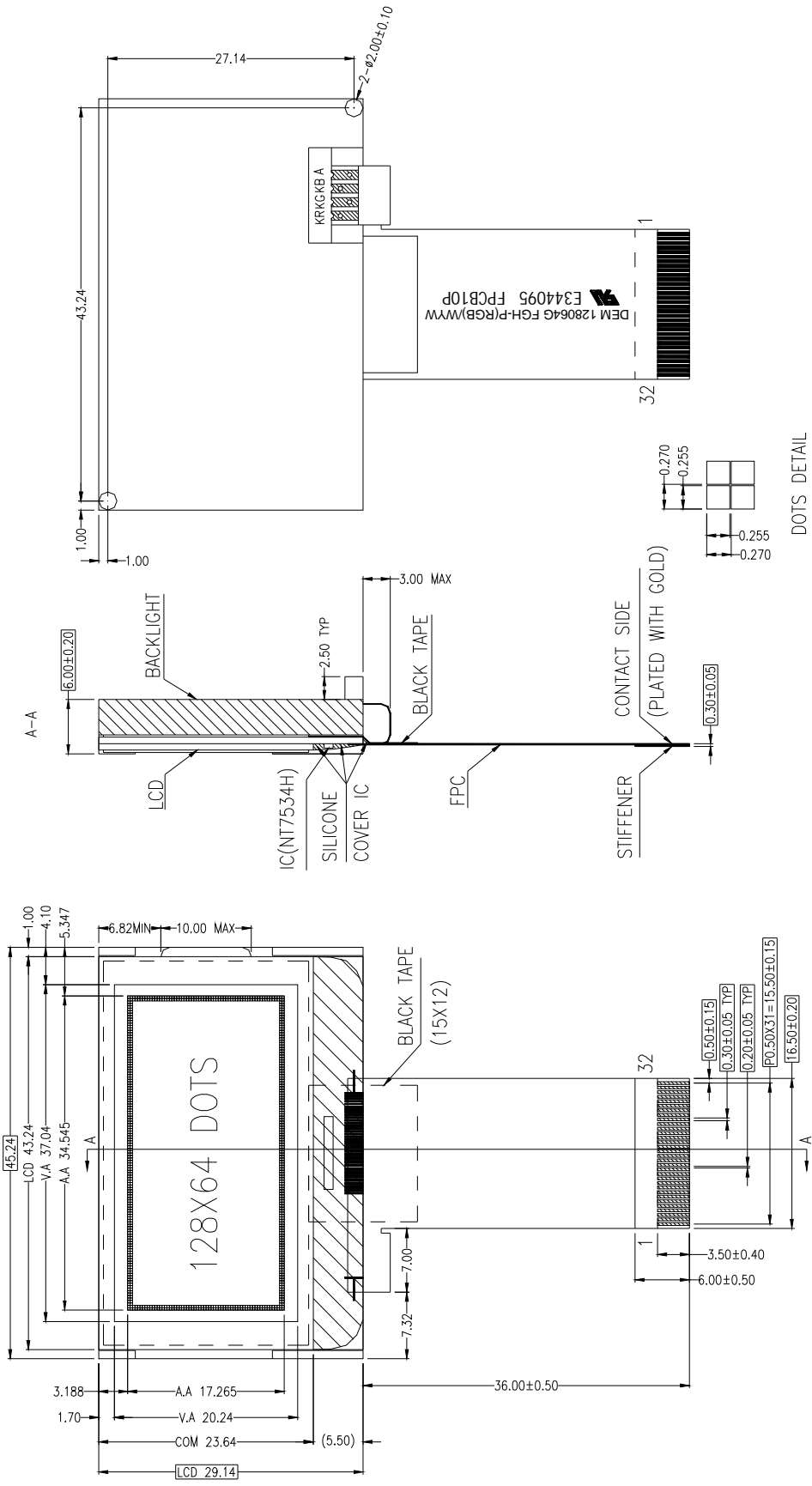
Module	LCD Type
DEM 128064G FGH-P(RGB)	FSTN Transflective Positive Mode

- I Viewing Direction : 6 O'clock
- I Driving Scheme : 1/ 65 Duty, 1/ 9 Bias,
- I Power supply : 3.3 Volt (typ.)
- I V_{LCD}(V₀-V_{SS}) : 10.7 Volt (typ.)
- I Display Contents : 128 x 64 Dots
- I Interface : Parallel & Serial
- I LCD Driver : NT7534H (Novatek)
- I Operating Temperature : -20°C to +70°C
- I Storage Temperature : -30°C to +80°C
- I RoHS : Compliant

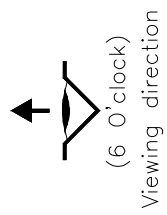
2. MODULE ARTWORK

- I Module Size : 45.24 x 29.14 x 6.00 mm (Without FPC)
- I Viewing Area : 37.04 x 20.24 mm
- I Active Area : 34.545 x 17.265 mm
- I Dot Size : 0.255 x 0.255 mm
- I Dot Pitch : 0.27 x 0.27 mm
- I Dot Gap : 0.015 mm

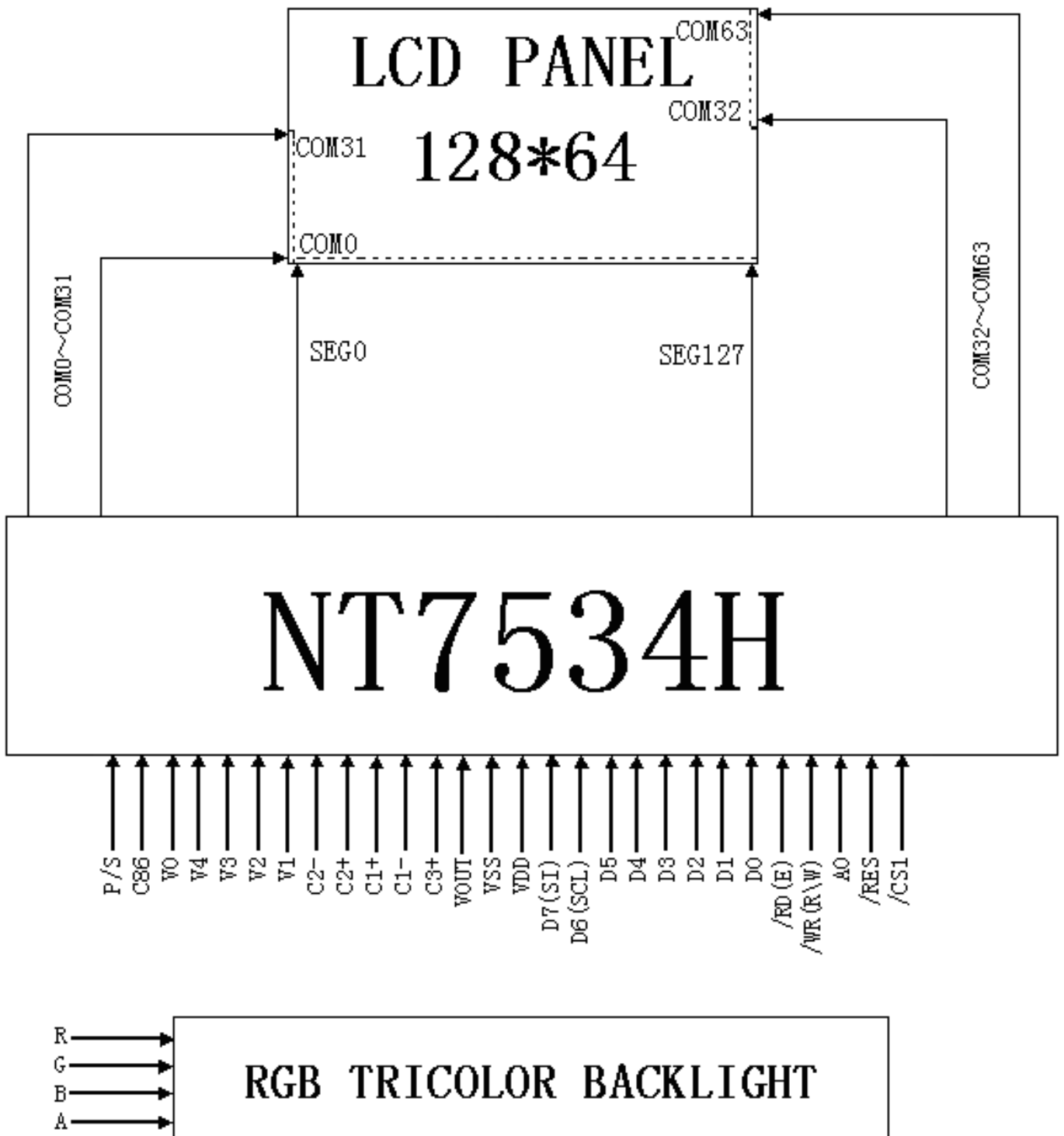
3. EXTERNAL DIMENSIONS



Remarks:
 1. Unmarked tolerance is ±0.3
 2. All materials comply with RoHs
 3. []critical dimension.



4. BLOCK DIAGRAM



5. PIN ASSIGNMENT.

PIN NO.	Symbol	Description																				
1	R	Cathode of RED LED backlight.																				
2	G	Cathode of GREEN LED backlight.																				
3	B	Cathode of BLUE LED backlight.																				
4	A	Anode of LED backlight																				
5	P/S	<p>This is the parallel data input/serial data input switch terminal P/S = “H”: Parallel data input P/S = “L”: Serial data input The following applies depending on the P/S status:</p> <table border="1"> <thead> <tr> <th>P/S</th> <th>Data/command</th> <th>Data</th> <th>Read/Write</th> <th>Serial Clock</th> </tr> </thead> <tbody> <tr> <td>“H”</td> <td>A0</td> <td>D0 to D7</td> <td>/RD,/WR</td> <td>-</td> </tr> <tr> <td>“L”</td> <td>A0</td> <td>SI(D7)</td> <td>Write only</td> <td>SCL(D6)</td> </tr> </tbody> </table> <p>When P/S = “L”, D0 to D5 are HZ. D0 to D5 may be “H”, “L” or Open. /RD (E) and /WR (R/W) are fixed to either “H” or “L”. With serial data input, RAM display data reading is not supported.</p>	P/S	Data/command	Data	Read/Write	Serial Clock	“H”	A0	D0 to D7	/RD,/WR	-	“L”	A0	SI(D7)	Write only	SCL(D6)					
P/S	Data/command	Data	Read/Write	Serial Clock																		
“H”	A0	D0 to D7	/RD,/WR	-																		
“L”	A0	SI(D7)	Write only	SCL(D6)																		
6	C86	<p>This is the MPU interface switch terminal C86 = “H”: 6800 Series MPU interface C86 = “L”: 8080 Series MPU interface.</p>																				
7	V0	<p>LCD driver supplies voltages. The voltage determined by the LCD cell is impedance-converted by a resistive driver or an operation amplifier for application. Voltages should be according to the following relationship: $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS2$ When the on-chip operating power circuit is on, the following voltages are supplied to V1 to V4 by the on-chip power circuit. Voltage selection is performed by the LCD Bias Set command.</p>																				
8	V4																					
9	V3																					
10	V2	<table border="1"> <thead> <tr> <th>LCD bias</th> <th>V1</th> <th>V2</th> <th>V3</th> <th>V4</th> </tr> </thead> <tbody> <tr> <td>1/4bias</td> <td>3/4 V0</td> <td>2/4 V0</td> <td>2/4 V0</td> <td>1/4 V0</td> </tr> <tr> <td>1/5bias</td> <td>4/5 V0</td> <td>3/5 V0</td> <td>2/5 V0</td> <td>1/5 V0</td> </tr> <tr> <td>1/6bias</td> <td>5/6 V0</td> <td>4/6 V0</td> <td>2/6 V0</td> <td>1/6 V0</td> </tr> </tbody> </table>	LCD bias	V1	V2	V3	V4	1/4bias	3/4 V0	2/4 V0	2/4 V0	1/4 V0	1/5bias	4/5 V0	3/5 V0	2/5 V0	1/5 V0	1/6bias	5/6 V0	4/6 V0	2/6 V0	1/6 V0
LCD bias	V1	V2	V3	V4																		
1/4bias	3/4 V0	2/4 V0	2/4 V0	1/4 V0																		
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11	V1	<table border="1"> <tbody> <tr> <td>1/7bias</td> <td>6/7 V0</td> <td>5/7 V0</td> <td>2/7 V0</td> <td>1/7 V0</td> </tr> <tr> <td>1/8bias</td> <td>7/8 V0</td> <td>6/8 V0</td> <td>2/8 V0</td> <td>1/8 V0</td> </tr> <tr> <td>1/9bias</td> <td>8/9 V0</td> <td>7/9 V0</td> <td>2/9 V0</td> <td>1/9 V0</td> </tr> </tbody> </table>	1/7bias	6/7 V0	5/7 V0	2/7 V0	1/7 V0	1/8bias	7/8 V0	6/8 V0	2/8 V0	1/8 V0	1/9bias	8/9 V0	7/9 V0	2/9 V0	1/9 V0					
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12	C2-	Capacitor 2- pad for internal DC/DC voltage converter																				
13	C2+	Capacitor 2+ pad for internal DC/DC voltage converter																				
14	C1+	Capacitor 1+ pad for internal DC/DC voltage converter																				
15	C1-	Capacitor 1- pad for internal DC/DC voltage converter																				
16	C3+	Capacitor 3+ pad for internal DC/DC voltage converter																				
17	VOUT	DC/DC voltage converter output																				
18	VSS	Ground																				
19	VDD	Power supply input																				
20	D7(SI)	<p>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S=“L”), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance.</p>																				
21	D6(SCL)																					
22	D5																					
23	D4																					
24	D3																					
25	D2																					
26	D1																					
27	D0																					
28	/RD(E)	When connected to an 8080 MPU, it is active LOW. This pad is connected to the																				

		/RD signal of the 8080MPU, and the NT7534 data bus is in an output status when this signal is “L”. When connected to a 6800 Series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU
29	/WD(R/W)	When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU, this is the read/write control signal input terminal. When R/W = “H”: Read When R/W = “L”: Write
30	A0	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = “H”: Indicate that D0 to D7 are display data A0 = “L”: Indicates that D0 to D7 are control data
31	/RSE	When /RES is set to “L”, the settings are initialized. The reset operation is performed by the /RES signal level
32	/CS1	This is the chip select signal. When /CS1=“L” and CS2=“H”, then the chip select becomes active, and data/command I/O is enabled.

6. BACKLIGHT ELECTRICAL /OPTICAL CHARATERISTICS

Electronics/Optical Specifications:

RED:

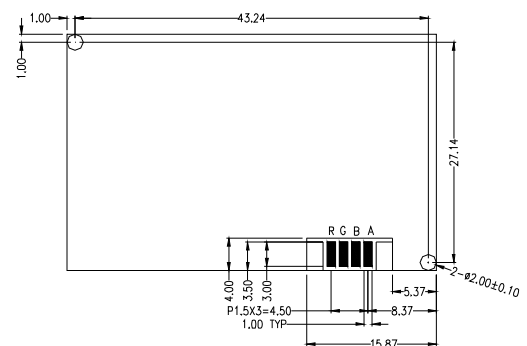
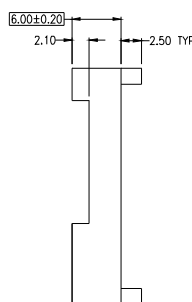
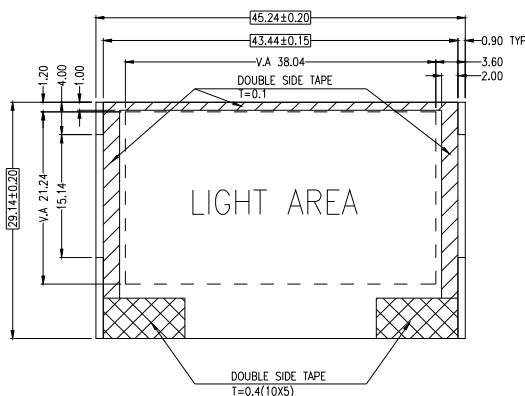
	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Forward Voltage	V_f		3.3		V	
Forward Current	I_f	--	30	40	mA	$V_f=3.3V$
Power Dissipation	P_d	--	--	0.132	W	$V_f=3.3V$
Reverse Voltage	V_R	--	--	5	V	--
Reverse Current	I_R	--	--	0.1	mA	$V_R=5V$ Each chip
Luminous Intensity	I_v	20	50	--	cd/m ²	$V_f=3.3V$
Luminous Uniformity	ΔIV	65	--	--	%	$V_f=3.3V$
Emission Wavelength	λ_p	620	--	630	nm	$I_f=25mA$ $T_a=25^\circ C$ Each chip

Blue:

	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Forward Voltage	V_f		3.3		V	
Forward Current	I_f	--	30	40	mA	$V_f=3.3V$
Power Dissipation	P_d	--	--	0.132	W	$V_f=3.3V$
Reverse Voltage	V_R	--	--	5	V	--
Reverse Current	I_R	--	--	0.1	mA	$V_R=5V$ Each chip
Luminous Intensity	I_v	12	20	--	cd/m ²	$V_f=3.3V$
Luminous Uniformity	ΔIV	65	--	--	%	$V_f=3.3V$
Emission Wavelength	λ_p	465	--	476	nm	$I_f=15mA$ $T_a=25^\circ C$ Each chip

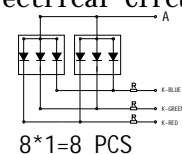
Green:

	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Forward Voltage	V_f		3.3		V	
Forward Current	I_f	--	30	40	mA	$V_f=3.3V$
Power Dissipation	P_d	--	--	0.132	W	$V_f=3.3V$
Reverse Voltage	V_R	--	--	5	V	--
Reverse Current	I_R	--	--	0.1	mA	$V_R=5V$ Each chip
Luminous Intensity	I_v	60	90	--	cd/m ²	$V_f=3.3V$
Luminous Uniformity	ΔIV	65	--	--	%	$V_f=3.3V$
Emission Wavelength	λ_p	520	--	530	nm	$I_f=15mA$ $T_a=25^\circ C$ Each chip



- Remarks:
- 1.Unmarked tolerance is ± 0.3
 - 2.All materials comply with RoHs
 3. ...:critical dimension.
 - 4.COLOR:RGB
 - 5.life time 50,000 hours

Electrical Circuit



7. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Power	VDD	-0.3	+4.0	V
Voltage converter output	Vout	-0.3	+15.0	V
LCD supply voltage	V0	-0.3	15.0	V
Operating temperature	Topr	-20	+70	°C
Storage temperature	Tstg	-30	+80	°C

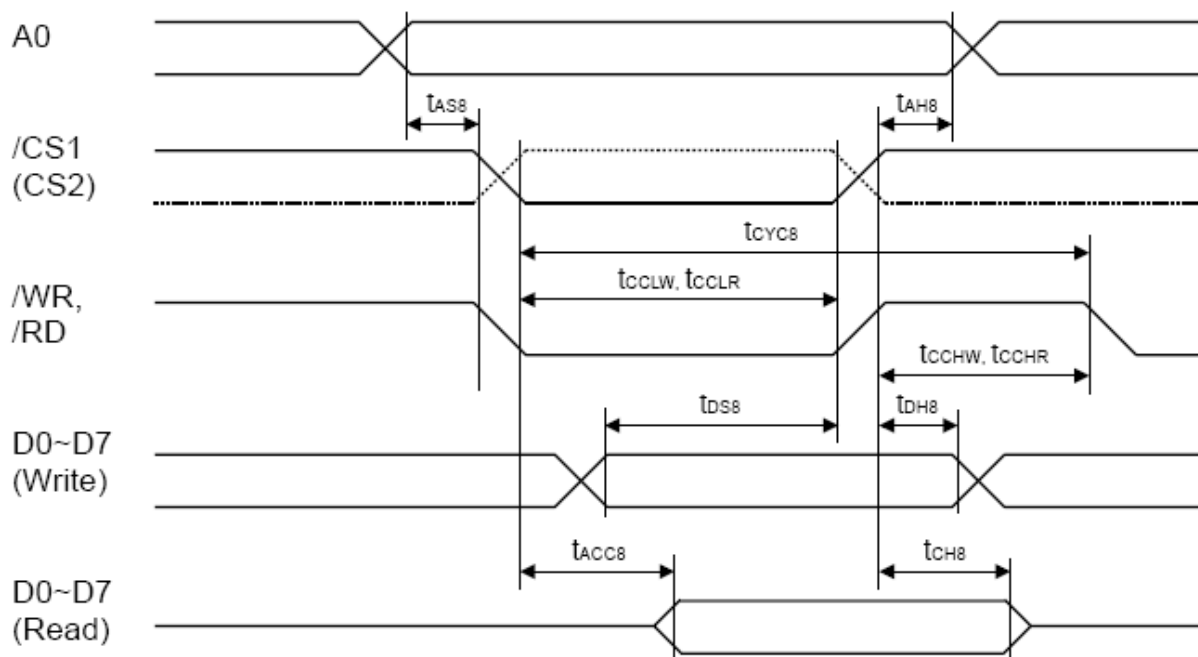
8. ELECTRICAL CHARACTERISTICS

8-1. DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V _{DD}	3.0	3.3	3.6	V	
LCD Voltage	V _{LCD}	10.4	10.7	11.0	V	V ₀ -V _{SS}
IDD	Current consumption	-	20	35	uA	VDD=3.3V, V0=10.7V, built-in boosting power supply off, display on, Display data=checker and no access Ta=25°C
		-	90	160	uA	VDD=3.3V, V0=10.7V, 4X built-in boosting power supply, display on, Display data=checker and no access, Temperature radiant is -0.05%/°C, Ta=25°C
		-	150	255	uA	VDD=3.3V, V0=10.7V, 4X built-in boosting power supply, display on, Display data=checker and no access, Temperature gradient is -0.05%/°C, Ta=25°C

8-2. AC Characteristics

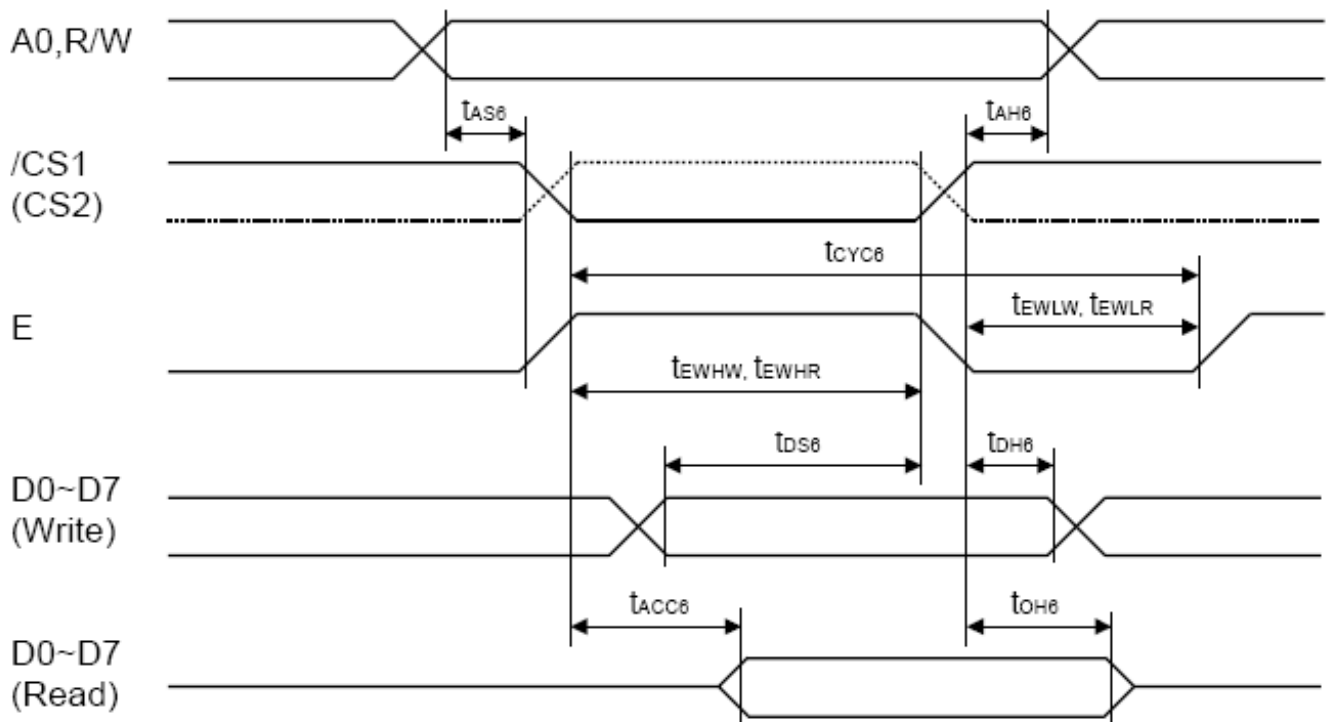
System Buses Read/Write Characteristics (for 8080 Series MPU)



Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T _{AH8}	Address hold time	0	-	-	ns	A0
T _{AS8}	Address setup time	0	-	-	ns	
t _{CYC8}	System cycle time	240	-	-	ns	
t _{CCLW}	Control low pulse width (write)	90	-	-	ns	/WR
t _{CCLR}	Control low pulse width (read)	120	-	-	ns	/RD
t _{CCHW}	Control high pulse width (write)	100	-	-	ns	/WR
t _{CCHR}	Control high pulse width (read)	60	-	-	ns	/RD
T _{DS8}	Data setup time	40	-	-	ns	D0~D7
T _{DH8}	Data hold time	10	-	-	ns	
t _{ACC8}	/RD access time	-	-	140	ns	D0~D7, CL = 100pF
T _{CH8}	Output disable time	5	-	50	ns	

- *1. The input signal rise time and fall time (tr, tr) is specified at 15ns or less.
 $(t_r + t_f) < (t_{CYC8} - t_{CCLW} - t_{CCHW})$ for write, $(t_r + t_f) < (t_{CYC8} - t_{CCLR} - t_{CCHR})$ for read.
- *2. All timing is specified using 20% and 80% of VDD as the reference.
- *3. t_{CCLW} and t_{CCLR} are specified as the overlap interval when /CS1 is low (CS2 is high) and /WR or /RD is low.

System Buses Read/Write Characteristics (for 6800 Series MPU)

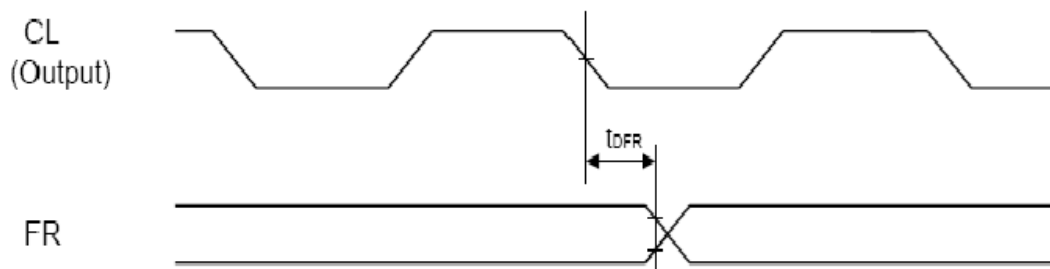


Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tscyc	Serial clock cycle	120	-	-	ns	SCL
tshw	Serial clock H pulse width	60	-	-	ns	SCL
tslw	Serial clock L pulse width	60	-	-	ns	SCL
tsas	Address setup time	30	-	-	ns	A0
tsah	Address hold time	20	-	-	ns	A0
tsds	Data setup time	30	-	-	ns	SI
tsdh	Data hold time	20	-	-	ns	SI
tcss	Chip select setup time	20	-	-	ns	/CS1, CS2
tcsH	Chip select hold time	40	-	-	ns	/CS1, CS2

*1. The input signal rise time and fall time (tr, tr) is specified as 15ns or less.

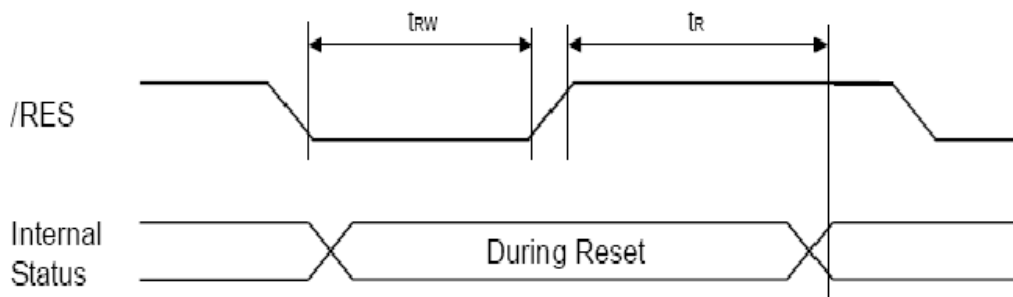
*2. All timing is specified using 20% and 80% of VDD as the standard.

Display Control Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tDFR	FR delay time	-	20	80	ns	CL = 50 pF

Reset Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tr	Reset Time	-	-	1.0	μs	
trw	Reset low pulse width	10	-	-	μs	/RES

9. INSTRUCTION DESCRIPTION

Command	A0	/RD	/WR	Code								Hex	Function	
				D7	D6	D5	D4	D3	D2	D1	D0			
(1)Display OFF	0	1	0	1	0	1	0	1	1	1	0	1	AEh AFh	Turn on LCD panel when high, and turn off when low
(2)Display start line set	0	1	0	0	1	Display start address					40h To 7Fh	Specifies RAM display line for com0		
(3)Page address set	0	1	0	1	0	1	1	Page address				B0h To B8h	Set the display data RAM page in page address register	
(4)Column address set	0	1	0	0	0	0	1	Higher column address			00h To 18h	Set 4 higher bits and 4 lower bits of column address of display data RAM in register		
	0	1	0	0	0	0	0	Lower column address						
(5)Read status	0	0	1	Status				0	0	0	0	XX	Read the status information	
(6)Write display data	1	1	0	Write data								XX	Write data in display data RAM	
(7)Read display data	1	0	1	Read data								XX	Read data from display data RAM	
(8)ADC select	0	1	0	1	0	1	0	0	0	0	0	1	A0h A1h	Set the display data RAM address SEG output correspondence
(9)Normal/Reverse display	0	1	0	1	0	1	0	0	1	1	0	1	A6h A7h	Normal indication when low .but full indication when high
(10)Entire display on/off	0	1	0	1	0	1	0	0	1	0	0	1	A4h A5H	Select normal display (0) or entire display on
(11)LCD bias set	0	1	0	1	0	1	0	0	0	1	0	1	A2h A3h	Sets LCD driving voltage bias ratio
(12)Read –modify-write	0	1	0	1	1	1	0	0	0	0	0	0	E0h	Increments column address counter during each write
13) End	0	1	0	1	1	1	0	1	1	1	0	0	EEh	Releases the Read-Modify -Write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	0	E2h	Resets internal functions
(15) Common Output Mode Select	0	1	0	1	1	0	1	0	1	*	*	*	C0h to CFh	Select COM output scan direction invalid data
(16) Power Control Set	0	1	0	0	0	1	0	1	Operation Status			28h to 2Fh	Select the power circuit operation mode	
17) V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h to 27h	Select internal resistor ratio Rb/Ra mode	
(18) Electronic Volume mode Set Electronic Volume Register Set	0	1	0	1	0	0	0	0	0	0	1	1	81h	
	0	1	0	*	*	Electronic Control Value					XX	Sets the V0 output voltage electronic volume register		
(19) Set Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0	1	ACH ADh	Sets static indicator ON/OFF 0: OFF, 1: ON

Set Static Indicator Register	0	1	0	*	*	*	*	*	*	Mode		XX	Sets the flash mode
(20) Power Save	0	1	0	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation
(22) Oscillation Frequency Select	0	1	0	1	1	1	0	0	1	0	0	E4h E5h	Select the oscillation frequency
(23) Partial Display mode Set	0	1	0	1	0	0	0	0	0	1	0	82h 83h	Enter/Release the partial display mode
(24) Partial Display Duty Set	0	1	0	0	0	1	1	0	Duty Ratio			30h 37h	Sets the LCD duty ratio for partial display mode
(25) Partial Display Bias Set	0	1	0	0	0	1	1	1	Bias Ratio			38h 3Fh	Sets the LCD bias ratio for partial display mode
(26) Partial Start Line Set	0	1	0	1	1	0	1	0	0	1	1	D3h	Enter Partial Start Line Set
Partial Start Line Set	0	1	0	1	1	Partial Start Line					XX	Sets the LCD Number of partial display start line	
(27) N-Line Inversion Set	0	1	0	1	0	0	0	0	1	0	1	85h	Enter N-Line inversion
Number of Line Set	0	0	*	*	*	*	Number of Line					XX	Sets the number of line used for N-Line inversion
(28) N-Line Inversion Release	0	1	0	1	0	0	0	0	1	0	0	84h	Exit N-Line Inversion
(29) DC/DC Clock Set	0	1	0	1	1	1	0	0	1	1	0	E6h	Set DC/DC Clock Frequency
DC/DC Clock Division Set	0	1	0	1	1	0	0	Clock Division				XX	Set the Division of DC/DC Clock Frequency
(30) Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!
(31) Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset

NOTE: Do not use any other command, or system malfunction may result

10. LCD MODULES HANDLING PRECAUTIONS

- n** The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- n** If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.
- n** Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- n** The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.
- n** To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
 - Be sure to ground the body when handling the LCD module.
 - Tools required for assembly, such as soldering irons, must be properly grounded.
 - To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
 - The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.
- n** Storage precautions
When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below -20°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

11. OTHERS

- n** Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.
- n** If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.
- n** To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules:
 - Exposed area of the printed circuit board
 - Terminal electrode sections.