DISPLAY Elektronik GmbH

DATA SHEET

PRODUCT SPECIFICATION

EPD MODULE

DEE 122250B-DWRY

2.13"

E-Paper Display

PRODUCT SPECIFICATION Ver.: 2.0

24.03.2025

Version	Content	Date	Producer
2.0	New release	24.03.2025	MH-AI

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1. Over View

DEE 122250B-DWRY is an Active Matrix EPD all-in-one driver with timing controller for ESL. The sources have 2-bit outputs per pixel to support white/black/red/yellow. The 2.13 inch active area contains 250 × 122pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Features

- ◆250×122 pixels display
- ◆High contrast High reflectance
- ◆Ultra wide viewing angle Ultra low power consumption
- ◆Pure reflective mode
- ◆Bi-stable display
- ◆Commercial temperature range
- ◆Landscape portrait modes
- ◆Hard-coat antiglare display surface
- ◆Ultra Low current deep sleep mode
- ◆On chip display RAM
- ◆Waveform can stored in On-chip OTP or written by MCU
- ◆Serial peripheral interface available
- ◆On-chip oscillator
- ◆On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆Built-in temperature sensor

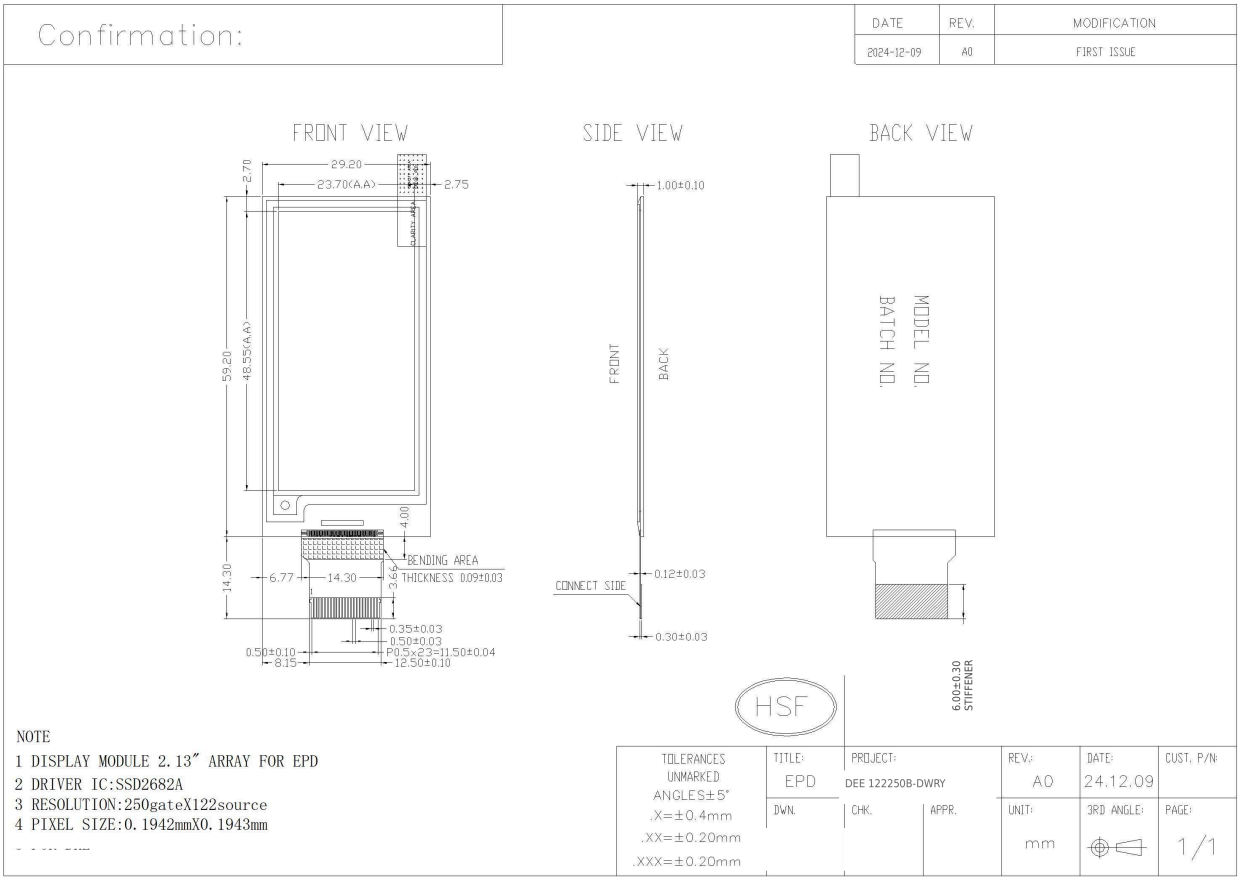
3. Mechanical and Optical Specification

Parameter	Specifications	Unit	Remark
Screen Size	2.13	Inch	
Display Resolution	250(V) ×122(H)	Pixel	DPI:131
Active Area	23.70×48.55	mm	
Pixel Pitch	0.1942×0.1943	mm	
Pixel Configuration	Rectangle		
Outline Dimension	29.20(H)×59.20 (V) ×1.00(D)	mm	
Weight	3.2±0.5g	g	

Temperature Range(℃)		0-9	10-19	20-29	30-40	Units
White State	TYP L*	64	63	63	63	
	MIN L*	62	62	62	62	
	a*	≤0	≤0	≤0	≤0	
	b*	≤2.5	≤2.5	≤2.5	≤2.5	
Black State	TYP L*	9	9	9	9	
	MAX L*	11	11	11	11	
	a*	≤9	≤9	≤8	≤10	
Red State	MIN L*	23	23	24	23	
	TYP a*	36	38	40	40	
	MIN a*	34	34	38	38	
	MAX b*	34	34	34	34	
Yellow State	MIN L*	50	50	54	54	
	TYP b*	55	63	66	66	
	MIN b*	53	56	60	60	
	MAX a*	18	18	18	18	
Ghosting		≤2	≤2	≤2	≤2	delta E

Notes: 3-1. Luminance meter: Eye-One Pro Spectrophotometer.

4. Mechanical Drawing of EPD Module



5. Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	NC		Do not connect with other NC pins	Keep Open
7	NC		Do not connect with other NC pins	Keep Open
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin Low when -Outputting display waveform -Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI,VDDIO	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to V_{DDIO} +0.5	V
Logic Output voltage	VOUT	-0.5 to V_{DDIO} +0.5	V
Operating Temp range	TOPR	0 to+40	ºC.
Storage Temp range	TSTG	-25 to+70	ºC.
Optimal Storage Temp	TSTGo	23±2	ºC.
Optimal StorageHumidity	HSTGo	55±10	%RH

Note:

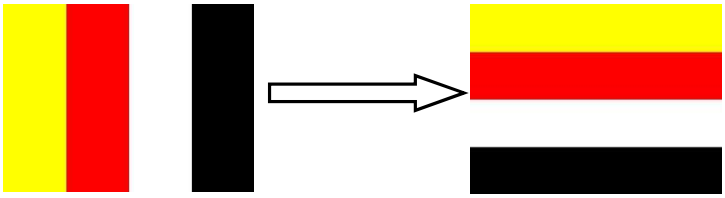
1. Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.
2. The display screen should be kept white and face up during storage. Please refer to the [Reliability Test] section.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{CI}	-	VCI	2.2	3.0	3.6	V
Power for interface logic pins	V_{DDIO}	-	VDDIO	2.2	-	3.6	V
VCOM_DC output voltage	V_{com}	-	VCOM	-3.0	-	-0.2	V
Core logic voltage	V_{DD}		VDD	-	-	-	V
High level input voltage	V_{IH}	-	-	0.8 V_{DDIO}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{DDIO}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.8 V_{DDIO}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.2 V_{DDIO}	V
Typical power	P_{TYP}	V_{CI} =3.0V	-	-	6	-	mW
Deep sleep mode	P_{STPY}	V_{CI} =3.0V	-	-	-	-	mW
Typical operating current	I_{opr_VCI}	V_{CI} =3.0V	-	-	2	-	mA
Image update time	-	23℃	-	-	20	-	Sec
Deep sleep mode current	I_{dslp_VCI}	DC/DC off No clock No input load Ram data not retain	-	-	-	TBD	uA

Notes: 1. The typical power is measured with following transition from horizontal 4 scale pattern to vertical 4 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Supplier.

4. Electrical measurement： Tektronix oscilloscope - MDO3014，

Tektronix current probe – TCP0030A.

6.3 MCU Interface

6.3.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-3-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

Table 6-3-1: MCU interface assignment under different bus interface mode

6.3.2 MCU Serial Interface (4-wire SPI)

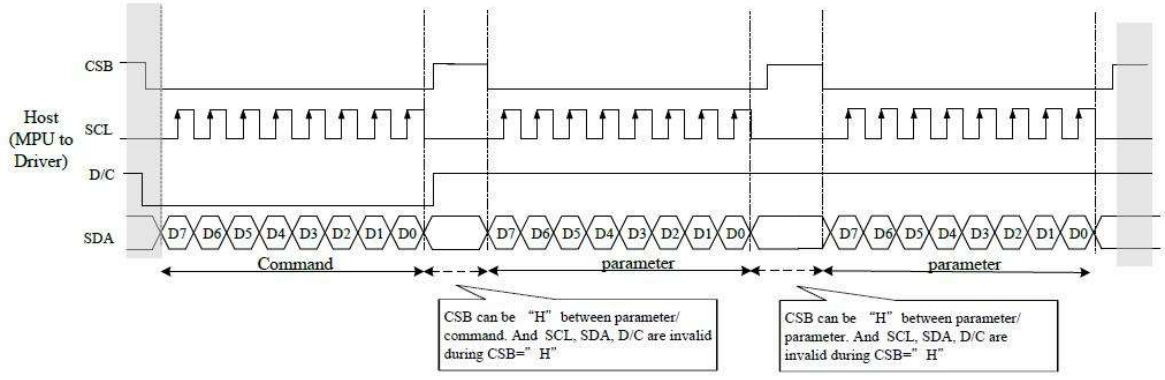
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Table 6-3-2: Control pins of 4-wire Serial Peripheral interface

Note: ↑ stands for rising edge of signal

Figure 6-3-1: 4-wire SPI mode



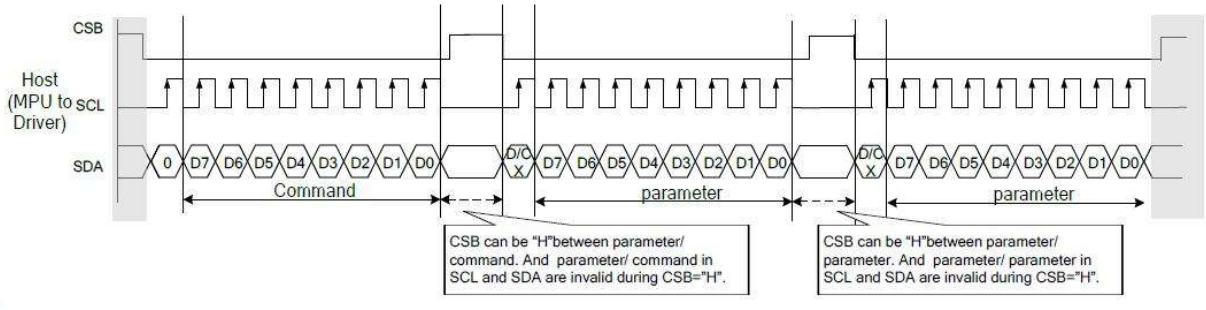
6.3.3 MCU Serial Interface (3-wire SPI)

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

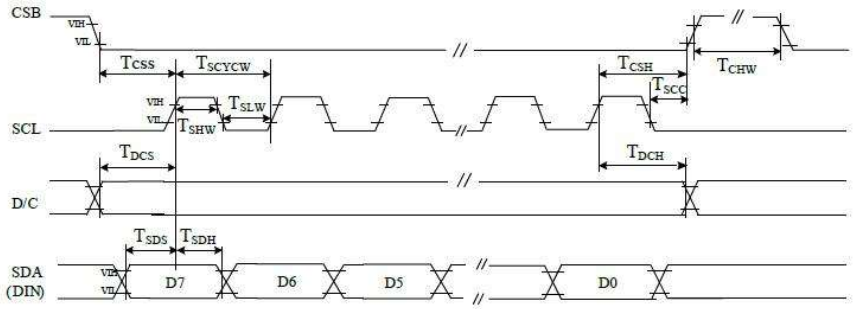
Table 6-3-3: Control pins of 3-wire Serial Peripheral interface

Note：↑ stands for rising edge of signal

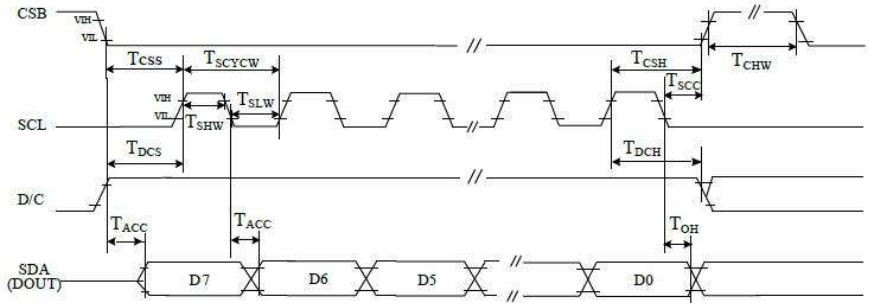
Figure 6-3-2: 3-wire SPI mode



6.3.4 Interface Timing



4 pin serial interface characteristics(write mode)



Serial Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{CSS}	CSB select setup time	TBD			ns
t_{SCH}	CSB select hold time	TBD			ns
t_{SCC}	CSB deselect setup time	TBD			ns
t_{CHW}	CSB deselect hold time	TBD			ns
t_{SCYCW}	Serial clock cycle (Write)	TBD			ns
t_{SHW}	SCL "H" pulse width (Write)	TBD			ns
t_{SLW}	SCL "L" pulse width (Write)	TBD			ns
t_{SCYCL}	Serial clock cycle (Read)	TBD			ns
t_{SHR}	SCL "H" pulse width (Read)	TBD			ns
t_{SLR}	SCL "L" pulse width (Read)	TBD			ns
t_{SDS}	Data setup time	TBD			ns
t_{SDH}	Data hold time	TBD			ns
t_{DCS}	DC setup time	TBD			ns
t_{DCH}	DC hold time	TBD			ns
t_{ACC}	Access time			TBD	ns
t_{OH}	Output disable time	TBD			ns

Note: All timings are based on 20% to 80% of VDDIO-GND

7.Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	00	0	0	0	0	0	0	0	0	PSR	Panel Setting Register A[7:0] = 2Fh [POR] B[7:0] = 09h [POR]
0	1		A_7	A_6	A_5	0	A_3	A_2	A_1	A_0		A[7:6] ~ RES[1:0] Display Resolution setting (source x gate) 00b: 128 x 250 (Default) 01b: 104 x 212 10b: 112 x 208 11b: 128 x 248 *Remark: Inactive Gate outputs will be VGL for DRF and AMV. Inactive Source outputs will follow VCOM LUT output for DRF A[5] ~ B_mode Blanking Mode for voltage switching, the duration setting follow CDI. 0: Mode A Blanking time only for ACVCOM. 1: Mode B (Default) Blanking time for ACVCOM or switch mode of source power. A[3] ~ UD Gate Scan Direction: 0: Scan down. First line to Last line: Gn-1 ... G0 1: Scan up. (Default) First line to Last line: G0 ... Gn-1 A[2] ~ SHL Source Shift Direction: 0: Shift left. First data to Last data: Sn-1 ... S0 1: Shift right. (Default) First data to Last data: S0 ... Sn-1 A[1] ~ SHD_N Booster Switch: 0 : Booster off, register data are kept, and Source/VBD/Vcom are kept 0V or floating. 1 : Booster on. (Default) A[0] ~ RST_N Soft Reset: 0: The controller is reset. Reset all registers to their default value. Driver all function will be disabled. 1: Normal operation (Default). BUSY_N will output low during operation.

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		B[7] ~ LUT_EN 0: During reset, auto load LUT from MTP if it is valid. When PON/DRF, analog setting will follow the content of MTP. (Default) 1: During reset, no action to load LUT from MTP. When PON/DRF, analog setting will follow the content of MCU B[6:5] ~ FOPT[1:0] FOPT function 00b: NO effect. Scan 1 frame after waveform finished (Default) 01b: Will scan 1 frame same as last output (of LUT) after waveform finished. 10b: Will scan 1 frame with Floating output after waveform finished. 11b: No Scan after waveform finished (Power off floating) B[4] ~ VCMZ VCOM Hi-Z option 0: NO effect. (default) 1: VCOM is always floating. B[3] ~ TS_AUTO Temperature Sensor auto option 0: NO effect. 1: Before loading MTP, Temperature Sensor will be activated automatically one time. (default) B[2] ~ TIEG VGL power off option 0: NO effect. (default) 1: After power off booster, VGL will be tied to GND. B[1] ~ NORG VCOM display end GND option 0: NO effect. (default) 1: After refreshing display, VCOM is tied to GND before power off B[0] ~ VC_LUTZ VCOM display end floating option 0: NO effect. 1: After refreshing display, the output of VCOM is set to floating automatically (default)

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>PWR</td><td>Power setting Register
A[5:0] = 07h [POR]
B[7:0] = F0h [POR]
C[6:0] = 00h [POR]
D[6:0] = 00h [POR]
E[6:0] = 00h [POR]
F[6:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>A[2] ~ VSC_EN
Source LV power selection:
0: External source power for VSH2 pin.
1: Internal DCDC function for generate source power. (default)
A[1] ~ VS_EN
Source LV power selection:
0: External source power for VSH1 and VSL pin.
1: Internal DCDC function for generate source power. (default)
A[0] ~ VG_EN
Gate power selection:
0: External gate power for VGH and VGL pin.
1: Internal DCDC function for generate gate power. (default)</td></tr>
<tr><td>0</td><td>1</td><td></td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>B_1</td><td>B_0</td><td></td><td>B[1:0] ~ VGPN [1:0]
Internal VGH / VGL Voltage Level Selection:
<table>
<tr><th>VGPN [1:0]</th><th>Gate Voltage Level</th></tr>
<tr><td>00</td><td>VGH=20V,VGL=-20V (Default)
VSH=15V, VSL=-15V</td></tr>
<tr><td>01</td><td>VGH=17V ,VGL=-17V
VSH=15V, VSL=-15V</td></tr>
<tr><td>10</td><td>VGH=15V,VGL=-15V
VSH=13V, VSL=-13V</td></tr>
<tr><td>11</td><td>Reserved.</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>C_6</td><td>C_5</td><td>C_4</td><td>C_3</td><td>C_2</td><td>C_1</td><td>C_0</td><td></td><td>C[6:0] ~ VSPL [6:0]
Internal Source Voltage Level Selection for VSH2@Mode0:
<table>
<tr><th>VSPL[6:0]</th><th>Voltage Level</th></tr>
<tr><td>00h</td><td>3.0V (default)</td></tr>
<tr><td>02h</td><td>3.2V</td></tr>
<tr><td>04h</td><td>3.4V</td></tr>
<tr><td>06h</td><td>3.6V</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>76h</td><td>14.8V</td></tr>
<tr><td>78h</td><td>15.0V</td></tr>
<tr><td>Other</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>D_6</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td><td>D_1</td><td>D_0</td><td></td><td>D[6:0] ~ VSNL[6:0]
Internal Source Voltage Level Selection for VSL@Mode1:
<table>
<tr><th>VSNL[6:0]</th><th>Voltage Level</th></tr>
<tr><td>00h</td><td>-3.0V (default)</td></tr>
<tr><td>02h</td><td>-3.2V</td></tr>
<tr><td>04h</td><td>-3.4V</td></tr>
<tr><td>06h</td><td>-3.6V</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>76h</td><td>-14.8V</td></tr>
<tr><td>78h</td><td>-15.0V</td></tr>
<tr><td>Other</td><td>Reserved</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>E_6</td><td>E_5</td><td>E_4</td><td>E_3</td><td>E_2</td><td>E_1</td><td>E_0</td><td></td><td>E[6:0] ~ VSPL2[6:0]
Internal Source Voltage Level Selection for VSH1@Mode1:
VSPL2[6:0] | Voltage Level
00h | 3.0V (default)
02h | 3.2V
04h | 3.4V
06h | 3.6V
: | :
76h | 14.8V
78h | 15.0V
Other | Reserved</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>F_6</td><td>F_5</td><td>F_4</td><td>F_3</td><td>F_2</td><td>F_1</td><td>F_0</td><td></td><td>F[6:0] ~ VSNL2[6:0]
Internal Source Voltage Level Selection for VSH2@Mode1:
VSNL2[6:0] | Voltage Level
00h | 3.0V (default)
02h | 3.2V
04h | 3.4V
06h | 3.6V
: | :
76h | 14.8V
78h | 15.0V
Other | Reserved</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>02</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>POF</td><td>Power OFF Command Register</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td><td>After power off command, driver will power off based on the Power OFF Sequence.
BUSY_N will output low during operation.
The Power OFF command will turn off DCDC, source driver, gate driver, VCOM driver, temperature sensor, but register and SRAM data will keep until VDD off.
SD output will base on previous condition.
*Remark: POF works at PON only</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>POFS</td><td>Power on/off Sequence Setting Register
A[7:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>A_5</td><td>A_4</td><td>0</td><td>0</td><td>A_1</td><td>A_0</td><td></td><td>A[5:4] ~ T_VDPG_OFF[1:0]
Power off delay from VGL to VGH
00b: 20ms (default)
01b: 40ms
10b: 60ms
11b: 80ms

A[1:0] ~ T_VDS_OFF[1:0]
Power off delay from VSHX/VSL to VGH
00b: 20ms (default)
01b: 40ms
10b: 60ms
11b : 80ms</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>04</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>PON</td><td>Power ON Command Register
After the Power ON command, driver will power on based on the Power ON Sequence.
BUSY_N will output low during operation.

* Remark:
PON include booster on, VSHx/VSLx regulator on
With default BTST, timing is >80ms</td></tr>
<tr><td colspan="13"></td></tr>
</table>

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	06	0	0	0	0	0	1	1	0	BTST	VGH Booster Soft Start Setting Register (for VGH) A[6:0] = 0Fh [POR] B[6:0] = 8Bh [POR] C[6:0] = 9Ch [POR] D[6:0] = 96h [POR]
0	1		0	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[6:4] ~ VGHSSC_ONT [2:0] VGH booster maximum MOSFET ON time (reserved) A[6:4] = 000 (Default) A[3:2] ~ T_VGHSSA [1:0] = 11 (Default) VGH booster soft start Phase A duration A[1:0] ~ T_VGHSSB [1:0] = 11 (Default) VGH booster soft start Phase B duration
0	1		1	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		1	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		1	D_6	D_5	D_4	D_3	D_2	D_1	D_0		

	Soft Start Phase Period (ms)
00	10
01	20
10	30
11	40

B[6:4] ~ VGHSSA_DRV [2:0], = 000 (Default)
VGH Phase A Driving Strength
C[6:4] ~ VGHSSB_DRV [2:0], = 001 (Default)
VGH Phase B Driving Strength
D[6:4] ~ VGHSSC_DRV [2:0] = 001 (Default)
VGH Phase C Driving Strength

Driving Strength			
000	0	100	(reserved)
001	1	101	(reserved)
010	2	110	(reserved)
011	3(strongest)	111	(reserved)

B[3:0] ~ VGHSSA_OFFT[[3:0], = 1011 (Default)
VGH Phase A Minimum OFF Time
C[3:0] ~ VGHSSB_OFFT[[3:0], = 1100 (Default)
VGH Phase B Minimum OFF Time
D[3:0] ~ VGHSSC_OFFT[[3:0], = 0110 (Default)
VGH Phase C Minimum OFF Time

Minimum OFF Time (setting)			
0000	OFFH0	1000	OFFH8
0001	OFFH1	1001	OFFH9
0010	OFFH2	1010	OFFHA
0011	OFFH3	1011	OFFHB
0100	OFFH4	1100	OFFHC
0101	OFFH5	1101	OFFHD
0110	OFFH6	1110	OFFHE
0111	OFFH7	1111	OFFHF

0	0	07	0	0	0	0	0	1	1	1	DSLP	Deep Sleep Register
0	1		1	0	1	0	0	1	0	1		This command makes the chip enter the deep-sleep mode. The deep sleep mode could return to stand-by mode by hardware reset assertion. The only one parameter is a check code, the command would be executed if check code is A5h.

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>DTM</td><td>Data Start transmission Register</td></tr>
<tr><td colspan="10">2 bit per pixel
0 1 KPixel1 [1:0] KPixel2 [1:0] KPixel3 [1:0] KPixel4 [1:0]
:
0 1 KPixel (4M-3) [1:0] KPixel (4M-2) [1:0] KPixel (4M-1) [1:0] KPixel (4M) [1:0]</td><td></td><td>This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command (R12H). Then the chip will start to send data/VCOM for panel.

KPixel[1:0] Source Driver Output
00b: DDX=1 (Default) Gray 0; DDX=0 Gray 3
01b: Gray 1; Gray 2
10b: Gray 2; Gray 1
11b: Gray 3; Gray 0

After issue this command, the host must send at least 1-byte data to the device.</td></tr>
<tr><td>0</td><td>0</td><td>12</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>DRF</td><td>Display Refresh Command Register</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td><td>After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT.
BUSY_N will output low during operation.</td></tr>
<tr><td>0</td><td>0</td><td>17</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>AUTO</td><td>Auto Sequence Register</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td>This command makes the chip enter the auto sequence
Single-chip application ONLY.
Auto Sequence Option
0xA5: Start Auto Sequence (PON > DRF > POF)
0xA7: Start Auto Sequence (PON > DRF > POF > DSLP).
Others: No effect
BUSY_N will output low during operation.</td></tr>
<tr><td>0</td><td>0</td><td>30</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>PLL</td><td>Frame Rate Control register
The command controls the clock frequency.
A[2:0] = 2h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td>A[3] ~ Dyna
Dynamic Frame Rate
0: Disable (Default)
1: Enable

A[2:0] ~ FR[2:0]
It supports the following frame rates.
Frame Rate Selection, Frame rate for Gate/Source switching that exclude the blanking time defined in CDI.
FR[2:0]: 000 12.5Hz; 001 25Hz; 010 50Hz (Default); 011 65Hz; 100 75Hz; 101 85Hz; 110 100Hz; 111 120Hz</td></tr>
</table>

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	40	0	1	0	0	0	0	0	0	TSC	Temperature Sensor Command Register
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		This command enables internal temperature sensor. BUSY_N will output low during operation. Then the temperature value can be read in 1degC step A[7:0] ~ TS [7:0]

TS [7:0]	Return Value(degC)
E7h	-25
...	...
FFh	-1
00h	0
01h	1
...	...
19h	25
...	...
31h	49
32h	50

0	0	41	0	1	0	0	0	0	0	1	TSE	Temperature Sensor Enable Register This command selects Temperature offset A[7:0] = 00h [POR]
0	1		0	0	0	0	A_3	A_2	A_1	0		A[3:0] ~ TO[3:1], Temperature offset:

TO[3:1]	Calculation	TO[3:1]	Calculation
000	+0	100	-4
001	+1	101	-3
010	+2	110	-2
011	+3	111	-1

0	0	50	0	1	0	1	0	0	0	0	CDI	VCOM and DATA interval setting Register This command indicates the Border Output Selection and the interval between Vcom and data output A[7:0] = 97h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:5]~VBD [2:0] Border Output Selection:

	DDX=1	DDX=0
VBD[2:0]	LUT (Default)	LUT
000	Gray 0	HIZ
001	Gray 1	Gray 3
010	Gray 2	Gray 2
011	Gray 3	Gray 1
100	HIZ(Default)	Gray 0

A[4]: DDX
Data Polarity for Pixel Data (See DTM command)
0: Invert
1: Non-invert (Default)
A[3:0] ~ CDI[3:0]
Gate and source blanking time (No gate source scanning)

CDI [3:0]	Interval (ms)	CDI [3:0]	Interval (ms)
0h	2	8h	40
1h	4	9h	60
2h	8	Ah	80
3h	12	Bh	100
4h	14	Ch	120
5h	16	Dh	140
6h	18	Eh	160
7h	20 (Default)	Fh	Reserved

User needs to review CDI setting to have stable VCOM in application

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	51	0	1	0	1	0	0	0	1	LPD	Lower Power Detection Register
1	1		0	0	0	0	0	0	0	A_0		BUSY_N will output low during operation. Then the LPD status can be read. A[0] ~ LPD status 0: Low power input VDD<2.5V, selected by LVD_SEL[1:0] in command LVSEL 1: Normal (default)
0	0	61	0	1	1	0	0	0	0	1	TRES	Resolution setting Register A[9:0] = 080h [POR] B[9:0] = 0FAh [POR]
0	1		0	0	0	0	0	0	A_9	A_8		This command defines alternative resolution A[9:8]=00b, A[7:0] ~ HRES[7:0] Horizontal Display Resolution Remark: Horizontal resolution should be 4-multiple. B[9:8]=00b, B[7:0] ~ VRES[7:0] Vertical Display Resolution e.g. HRES= 80h, VRES= FAh
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	B_9	B_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	65	0	1	1	0	0	1	0	1	GSST	Gate/Source Start Setting Register. A[9:0] = 000h [POR] B[9:0] = 000h [POR]
0	1		0	0	0	0	0	0	A_9	A_8		A[9:8]=00b, A[7:0] ~ S_start[7:0] First valid source output channel setting
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	B_9	B_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		

UD,SHL	Source and gate sequence
00	S127,G249 to S0,G0
01	S0, G249 to S127,G0
10	S127,G0 to S0, G249
11	S0,G0 to S127, G249

Remark:
1) Both PSR.RES & TRES command can set panel resolution. Priority will be given to the last received PSR or TRES command.
2) VRES[7:0] >= 152

S_start [7:0]	First valid source output
00h	S0 (Default)
04h	S4
08h	S8
...	...
78h	S120
7Ch	S124
Other	Reserved

B[9:8]=00b, B[7:0] ~ G_start[7:0]
First valid gate output channel setting

GSST and TRES can define the display window from target source and gate start and end line.
GD: First G active = G16, G_start[7:0]=16.
Last G active = G233, VRES[7:0]=218.
SD: First S active = S8, S_start[7:0]=8.
Last S active = S119, HRES[7:0]=112.

Remark:
1) PSR.RES[1:0] = 00
2) G_start+VRES< 250, S_start+HRES< 128.

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	70	0	1	1	1	0	0	0	0	REV	Chip Revision Register The command is to read the ID A[7:0] = C9h [POR] B[7:0] = 01h [POR] C[7:0] = 01h [POR]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	80	1	0	0	0	0	0	0	0	AMV	Auto Measurement VCOM Register This command implements related VCOM sensing setting. A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	0	A_0		A[7:6] ~ P[1:0] Number of sensing Points 00: 2 (Default) 01: 4 10: 8 11: 16 A[5:4] ~ AMVT[1:0] Auto Measure Vcom Time: Sensing Time 00: 5 sec. (Default) 01: 10 sec. 10: 15 sec. 11: 20 sec. A[3] ~ AMVX VCOM measurement Gate settings 0: Gate scan normally during VCOM measurement (Default) 1: All Gates ON during VCOM measurement A[2] ~ AMVS Source output of AMV: 0: Set Source output to 0V during Auto Measure VCOM period. (Default) 1: Set Source output to VSH_LV during Auto Measure VCOM period. A[0] ~ AMVE Auto Measure Vcom Enable (/Disable): 0: Disabled (Default) 1: Enabled BUSY_N will output low during operation. Requirement: AMV works at PON only
0	0	81	1	0	0	0	0	0	0	1	VV	Auto Measurement VCOM Register This command gets the Vcom value after AMV.
1	1		1	0	A_5	A_4	A_3	A_2	A_1	A_0		A[5:0] ~ VV[5:0]: Vcom read Value, valid range from -0.2V to -3.0V.

VV[5:0]	Vcom read value
00h	Reserved
04h	-0.2V
08h	-0.4V
0Ch	-0.6V
10h	-0.8V
...	...
3Ch	-3.0V
others	Reserved

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	82	1	0	0	0	0	0	1	0	VDCS	VCM_DC Setting Register This command sets VCOM_DC value. A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	0	0		A[7] ~ MTP_VCM Vcom follow VDCS after RESET. 0: Disable (Default), auto load from MTP if it is valid. 1: Enable, VCOM value from the VDCS[6:0] A[6:0] ~ VDCS[6:0]: VCOM_DC Setting, 0.2V step from -0.2V to -3V.

VDCS [6:0]	VCOM_DC Setting
00h	Reserved
04h	-0.2V
08h	-0.4V
0Ch	-0.6V
10h	-0.8V
...	...
3Ch	-3.0V
others	Reserved

0	0	83	1	0	0	0	0	0	1	1	PTLW	PARTIAL WINDOW This command sets partial window address. A[9:0] = 000h [POR] B[9:0] = 07Fh [POR] C[9:0] = 000h [POR] D[9:0] = 0F 9h [POR] E[7:0] = 00h [POR]
0	1		0	0	0	0	0	0	A_9	A_8		A[9:8]=00b, A[7:0] ~ HRST [7:0] Horizontal start address
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	B_9	B_8		B[9:8]=00b, B[7:0] ~ HRED [7:0] Horizontal end address
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	C_9	C_8		C[9:8]=00b, C[7:0] ~ VRST [7:0] Vertical start address
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		0	0	0	0	0	0	D_9	D_8		D[9:8]=00b, D[7:0] ~ VRED [7:0] Vertical end address
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		0	0	0	0	0	0	0	E_0		E[0] ~ PMODE 0: disable partial mode (Default) 1: enable partial mode Gate scan both inside and outside of the partial window Note: 1) HRST [7:0]<= HRED [7:0] 2) VRST [7:0]<= VRED [7:0]
0	0	90	1	0	0	1	0	0	0	0	PGM	Program Mode This command is to set MTP program mode After this command is issued, the chip would enter the program mode. After the programming procedure completed, a hardware reset is necessary for leave the program mode BUSY_N will output low until PGM mode is ready.

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	91	1	0	0	1	0	0	0	1	APG	Active Program This command is to execute MTP program After this command is issued, the chip would program the MTP. BUSY_N will output low during operation. Requirement: In PON mode with internal programming power.
0	0	92	1	0	0	1	0	0	1	0	RMTP	Read MTP Data
1	1		1st ~ dummy 2nd ~ N+1th Parameter									This command is to read the MTP content from SRAM. The 1st byte read is dummy byte. The 2nd byte read is the content of Address 0 in MTP The N+1th byte read is the content of Address n in MTP After issue this command, the host must read at least 1 byte data from the device.
0	0	E0	1	1	1	0	0	0	0	0	CCSET	CCSET for temperature input selection A[7:0] = 00h [POR]
0	1		0	0	0	0	0	0	A_1	0		A[1] = TSFIX Temperature Input selection 0: Use Internal Temperature sensor (Default) 1: Use TSSET[7:0] value
0	0	E3	1	1	1	0	0	0	1	1	PWS	Power Saving Register This command is sets for saving power VCOM/Source power saving during display refresh period. A[7:0] = 65h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		If the output voltage of VCOM/Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters. A[7:4] = VCOM_W[3:0]

VCOM_W [3:0]	VCOM_power saving width. (time unit)	VCOM_W [3:0]	VCOM_power saving width. (time unit)
0	Reserved	8	8
1	1	9	9
2	2	10	10
3	3	11	11
4	4	12	12
5	5	13	13
6	6 [Default]	14	14
7	7	15	15

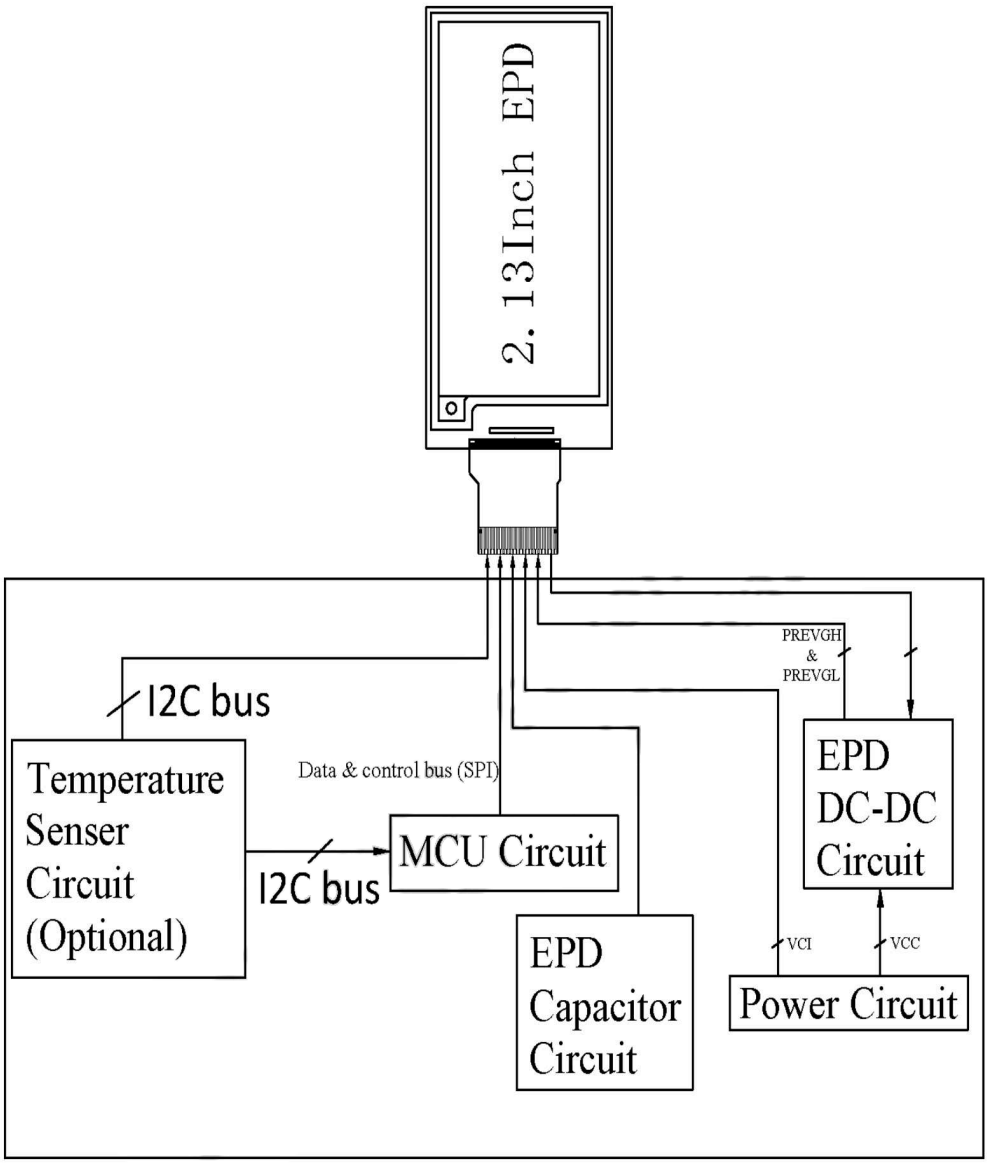
A[3:0] = SD_W[3:0]

SD_W [3:0]	Source power saving width[us]	SD_W [3:0]	Source power saving width [us]
0	Reserved	8	4
1	0.5	9	4.5
2	1	10	5
3	1.5	11	5.5
4	2	12	6
5	2.5[Default]	13	6.5
6	3	14	7
7	3.5	15	7.5

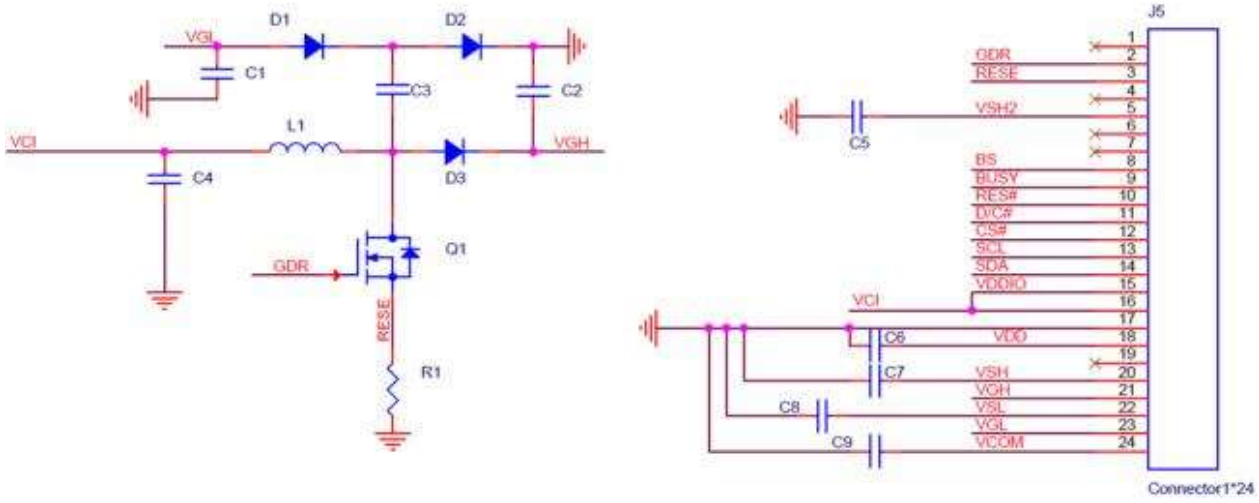
Remark:
VCOM_W setting < CDI setting
SD_W setting < S2G setting

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>E4</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>LVSEL</td><td>LVD Voltage Select Register
This command is sets for low power detect level power
A[1:0] = 3h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_1</td><td>A_0</td><td></td><td>A[1:0] ~ LVD_SEL[1:0]
Low power detection threshold
00: 2.2V
01: 2.3V
10: 2.4V
11 : 2.5V (Default)</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>E6</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>TSSET</td><td>Manual input temperature value
This command is to force the TS value
A[7:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>A[7:0] ~ TS_SET[7:0]
When TSFIX=1, Temperature value will be set by TS_SET[7:0].
Format of the temperature value is 8-bit binary value and it is 1degC per step.
<table>
<tr><th>TS_SET[7:0]</th><th>Force the TS Value(degC)</th></tr>
<tr><td>E7h</td><td>-25</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>FFh</td><td>-1</td></tr>
<tr><td>00h</td><td>0</td></tr>
<tr><td>01h</td><td>1</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>19h</td><td>25</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>31h</td><td>49</td></tr>
<tr><td>32h</td><td>50</td></tr>
</table></td></tr>
</table>

8. Block Diagram



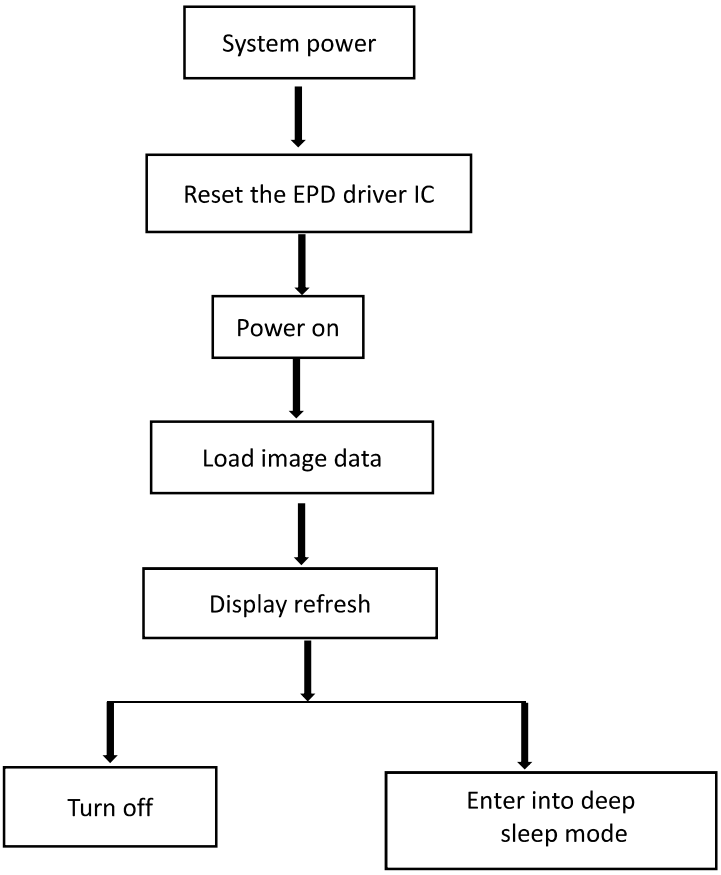
9. Typical Application Circuit with SPI Interface



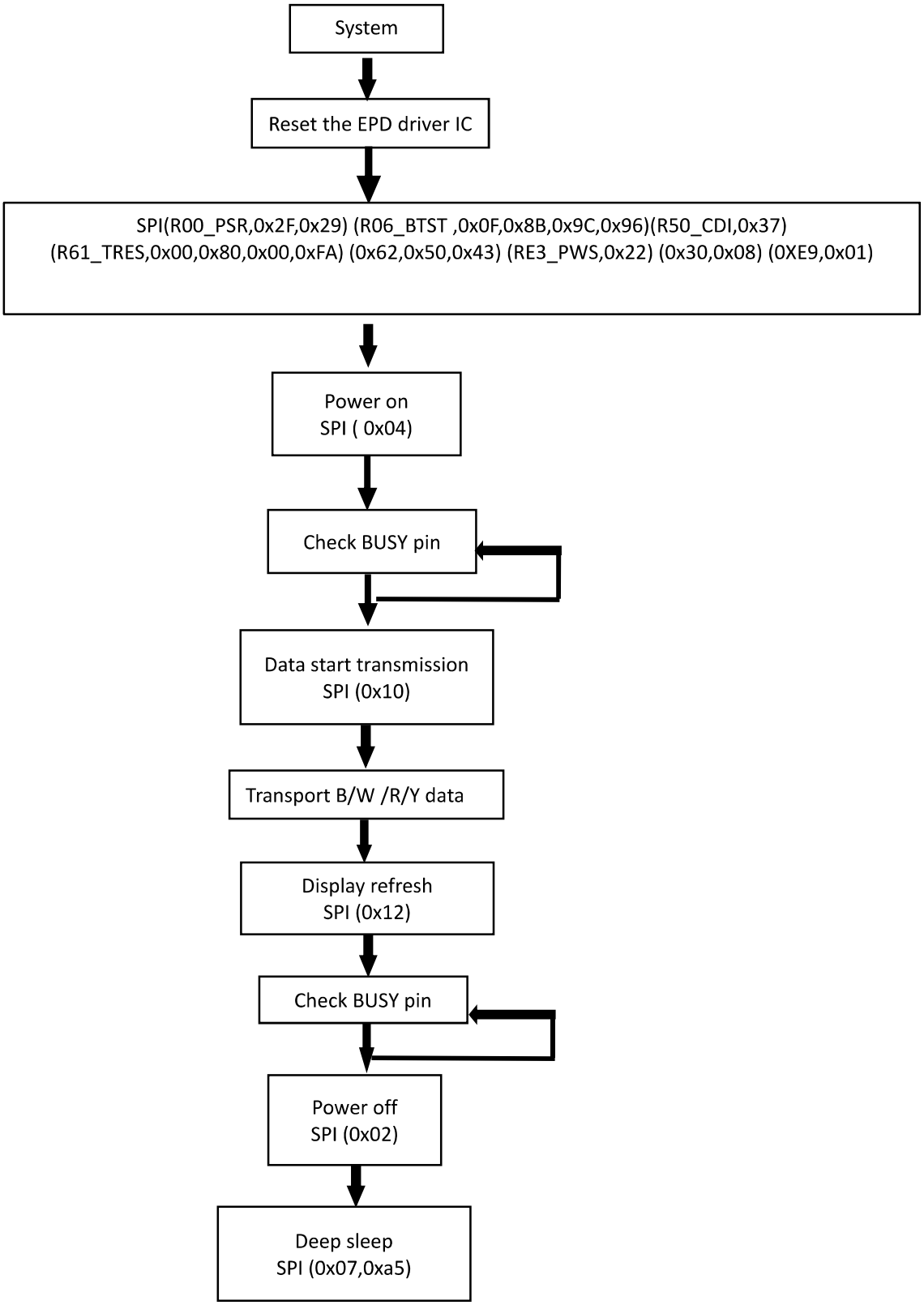
Part Name	Value	Reference Part
C1 C2 C3 C5 C7 C8	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
C6 C4	1uF	X5R/X7R; Voltage Rating : 6V or 25V
C9	0.47uF, 1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
R1	2.2Ω	0402/0603/0805; 1% variation, ≥0.05W
D1 D2 D3	Diode	MBR0530 1) Reverse DC voltage ≥ 30V 2) Io ≥500mA 3) Forward voltage ≤ 430mV
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage ≤ 30V 2) Vgs(th) = 0.9V (Typ), 1.3V (Max) 3) Rds on ≤ 2.1Ω @ Vgs = 2.5V
L1	47UH	CDRH2D18 / LDNP-470NC Io= 500mA (Max)

10 Typical Operating Sequence

10.1 LUT from OTP Operation Flow



10.2 OTP Operation Reference Program Code



11. Reliability Test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C，500 h Test in white pattern
2	High-Temperature Storage	T=60ºC，RH=35%，500h Test in white pattern
3	High-Temperature Operation	T=40ºC，RH=35%， 500h
4	Low-Temperature Operation	0ºC，500h
5	High-Temperature, High-Humidity Operation	T=40ºC，RH=80%，500h
6	High-Temperature, High-Humidity Storage	T=60ºC，RH=80%，500h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+60 °C 30 min] : 100 cycles Test in white pattern
8	ESD Gun	Air+/-4KV;Contact+/-2KV Contact+/-2KV(HBMC:100pF;R:1.5k ohm) Contact+/-200V(MMC:200pF;R:0 ohm) (Naked EPD display,including IC and FPC area)
9	Vibration test	Frequency: 10-500Hz Direction: X, Y, Z Duration: 1 hour in each direction
10	Dropping test	The test height is determined by the weight of the test object. Weight ≤20KG, drop height 1000mm Weight ≤50KG, drop height 500mm Weight ≤100KG, drop height 250mm

Note：1. Stay white pattern for storage and non-operation test.

2. Operation is black→white→red→yellow pattern, the interval is 150s.

3. Put in 20℃--25℃ for 1hour after test finished, The function ,appearance and display performance is OK.

12.Quality Assurance

12.1 Environment

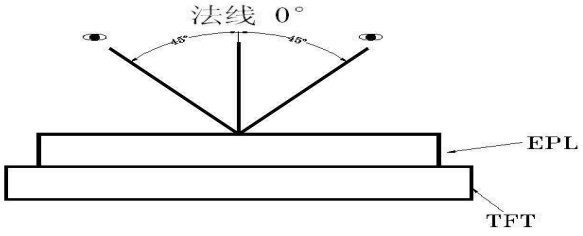
Temperature： 23±3℃

Humidity： 55±10%RH

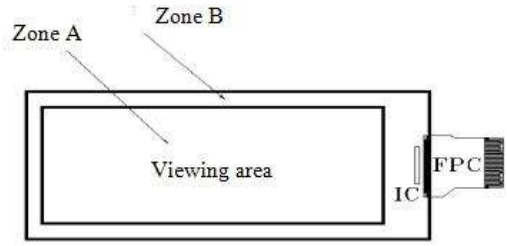
12.2 Illuminance

Brightness:1200～1500LUX;distance:20-30CM;Angle:Relate 45°surround.

12.3 Inspect method

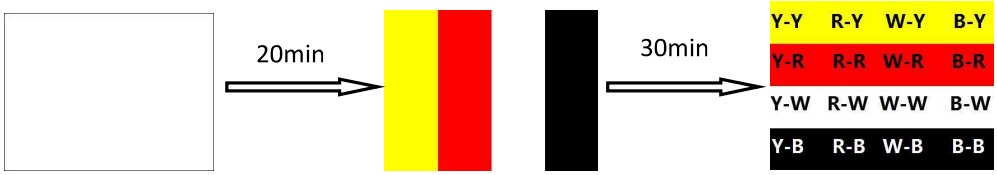


12.4 Display area



12.5 Ghosting test method

Four-color ghosting is measured with following transition from horizontal 4 scale pattern to vertical 4 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by Supplier.



1）Measurement Instruments：X-rite i1Pro

2）Ghosting formula:

W ghosting：△E= Max (Δ Eab(Y-W, R-W), Δ Eab(Y-W, W-W), Δ Eab(Y-W, B-W), Δ Eab(R-W, W-W), Δ Eab(R-W, B-W), Δ Eab(W-W, B-W))

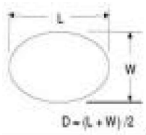
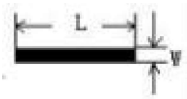
K ghosting：△E= Max (Δ Eab(Y-B, R-B), Δ Eab(Y-B, W-B), Δ Eab(Y-B, B-B), Δ Eab(R-B, W-B), Δ Eab(R-B, B-B), Δ Eab(W-B, B-B))

R ghosting：△E= Max (Δ Eab(Y-R, R-R), Δ Eab(Y-R, W-R), Δ Eab(Y-R, B-R), Δ Eab(R-R, W-R), Δ Eab(R-R, B-R), Δ Eab(W-R, B-R))

Y ghosting：△E= Max (Δ Eab(Y-Y, R-Y), Δ Eab(Y-Y, W-Y), Δ Eab(Y-Y, B-Y), Δ Eab(R-Y, W-Y), Δ Eab(R-Y, B-Y), Δ Eab(W-Y, B-Y))

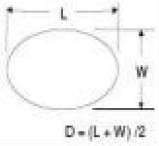
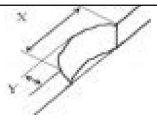
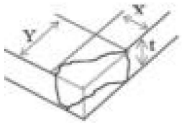
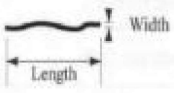
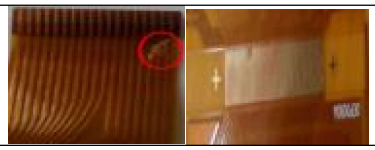
12.6 Inspection standard

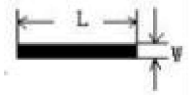
12.6.1 Electric inspection standard

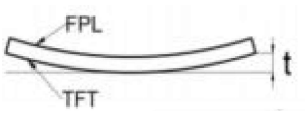
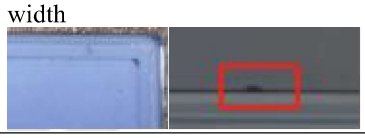
NO.	Item	Standard	Defect level	Method	Scope
1	Display	Display complete Display uniform	MA	Visual inspection	Zone A
2	Black/White spots	 D≤0.25mm，Allowed 0.25mm＜D≤0.4mm。 N≤4 allowable D＞0.4mm is not allowed	MI	Visual Inspection card	Zone A
3	Show B/W lines	 L≤0.4mm,W≤0.1mm negligible 0.4mm＜L≤1.0mm 0.1mm＜W≤0.4mm N≤4 allowable L＞1.0mm ,W＞0.4mm is not allowed	MI	Visual Inspection card	Zone A
4	Ghost image	Allowed in switching process	MI	Visual	Zone A
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection card	Zone A
7	Short circuit/ Circuit break/ Display abnormal	Not Allow	MA	Visual	Zone A

8	Corner mura	X>1mm， Y>1mm,not allow 	MI	Visual/Ruler	Zone A

12.6.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 D≤0.25mm negligible 0.25mm＜D≤0.4mm N≤4 allowable D＞0.4mm is not allowed	MI	Visual/ inspection Card	Zone A
2	Chips/Scratch/ Edge crown	 X≤3mm,Y≤0.5mm t= not counted，and without affecting the electrode , permissible  2mm≤X or 2mm≤Y t= not counted.and without affecting the electrode , permissible  W≤0.1mm,L≤5mm, without affecting the electrode , n≤2	MI	Visual / Ruler	Zone A/B
3	TFT Cracks	Not Allow 	MA	Visual / Microscope	Zone A/B
4	Dirty/ foreign body	Allowed if can be removed	MI	Visual / clean cloth	Zone A / B
5	FPC broken/ Goldfingers oxidation/ scratch		MA	Visual / Microscope	Zone B

		Not Allow			
6	B/W Line	 L≤0.4mm,W≤0.1mm negligible 0.4mm＜L≤1.0mm 0.1mm＜W≤0.4mm N≤4 allowable L＞1.0mm ,W＞0.4mm is not allowed	MI	Visual / Ruler	Zone A
7	TFT edge bulge /TFT chromatic aberration	 TFT edge bulge： X≤3mm，Y≤0.3mm Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A/B
8	Electrostatic point	D≤0.2mm, allow 0.2mm＜D≤0.35mm ,n≤4 allow D＞0.35mm is not allowed (n≤5 items are allowed within 5 mm in diameter)	MI	Visual /inspection card	Zone A
9	PCB damaged/ Poor welding/ Curl	PCB（Circuit area）damaged Not Allow PCB Poor welding Not Allow PCB Curl≤1%	MA	Visual / Ruler	Zone B

10	Edge glue height/ Edge glue bubble	Edge Adhesives H≤PS surface (Including protect film) Edge adhesives overflow onto protect film ≤1/2 FPL to PS Margin width Length excluding Edge adhesives seep in≤1/2 FPL Margin width Length excluding Edge adhesives bubble：bubble Width ≤1/2 Margin width；Length ≤5.0mm。n≤5	MI	Visual / Ruler	Zone B
11	Protect film	Surface scratch but not effect protect function, Allowed	MI	Visual	Zone A/B
12	Silicon glue	Thickness≤PS surface(With protect film): Full cover the IC; Shape: The width on the FPC≤1.0mm (Front) The width on the FPC≤1.0mm (Back) smooth surface, No obvious raised.	MI	Visual/Ruler	Zone B
13	Warp degree (TFT substrate)	 t≤1.0mm	MI	Ruler	Zone B
14	Color difference in COM area (Silver point area)	Allowed	MI	Visual	Zone B
15	Corner and edge damage of FPL	Corner and edge damage ≤ 1/2 border width 	MI	Visual / Ruler	Zone A

13. Handling, Safety, and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
Product Environmental certification	
ROHS	
REMARK	
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.	
Transport environment	
When the humidity of transportation environment is between 45%RH~70%RH, the product can be stored for 30 days, and the product can be stored for 10 days if it is lower or higher than this range	