DISPLAY Elektronik GmbH

DATA SHEET

PRODUCT SPECIFICATION

EPD MODULE

DEE 122250B-DW-H

2.13"

E-Paper Display

PRODUCT SPECIFICATION Ver.: 2.0

15.05.2025

Version	Content	Date	Producer
2.0	New release	15.05.2025	MH-AI

CONTENTS

1. Over View 4
2. Features 4
3. Mechanical and Optical Specification 5
4. Mechanical Drawing of EPD Module 6
5. Input/output Pin Assignment 7
6. Electrical Characteristics 9
6.1 Absolute Maximum Rating 9
6.2 Panel DC Characteristics 10
6.3 Panel AC Characteristics 11
6.4 MCU Interface 12
6.4.1 MCU Interface Selection 12
6.4.2 MCU Serial Interface (4-wire SPI) 12
6.4.3 MCU Serial Interface (3-wire SPI) 14
6.4.4 Interface Timing 15
7. Command Table 17
8. Block Diagram 31
9. Typical Application Circuit with SPI Interface 32
10. Typical Operating Sequence 33
10.1 LUT from OTP Operation Flow 33
10.2 LUT from OTP Operation Reference Program Code 34
11. Reliability Test 35
12. Quality Assurance 36
12.1 Environment 36
12.2 Illuminance 36
12.3 Inspect method 36
12.4 Display area 36
12.5 Ghosting test method 36
12.6 Inspection standard 37
12.6.1 Electric inspection standard 37
12.6.2 Appearance inspection standard 38
13. Handling, Safety, and Environment Requirements 40

1. Over View

DEE 122250B-DW-H is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white and black full display capabilities.The 2.13 inch active area contains 122 x 250 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Features

◆122 x 250 pixels display

◆High contrast High reflectance

◆Ultra wide viewing angle Ultra low power consumption

◆Pure reflective mode

◆Bi-stable display

◆Commercial temperature range

◆Landscape portrait modes

◆Hard-coat antiglare display surface

◆Ultra Low current deep sleep mode

◆On chip display RAM

◆Waveform can stored in On-chip OTP or written by MCU

◆Serial peripheral interface available

◆On-chip oscillator

◆On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage

◆I^2C signal master interface to read external temperature sensor

◆Built-in temperature sensor

3.Mechanical and Optical Specification

Parameter	Specifications	Unit	Remark
Screen Size	2.13	Inch	
Display Resolution	122(H)×250(V)	Pixel	DPI:130
Active Area	23.70×48.55	mm	
Pixel Pitch	0.1942×0.1942	mm	
Pixel Configuration	Rectangle		
Outline Dimension	29.2(H)×59.2(V) ×1.0(D)	mm	
Weight	3.2±0.5	g	

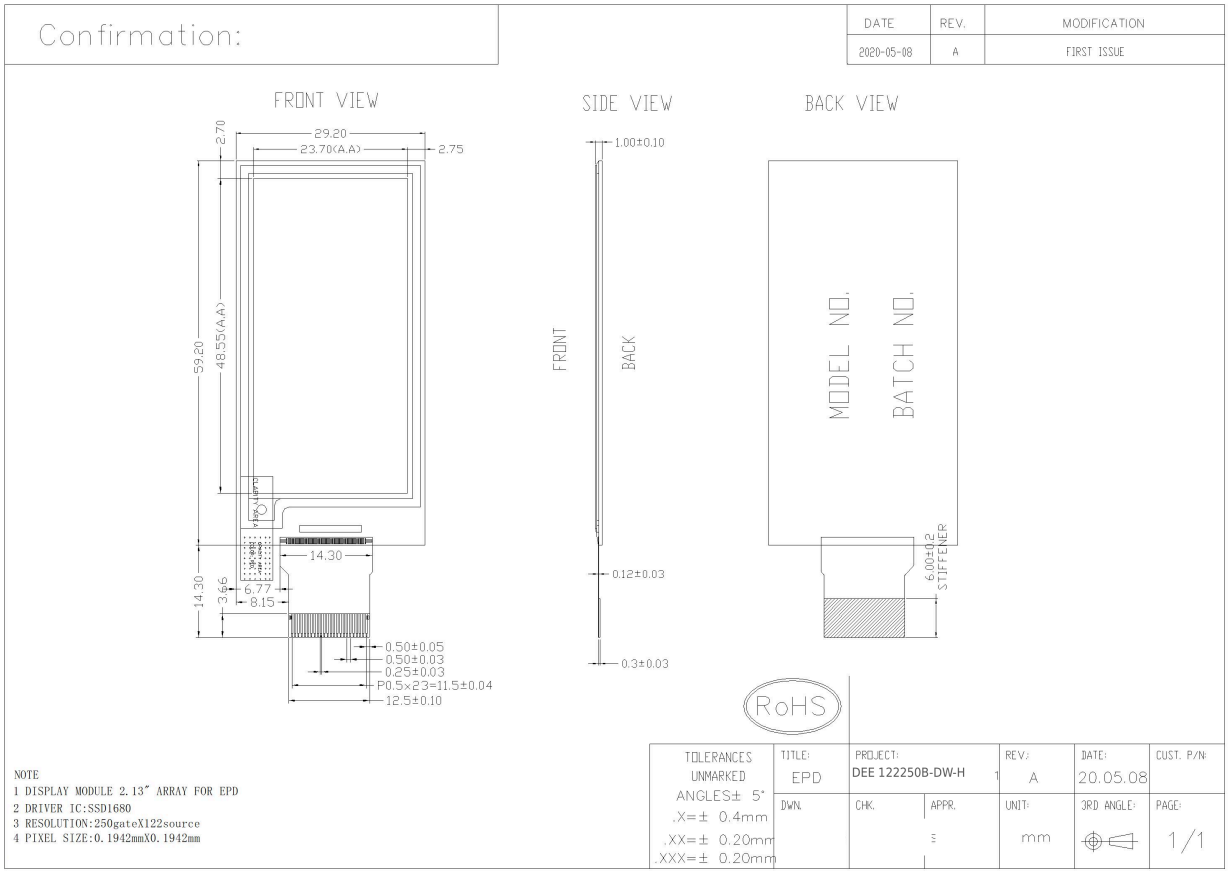
Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
KS	Black State L* value	-20~60°C	-	18	-		3-1
	Black Ghosting ΔL	0~50°C	-	-	1		3-1
	Black Ghosting ΔL	-20~0°C&50~60°C	-	-	2		3-1
WS	White State L* value	0~50°C	65	67	-		3-1
	White State L* value	-20~0°C&50~60°C	62	-	-		3-1
	White Ghosting ΔL	0~50°C	-	-	1		3-1
	White Ghosting ΔL	-20~0°C&50~60°C	-	-	2		3-1
CR	Contrast Ratio	Indoor	13:1	15:1	-		3-1 3-2
GN	2Grey Level	-	-	-	-		
Life		Temp:23±3°C Humidity:55±10%RH		5years			3-3

Notes: 3-1. Luminance meter: Eye-One Pro Spectrophotometer.

3-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

3-3. When the product is stored. The display screen should be kept white and face up.

4.Mechanical Drawing of EPD Module



5.Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage 2	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	Note 5-6
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	Note 5-6
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when -Outputting display waveform -Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

Note 5-6: This pin connect to the VSS if there is no external temperature sensor.

External pull up resistor is required when connecting to I2C slave.

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI,VDDIO	-0.5 to +6.0	V
Logic Input voltage	VIN	-0.5 to V_{DDIO} +0.5	V
Logic Output voltage	VOUT	-0.5 to V_{DDIO} +0.5	V
Operating Temp range	TOPR	-20 to +60	ºC.
Storage Temp range	TSTG	-25 to+70	ºC.
Optimal Storage Temp	TSTGo	23±2	ºC.
Optimal Storage Humidity	HSTGo	55±10	%RH

Note:

1． Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

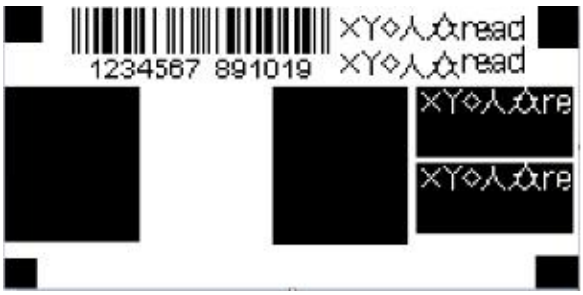
2． The display screen should be kept white and face up during storage. Please refer to the [Reliability Test] section.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR = 23ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{CI}	-	VCI	2.2	3.0	3.7	V
Power for interface logic pins	V_{DDIO}		VDDIO	2.2	-	3.7	V
	Core logic voltage	V_{DD}		VDD	-	-	-	V
VCOM_DC output voltage	V_{com}	-	VCOM	-3.0	-	-0.2	V
High level input voltage	V_{IH}	-	-	0.8 V_{DDIO}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{DDIO}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.9 V_{DDIO}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.1 V_{DDIO}	V
Typical power	P_{TYP}	V_{CI} =3.0V	-	-	12	-	mW
Deep sleep mode	P_{STPY}	V_{CI} =3.0V	-	-	0.0009	-	mW
Typical operating current	Iopr_VCI	V_{CI} =3.0V	-	-	4	-	mA
Image update time	-	23 ºC	-	-	4	-	sec
Typical peak current	Iopr_VCI	2.3~3.6v			30	-	mA
Deep sleep mode current	Idslp_V_{CI}	DC/DC off No clock No input load Ram data not retain	-	-	0.3	3	uA

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3. The listed electrical characteristics are only guaranteed under the controller & waveform provided by Supplier.

Tektronix current probe – TCPA300.

6.3 Panel AC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	VCI=3.0V Enable Clock and Analog by Master Activation Command VGH=20V VGL=-VGH VSH1=15V VSH2=5V VSL=-15V VCOM = -2V No waveform transitions. No loading. No RAM read/write No OTP read /write	VCOM	-2.2	-2	-1.8	V
Positive Source output voltage	V_{SH}		S_0~S_{127}	+14.8	+15	+15.2	V
Negative Source output voltage	V_{SL}		S_0~S_{127}	-15.2	-15	-14.8	V
Positive gate output voltage	Vgh		G_0~G_{295}	+19.5	+20	+20.5	V
Negative gate output voltage	Vgl		G_0~G_{295}	-20.5	-20	-19.5	V

6.4 MCU Interface

6.4.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

Table 6-4-1: MCU interface assignment under different bus interface mode

6.4.2 MCU Serial Interface (4-wire SPI)

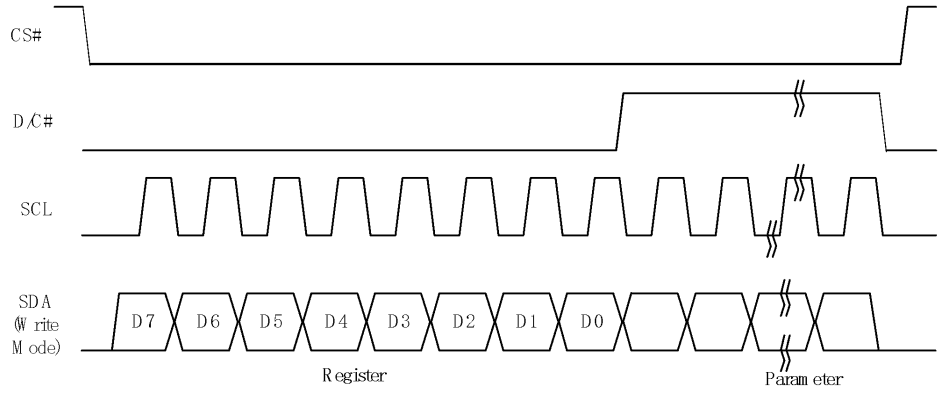
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

In the write mode SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte . The data byte in the shift register is written to the Graphic Display Data RAM /Data Byte register or command Byte register according to D/C# pin.

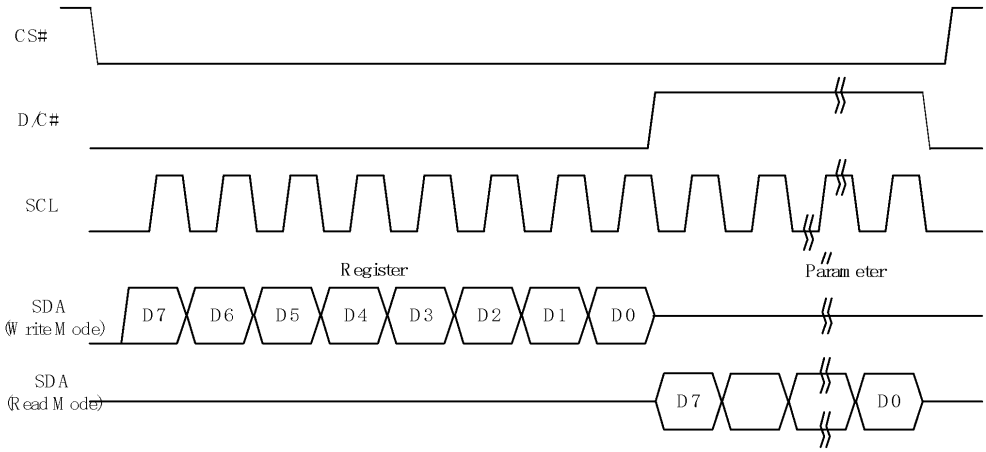
Figure 6-1: Write procedure in 4-wire SPI mode



In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, … D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-2: Read procedure in 4-wire SPI mode



6.4.3 MCU Serial Interface (3-wire SPI)

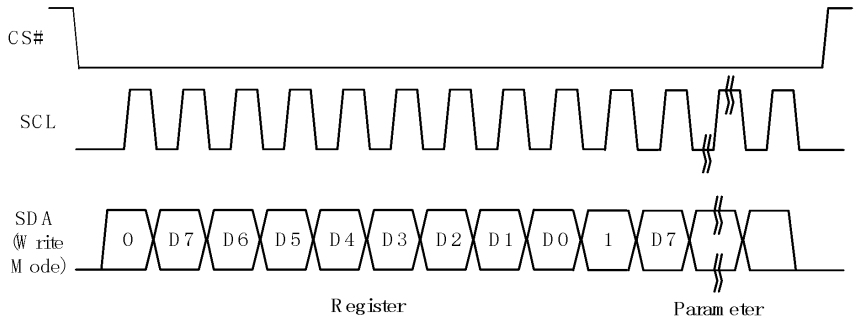
The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Note：↑ stands for rising edge of signal

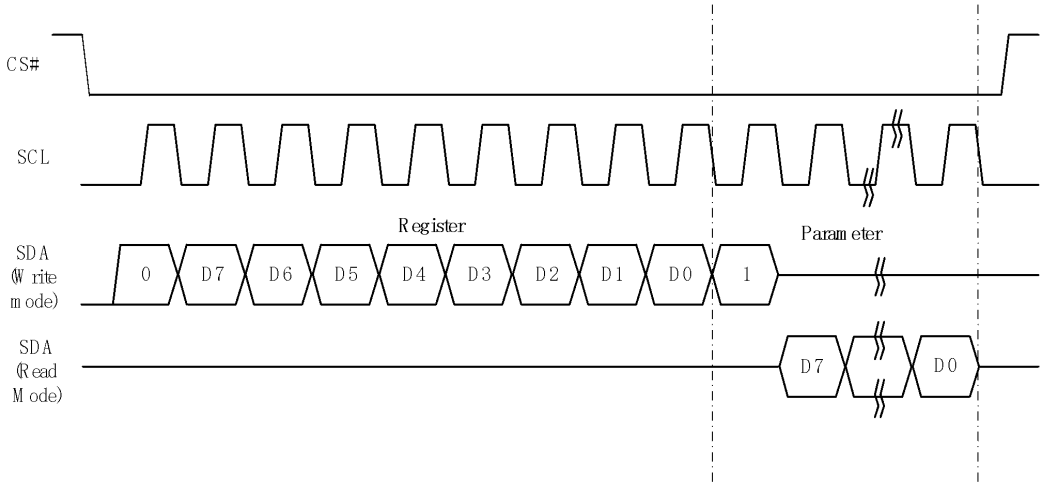
Figure 6-3: Write procedure in 3-wire SPI mode



In the Read mode:

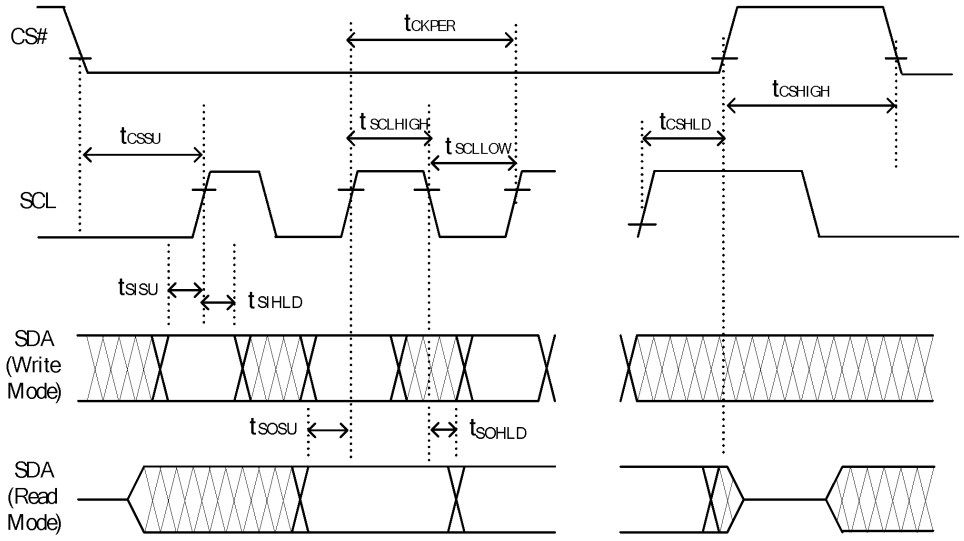
1. After driving CS# to low, MCU need to define the register to be read.
2. D/C=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0.
4. D/C=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, … D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-4: Read procedure in 3-wire SPI mode



6.4.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC.



Changed Diagram

Serial Interface Timing Characteristics

(VDDIO - VSS = 2.2V to 3.7V, TOPR = 23°C, CL=20pF)

Write mode

Symbol	Parameter	Min	Typ.	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	60			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	65			ns
tCSHIGH	Time CS# has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ.	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CS# has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

7.Command Table

Table 7-1: Command Table

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver output control	Gate setting A[8:0]= 0x127 [POR], 296 MUX MUX gate lines setting as (A[8:0] + 1). B [2:0] = 000 [POR]. Gate scanning sequence and direction B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, ... GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, ... B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3...295 (left and right gate interlaced) SM=1, G0, G2, G4 ...G294, G1, G3, ...G295 B[0]: TB TB = 0 [POR], scan from G0 to G295 TB = 1, scan from G295 to G0.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		0	0	0	0	0	B_2	B_1	B_0		
0	0	03	0	0	0	0	0	0	1	1	Gate driving voltage control	Set gate driving voltage A[4:0] = 0x00 [POR] VGH setting from 10V to 20V
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		

A[4:0]	VGH	A[4:0]	VGH
00h	20	0Dh	15
03h	10	0Eh	15.5
04h	10.5	0Fh	16
05h	11	10h	16.5
06h	11.5	11h	17
07h	12	12h	17.5
08h	12.5	13h	18
07h	12	14h	18.5
08h	12.5	15h	19
09h	13	16h	19.5
0Ah	13.5	17h	20
0Bh	14	Other	NA
0Ch	14.5		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source driving voltage control	Set source driving voltage A[7:0] = 0x41 [POR], VSH1 at 15V B [7:0] = 0xA8 [POR], VSH2 at 5V. C[7:0] = 0x32 [POR], VSL at -15V Remark: VSH1>=VSH2
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		

A[7]/B[7] = 1,
VSH1/VSH2 voltage setting from 2.4V to 8.8V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	AFh	6.7
8Fh	2.5	B0h	6.8
90h	2.6	B1h	6.9
91h	2.7	B2h	6
92h	2.8	B3h	6.1
93h	2.9	B4h	6.2
94h	3	B5h	6.3
95h	3.1	B6h	6.4
96h	3.2	B7h	6.5
97h	3.3	B8h	6.6
98h	3.4	B9h	6.7
99h	3.5	BAh	6.8
9Ah	3.6	BBh	6.9
9Bh	3.7	BCh	7
9Ch	3.8	BDh	7.1
9Dh	3.9	BEh	7.2
9Eh	4	BFh	7.3
9Fh	4.1	C0h	7.4
A0h	4.2	C1h	7.5
A1h	4.3	C2h	7.6
A2h	4.4	C3h	7.7
A3h	4.5	C4h	7.8
A4h	4.6	C5h	7.9
A5h	4.7	C6h	8
A6h	4.8	C7h	8.1
A7h	4.9	C8h	8.2
A8h	5	C9h	8.3
A9h	5.1	CAh	8.4
AAh	5.2	CBh	8.5
ABh	5.3	CCh	8.6
ACh	5.4	CDh	8.7
ADh	5.5	CEh	8.8
AEh	5.6	Other	NA

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 9V to 17V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
23h	9	3Ch	14
24h	9.2	3Dh	14.2
25h	9.4	3Eh	14.4
26h	9.6	3Fh	14.6
27h	9.8	40h	14.8
28h	10	41h	15
29h	10.2	42h	15.2
2Ah	10.4	43h	15.4
2Bh	10.6	44h	15.6
2Ch	10.8	45h	15.8
2Dh	11	46h	16
2Eh	11.2	47h	16.2
2Fh	11.4	48h	16.4
30h	11.6	49h	16.6
31h	11.8	4Ah	16.8
32h	12	4Bh	17
33h	12.2	Other	NA
34h	12.4		
35h	12.6		
36h	12.8		
37h	13		
38h	13.2		
39h	13.4		
3Ah	13.6		
3Bh	13.8		

C[7] = 0,
VSL setting from -5V to -17V

C[7:0]	VSL
0Ah	-5
0Ch	-5.5
0Eh	-6
10h	-6.5
12h	-7
14h	-7.5
16h	-8
18h	-8.5
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
Other	NA

0	0	08	0	0	0	0	1	0	0	0	Initial code setting OTP Program	Program initial code setting The command required ENABLE CLOCK SIGNAL. Refer to command 0x22 for detail. BUSY pad will output high during operation.
0	0	09	0	0	0	0	1	0	0	1	Write command for initial code setting	Write command for initial code setting Selection A[7:0] ~ D[7:0]: Reserved Details refer to Application Notes of initial code setting
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	0	0A	0	0	0	0	1	0	1	0	Read command for initial code setting	Read command for initial code setting

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	0C	0	0	0	0	1	1	0	0	Booster soft start control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting.
0	1		1	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:0] -> Soft start setting for Phase1 ■ 8Bh [POR]
0	1		1	B_6	B_5	B_4	B_3	B_2	B_1	B_0		B[7:0] -> Soft start setting for Phase2 ■ 9Ch [POR]
0	1		1	C_6	C_5	C_4	C_3	C_2	C_1	C_0		C[7:0] -> Soft start setting for Phase3 ■ 96h [POR]
0	1		0	0	D_5	D_4	D_3	D_2	D_1	D_0		D[7:0] -> Duration setting ■ 0Fh [POR]

Bit Description of each byte:
A[6:0] / B[6:0] / C[6:0]:

Bit[6:4]	Driving strength selection
000	1(Weakest)
001	2
010	3
011	4
100	5
101	6
110	7
111	8(Strongest)

Bit[3:0]	Min off time setting of GDR [Time unit]
0000 ~ 0011	NA
0100	2.6
0101	3.2
0110	3.9
0111	4.6
1000	5.4
1001	6.3
1010	7.3
1011	8.4
1100	9.8
1101	11.5
1110	13.8
1111	16.5

D[5:0]: duration setting of phase
D[5:4]: duration setting of phase 3
D[3:2]: duration setting of phase 2
D[1:0]: duration setting of phase 1

Bit[1:0]	Duration of phase [Approximation]
00	10ms
01	20ms
10	30ms
11	40ms

Command Table

R/W	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	10	0	0	0	1	0	0	0	0	Deep sleep mode control	Deep sleep mode control: A[1:0] : Description 00 Normal Mode [POR] 01 Enter Deep Sleep Mode 1 11 Enter Deep Sleep Mode 2 After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit deep sleep mode, user required to send HWRESET to the driver
0	1		0	0	0	0	0	0	A_1	A_0		
0	0	11	0	0	0	1	0	0	0	1	Data entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	14	0	0	0	1	0	1	0	0	HV ready detection	HV ready detection A[7:0] = 0x00 [POR] The command required Enable clock signal and Enable Analog. Refer to command 0x22 for detail. After this command initiated, HV ready detection starts. BUSY pad will output high during detection. The detection result can be read from the status bit read (Command 0x2F). A[6:4]=n for cool down duration: 10ms x (n+1) A[2:0]=m for number of Cool Down Loop to detect. The max HV ready duration is 10ms x (n+1) x (m) HV ready detection will be trigger after each cool down time. The detection will be completed when HV is ready. For 1 shot HV ready detection, A[7:0] can be set as 00h.
0	1		0	A_6	A_5	A_4	0	A_2	A_1	A_0		
0	0	15	0	0	0	1	0	1	0	1	VCI detection	VCI detection A[2:0] = 100 [POR] , detect level at 2.3V A[2:0] : VCI level detect A[2:0] / VCI level 011 / 2.2V 100 / 2.3V 101 / 2.4V 110 / 2.5V 111 / 2.6V Other / NA The command required Enable clock signal and Enable Analog. Refer to command 0x22 for detail. After this command initiated, VCI detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	18	0	0	0	1	1	0	0	0	Temperature sensor control	Temperature sensor selection A[7:0] = 0x48 [POR], external temperatrure sensor A[7:0] = 0x80, Internal temperature sensor
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	1A	0	0	0	1	1	0	1	0	Temperature sensor control (write to temperature register)	Write to temperature register. A[7:0] = 0x7F [POR]
0	1		A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4		
0	1		A_3	A_2	A_1	A_0	0	0	0	0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	1B	0	0	0	1	1	0	1	1	Temperature sensor control (read from temperature register)	Read from temperature register.
1	1		A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4		
1	1		A_3	A_2	A_1	A_0	0	0	0	0		
0	0	1C	0	0	0	1	1	1	0	0	Temperature sensor control (Write command to external temperature sensor)	Write command to external temperature sensor. A[7:0] = 0x00 [POR], B[7:0] = 0x00 [POR], C[7:0] = 0x00 [POR], A[7:6] A[7:6] – Select no of byte to be sent 00 – Address + pointer 01 – Address + pointer + 1st parameter 10 – Address + pointer + 1st parameter + 2nd pointer 11 – Address A[5:0] – Pointer setting B[7:0] – 1st parameter C[7:0] – 2nd parameter The command required ENABLE CLOCK SIGNAL. Refer to command 0x22 for detail. After this command initiated, write command to external temperature sensor starts. BUSY pad will output high during operation.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	20	0	0	1	0	0	0	0	0	Master activation	Activate display update sequence The display update sequence option is located at command 0x22. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for display update A[7:0] = 00h [POR] B[7:0] = 00h [POR] A[7:4] Red RAM option 0000 – Normal 0100 – Bypass RAM content as 0 1000 – Inverse RAM content A[3:0] BW RAM option 0000 – Normal 0100 – Bypass RAM content as 0 1000 – Inverse RAM content B[7] Source output mode 0 – Available source from S0 to S175 1 – Available source from S8 to S167
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	0	0	0	0	0	0	0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR)
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Operating sequence	Parameter (in Hex)
Enable clock signal	80
Disable clock signal	01
Enable clock signal → Enable Analog	C0
Disable Analog → Disable clock signal	03
Enable clock signal → Load LUT with DISPLAY Mode 1 → Disable clock signal	91
Enable clock signal → Load LUT with DISPLAY Mode 2 → Disable clock signal	99
Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 1 → Disable clock signal	B1
Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 2 → Disable clock signal	B9
Enable clock signal → Enable Analog → Display with DISPLAY Mode 1 → Disable Analog → Disable OSC	C7
Enable clock signal → Enable Analog → Display with DISPLAY Mode 2 → Disable Analog → Disable OSC	CF
Enable clock signal → Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 1 → Disable Analog → Disable OSC	F7
Enable clock signal → Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 2 → Disable Analog → Disable OSC	FF

0	0	24	0	0	1	0	0	1	0	0	Write RAM (Black White) / RAM 0x24	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM 0x26	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of RAM0x26 = 1 For non-Red pixel [Black or White]: Content of RAM0x26 = 0
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM. According to parameter of command 0x41 to select reading RAM0x24/ RAM0x26, until another command is written. Address pointers will advance accordingly. The 1st byte of data read is dummy data.
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in command 0x29 before reading VCOM value. The sensed VCOM voltage is stored in register. The command required ENABLE CLOCK SIGNAL and ENABLE ANALOG Refer to command 0x22 for detail. BUSY pad will output high during operation.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. A[3:0] = 0x09, duration = 10s. VCOM sense duration = (A[3:0]+1) sec
0	1		0	1	0	0	A_3	A_2	A_1	A_0		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP The command required ENABLE CLOCK SIGNAL. Refer to command 0x22 for detail. BUSY pad will output high during operation.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

A[7:0]	VCOM	A[7:0]	VCOM
08h	-0.2	44h	-1.7
0Ch	-0.3	48h	-1.8
10h	-0.4	4Ch	-1.9
14h	-0.5	50h	-2
18h	-0.6	54h	-2.1
1Ch	-0.7	58h	-2.2
20h	-0.8	5Ch	-2.3
24h	-0.9	60h	-2.4
28h	-1	64h	-2.5
2Ch	-1.1	68h	-2.6
30h	-1.2	6Ch	-2.7
34h	-1.3	70h	-2.8
38h	-1.4	74h	-2.9
3Ch	-1.5	78h	-3
40h	-1.6	Other	NA

0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read for Display Option	Read Register for Display Option: A[7:0]: VCOM OTP Selection (Command 0x37, Byte A) B[7:0]: VCOM Register (Command 0x2C) C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes] H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
1	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
1	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
1	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
1	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
1	1		K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0		

0	0	2E	0	0	1	0	1	1	1	0	User ID Read	Read 10 Byte User ID stored in OTP: A[7:0]]~J[7:0]: UserID (R38, Byte A and Byte J) [10 bytes]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
1	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
1	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
1	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
1	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2F	0	0	1	0	1	1	1	1	Status bit read	Read IC status bit [POR 0x01] A[5]: HV ready detection flag [POR=0] 0: Ready 1: Not Ready A[4]: VCI detection flag [POR=0] 0: Normal 1: VCI lower than the detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
1	1		0	0	A_5	A_4	0	0	A_1	A_0		
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of waveform setting The contents should be written into RAM before sending this command. The command required ENABLE CLOCK SIGNAL. Refer to command 0x22 for detail. BUSY pad will output high during operation.
0	0	31	0	0	1	1	0	0	0	1	Load WS OTP	Load OTP of Waveform Setting The command required ENABLE CLOCK SIGNAL. Refer to command 0x22 for detail. BUSY pad will output high during operation.
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [153 bytes], which contains the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR[n] and XON[nXY] Refer to Session 6.7 WAVEFORM SETTING
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		:	:	:	:	:	:	:	:		
0	1		.	..	.	.	.	.	.	.		
0	0	34	0	0	1	1	0	1	0	0	CRC calculation	CRC calculation command For details, please refer to SSD1680 application note. BUSY pad will output high during operation.
0	0	35	0	0	1	1	0	1	0	1	CRC Status Read	CRC Status Read A[15:0] is the CRC read out value
1	1		A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8		
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	37	0	0	1	1	0	1	1	1	Write Register for Display Option	Write Register for Display Option A[7] Spare VCOM OTP selection 0: Default [POR] 1: Spare B[7:0] Display Mode for WS[7:0] C[7:0] Display Mode for WS[15:8] D[7:0] Display Mode for WS[23:16] E[7:0] Display Mode for WS[31:24] F[3:0] Display Mode for WS[35:32] 0: Display Mode 1 1: Display Mode 2 F[6]: PingPong for Display Mode 2 0: RAM Ping-Pong disable [POR] 1: RAM Ping-Pong enable G[7:0]~J[7:0] module ID /waveform version. Remarks: 1) A[7:0]~J[7:0] can be stored in OTP by command 0x36 2) RAM Ping-Pong function is not support for Display Mode 1
0	1		A_7	0	0	0	0	0	0	0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	1		0	F_6	0	0	F_3	F_2	F_1	F_0		
0	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
0	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
0	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID A[7:0]]~J[7:0]: UserID [10 bytes] Remarks: A[7:0]~J[7:0] can be stored in OTP by command 0x36
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
0	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
0	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
0	0	39	0	0	1	1	1	0	0	1	OTP program mode	OTP program mode A[1:0] = 00: Normal Mode [POR] A[1:0] = 11: Internal generated OTP programming voltage User is required to EXACTLY follow the reference code sequences
0	1		0	0	0	0	0	0	A_1	A_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HIZ. A [7:6] :Select VBD option
0	1		A_7	A_6	A_5	A_4	0	A_2	A_1	A_0		

A[7:6]	Select VBD as
00	GS Transition, Defined in A[2] and A[1:0]
01	Fix Level, Defined in A[5:4]
10	VCOM
11[POR]	HiZ

A [5:4] Fix Level Setting for VBD

A[5:4]	VBD level
00	VSS
01	VSH1
10	VSL
11	VSH2

A[2] GS Transition control

A[2]	GS Transition control
0	Follow LUT (Output VCOM @ RED)
1	Follow LUT

A [1:0] GS Transition setting for VBD

A[1:0]	VBD Transition
00	LUT0
01	LUT1
10	LUT2
11	LUT3

0	0	3F	0	0	1	1	1	1	1	1	End Option (EOPT)	This command defined the display off sequence. Set A[7:0] to 0x22, Display off sequence: • 2 scan frames to discharge TFT pixels voltage • VCOM and HV power will be discharged in a sequence. Set A[7:0] to 0x07, Display off sequence: • No scan frame, keep previous TFT pixels voltage • VCOM will float. VSH1/VSH2/VSL/VGH will be discharged & VGL will float in a sequence. For 0x07 setting, VCOM and VGL are floating after display update. Please wait until the system completely discharge before next operation.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0 : Read RAM corresponding to RAM0x24 1 : Read RAM corresponding to RAM0x26
0	1		0	0	0	0	0	0	0	A_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit for RAM A[5:0]: XSA[5:0], XStart, POR = 00h B[5:0]: XEA[5:0], XEnd, POR = 15h
0	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit for RAM A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 127h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	0	B_8		
0	0	46	0	1	0	0	0	1	1	0	Auto Write RAM0x26 for regular pattern	Auto Write RAM0x26 for regular pattern A[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate
0	1		A_7	A_6	A_5	A_4	0	A_2	A_1	A_0		

A[6:4]	Height	A[6:4]	Height
000	8	100	128
001	16	101	256
010	32	110	296
011	64	111	NA

A[2:0]: Step Width, POR= 000
Step of alter RAM in X-direction according to Source

A[2:0]	Width	A[2:0]	Width
000	8	100	128
001	16	101	176
010	32	110	NA
011	64	111	NA

BUSY pad will output high during operation.

0	0	47	0	1	0	0	0	1	1	1	Auto Write RAM0x24 for regular pattern	Auto Write RAM0x24 for regular pattern A[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate
0	1		A_7	A_6	A_5	A_4	0	A_2	A_1	A_0		

A[6:4]	Height	A[6:4]	Height
000	8	100	128
001	16	101	256
010	32	110	296
011	64	111	NA

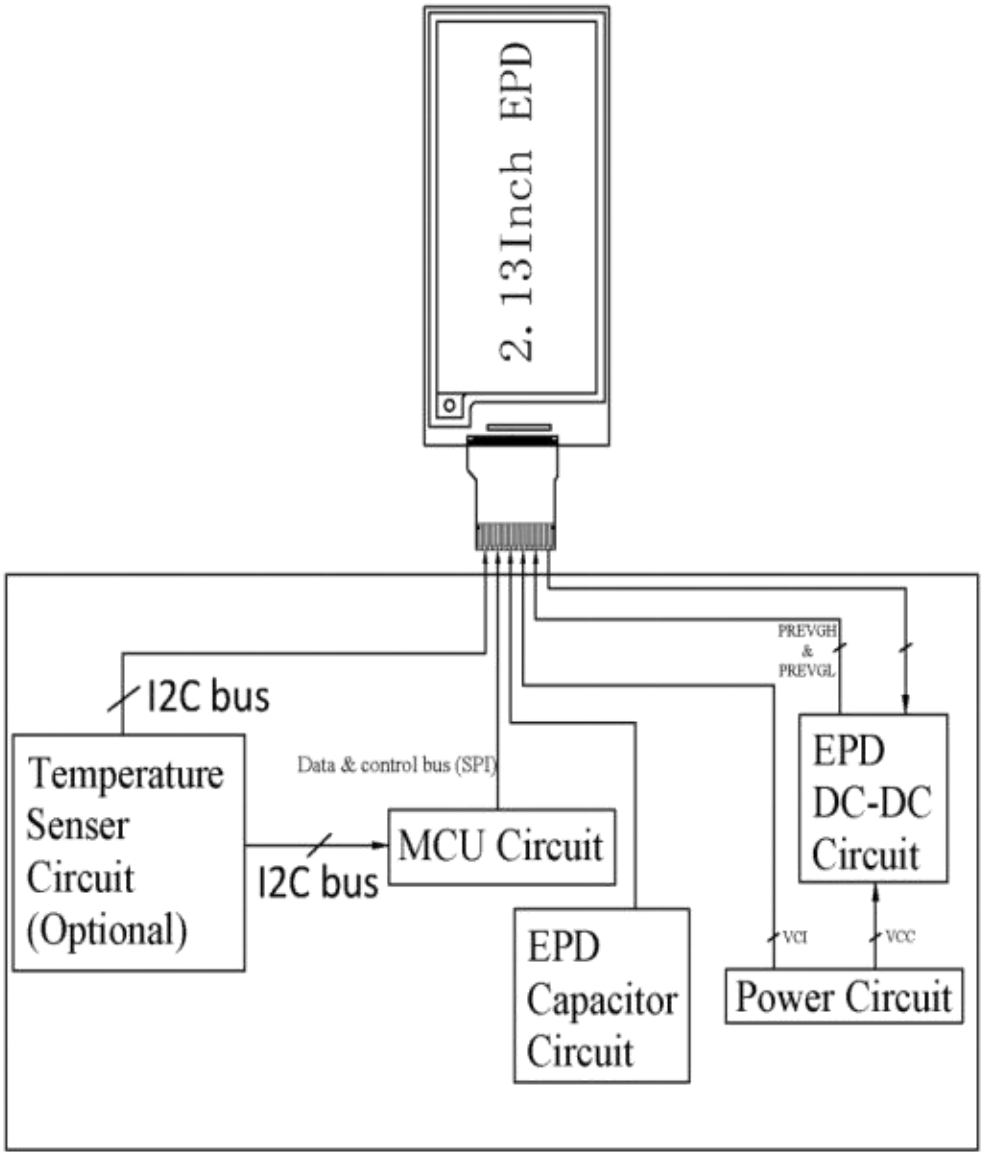
A[2:0]: Step Width, POR= 000
Step of alter RAM in X-direction according to Source

A[2:0]	Width	A[2:0]	Width
000	8	100	128
001	16	101	176
010	32	110	NA
011	64	111	NA

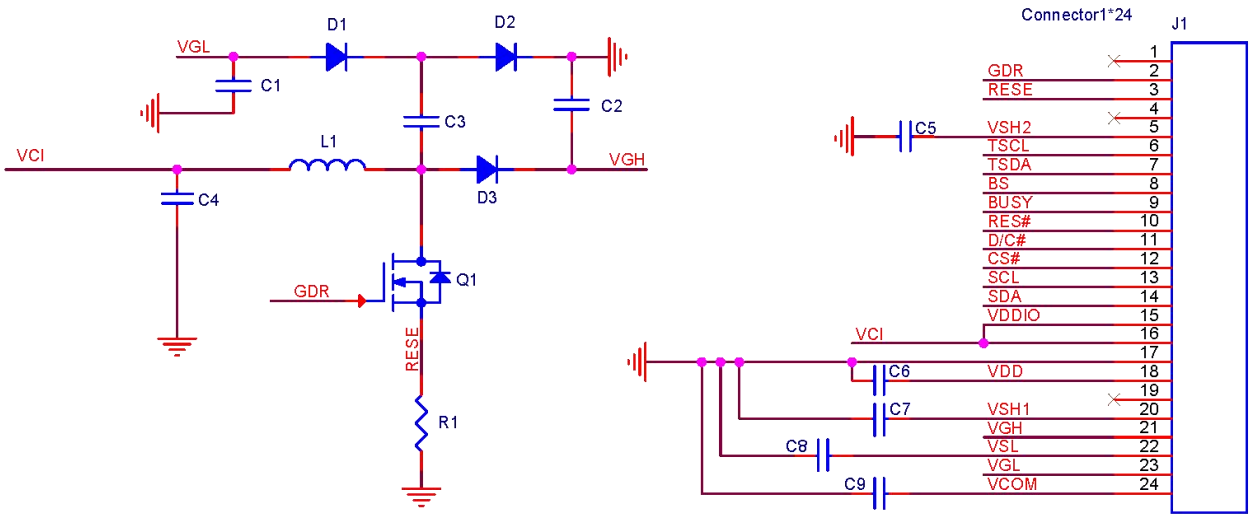
During operation, BUSY pad will output high.

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[5:0]: 00h [POR].
0	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: 000h [POR].
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	0	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate frame memory write or read commands.

8.Block Diagram



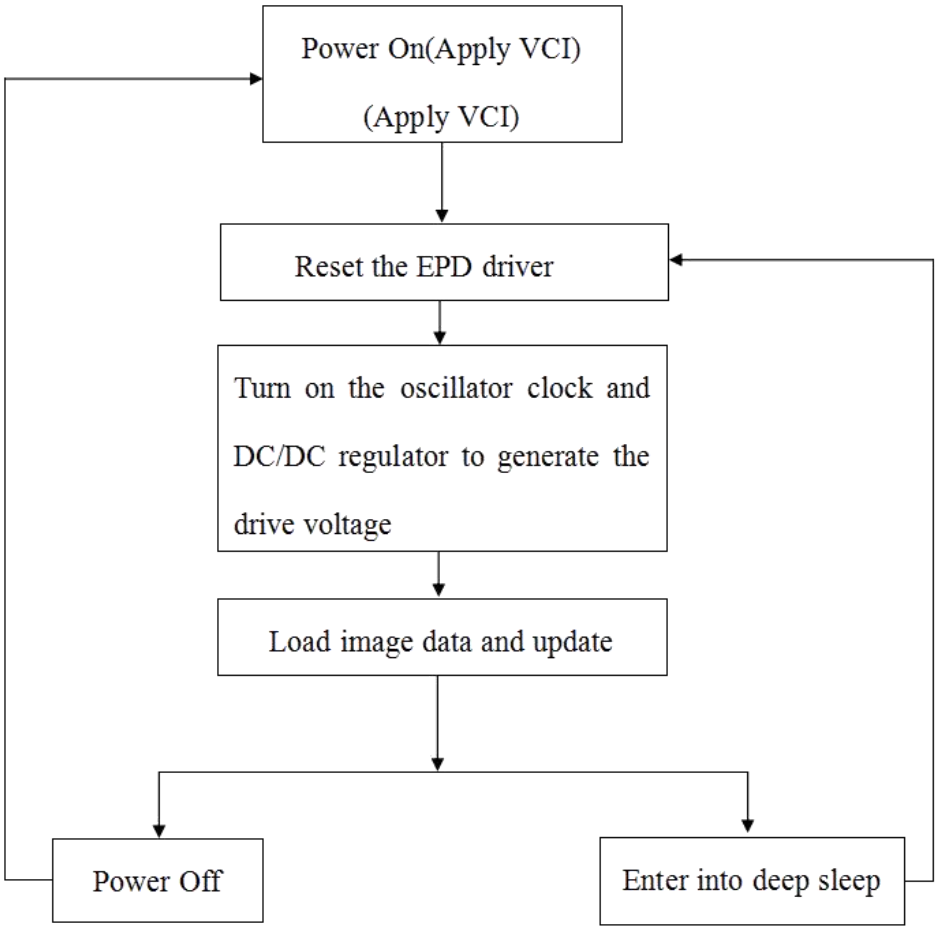
9. Typical Application Circuit with SPI Interface



Part Name	Value	Reference Part
C1C2C3 C5C7C8	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
C4C6	1uF	X5R/X7R; Voltage Rating : 6V or 25V
C9	0.47uF/1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
R1	2.2Ω	0402, 0603, 0805; 1% variation, ≥ 0.05W
D1 D2 D3	Diode	MBR0530 1) Reverse DC voltage ≥30V 2) Io ≥500mA 3) Forward voltage ≤ 430mV
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage ≥30V 2) Vgs(th) = 0.9V (Typ), 1.3V (Max) 3) Rds on ≤ 2.1Ω @ Vgs = 2.5V
L1	47uH	CDRH2D18 / LDNP-470NC Io= 500mA (Max)

10.Typical Operating Sequence

10.1 LUT from OTP Operation Flow



10.2 LUT from OTP Operation Reference Program Code

ACTION	VALUE/DATA	COMMENT
POWER ON		
delay	10ms	
PIN CONFIG		
RESE#	low	Hardware reset
delay	200us	
RESE#	high	
delay	200us	
Read busy pin		Wait for busy low
Command 0x12		Software reset
Read busy pin		Wait for busy low
SET VOLTAGE AND LOAD LUT		
LOAD IMAGE AND UPDATE		
Command 0x24	4000bytes	Load image (128/8*250)(BW)
Command 0x20		
Read busy pin		Wait for busy low
Command 0x10	Data 0X01	Enter deep sleep mode
POWER OFF		

11. Reliability Test

NO	Test items	Test condition
1	Low Temp. Operation	0℃ for 240 hrs
2	High Temp. High Humidity Storage	60℃ / 80% RH for 240 hrs
3	Thermal Shock	1cycle：-25℃ / 30min ~ 60℃ / 30min for 100 cycles
4	HighTempLowhumidityStorage	60℃/35%RH for 240hrs
5	High Temp. High Humidity Operation	40℃/80%RH for 240hrs
6	ESD Gun	Air+/-4KV;Contact+/-2KV Contact+/-2KV(HBMC:100pF;R:1.5k ohm) Contact+/-200V(MMC:200pF;R:0 ohm) (Naked EPD display,including IC and FPC area)
7	Vibration test	Frequency: 10-500Hz Direction: X, Y, Z Duration: 1 hour in each direction
8	Dropping test	The test height is determined by the weight of the test object. Weight ≤20KG, drop height 1000mm Weight ≤50KG, drop height 500mm Weight ≤100KG, drop height 250mm

Note：1. Stay white pattern for storage and non-operation test.
2. Operation is black→white pattern, the interval is 150s.

12. Quality Assurance

12.1 Environment

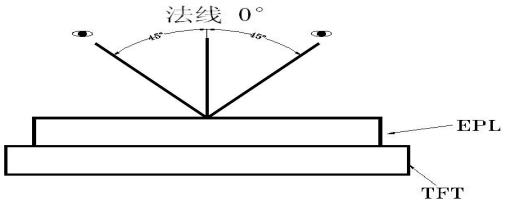
Temperature： 23±3℃

Humidity： 55±10%RH

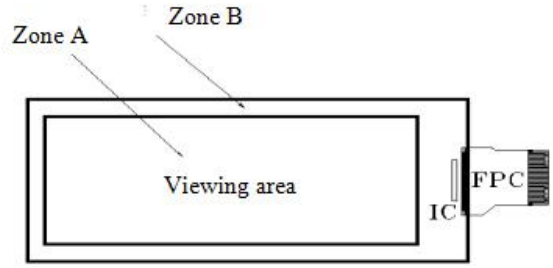
12.2 Illuminance

Brightness:1200～1500LUX;distance:20-30CM;Angle:Relate 45°surround.

12.3 Inspect method

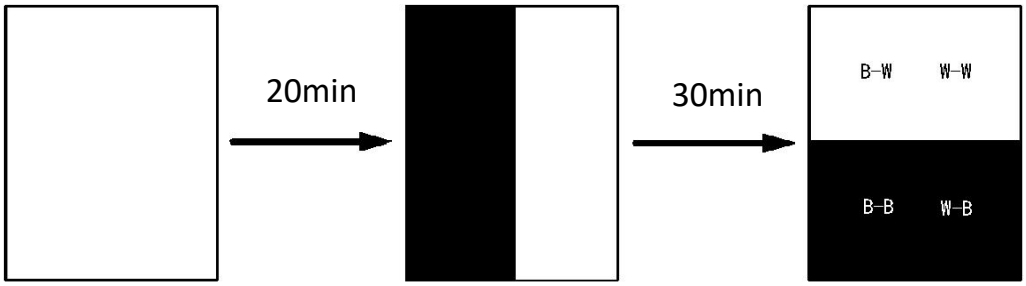


12.4 Display area



12.5 Ghosting test method

Two-color ghosting is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by Supplier.



1）Measurement Instruments：X-rite i1Pro

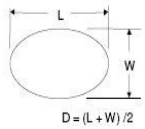
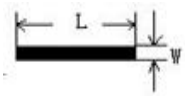
2）Ghosting formula:

W ghosting：△L= Max (Δ L(W-W, B-W)) - Min (Δ L(W-W B-W))

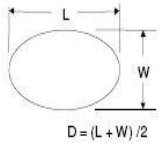
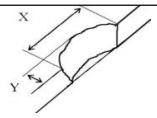
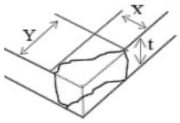
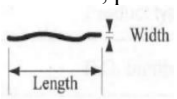
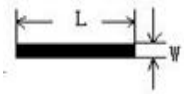
K ghosting：△L= Max (Δ L(W-B, B-B)) - Min(Δ L(W-B, B-B))

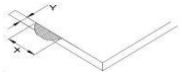
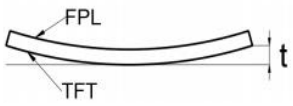
12.6 Inspection standard

12.6.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Display complete Display uniform	MA	Visual inspection	Zone A
2	Black/White spots	 D≤0.25mm，Allowed 0.25mm＜D≤0.4mm。 N≤4 allowable D＞0.4mm is not allowed	MI	Visual Inspection card	Zone A
3	Show B/W lines	 L≤0.4mm,W≤0.1mm negligible 0.4mm＜L≤1.0mm 0.1mm＜W≤0.4mm N≤4 allowable L＞1.0mm ,W＞0.4mm is not allowed	MI	Visual Inspection card	Zone A
4	Ghost image	Allowed in switching process	MI	Visual	Zone A
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection card	Zone A
7	Short circuit/ Circuit break/ Display abnormal	Not Allow	MA	Visual	Zone A
8	Corner mura	X>1mm，Y>1mm,not allow 	MI	Visual/Ruler	Zone A

12.6.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 D≤0.25mm negligible 0.25mm＜D≤0.4mm N≤4 allowable D＞0.4mm is not allowed	MI	Visual/ inspection Card	Zone A
2	Chips/Scratch/ Edge crown	 X≤3mm,Y≤0.5mm t= not counted，and without affecting the electrode , permissible  2mm≤X or 2mm≤Y t= not counted.and without affecting the electrode , permissible  W≤0.1mm,L≤5mm, without affecting the electrode , n≤2	MI	Visual / Ruler	Zone A/B
3	TFT Cracks	Not Allow	MA	Visual / Microscope	Zone A/B
4	Dirty/ foreign body	Allowed if can be removed	MI	Visual / clean cloth	Zone A / B
5	FPC broken/ Goldfingers oxidation/ scratch	 Not Allow	MA	Visual / Microscope	Zone B
6	B/W Line	 L≤0.4mm,W≤0.1mm negligible 0.4mm＜L≤1.0mm 0.1mm＜W≤0.4mm N≤4 allowable L＞1.0mm ,W＞0.4mm is not allowed	MI	Visual / Ruler	Zone A

7	TFT edge bulge /TFT chromatic aberration	 TFT edge bulge： X≤3mm，Y≤0.3mm Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A/B
8	Electrostatic point	D≤0.2mm, allow 0.2mm＜D≤0.35mm ,n≤4 allow D＞0.35mm is not allowed (n≤5 items are allowed within 5 mm in diameter)	MI	Visual /inspection card	Zone A
9	PCB damaged/ Poor welding/ Curl	PCB（Circuit area）damaged Not Allow PCB Poor welding Not Allow PCB Curl≤1%	MA	Visual / Ruler	Zone B
10	Edge glue height/ Edge glue bubble	Edge Adhesives H≤PS surface (Including protect film) Edge adhesives overflow onto protect film ≤1/2 FPL to PS Margin width Length excluding Edge adhesives seep in≤1/2 FPL Margin width Length excluding Edge adhesives bubble：bubble Width ≤1/2 Margin width；Length ≤5.0mm。n≤5	MI	Visual / Ruler	Zone B
11	Protect film	Surface scratch but not effect protect function, Allowed	MI	Visual	Zone A/B
12	Silicon glue	Thickness≤PS surface(With protect film): Full cover the IC; Shape: The width on the FPC≤1.0mm (Front) The width on the FPC≤1.0mm (Back) smooth surface, No obvious raised.	MI	Visual/Ruler	Zone B
13	Warp degree (TFT substrate)	 t≤1.0mm	MI	Ruler	Zone B
14	Color difference in COM area (Silver point area)	Allowed	MI	Visual	Zone B
15	Corner and edge damage of FPL	Corner and edge damage ≤ 1/2 border width 	MI	Visual / Ruler	Zone A

13. Handling, Safety, and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
Product Environmental certification	
ROHS	
REMARK	
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.	
Transport environment	
When the humidity of transportation environment is between 45%RH~70%RH, the product can be stored for 30 days, and the product can be stored for 10 days if it is lower or higher than this range	